



Janus
Technologies

School of Engineering Science
Burnaby, BC V5A 1S6
ensc440-darm@sfu.ca

April 19, 2009

Mr. Patrick Leung
School of Engineering Science
Simon Fraser University
Burnaby, British Columbia
V5A 1S6

Re: ENSC 440 Post-Mortem for the SolarMax Wireless Gateway Device

Dear Mr. Leung:

The attached Post-Mortem document outlines the process and team dynamics that our group experienced while designing and implementing the SolarMax Wireless Gateway Device. The project involved designing and implementing a programmable unit that allows for wireless control and monitoring of solar panels as well as a web-based interface.

This document outlines the current state of the project, future development plans, and any deviations from original designs that were implemented. Also included are budgetary and time constraints, as well as individual reflections on the technical and interpersonal experiences we encountered.

Janus Technologies consists of four motivated, innovative, and talented fifth-year engineering students: Adam Ciapponi, Matthew Giassa, Daniel Hilbich, and Robert Szolomicki. If you have any questions or concerns about our proposal, please feel free to contact me by phone at (604) 345-4664 or by e-mail at ensc440-darm@sfu.ca.

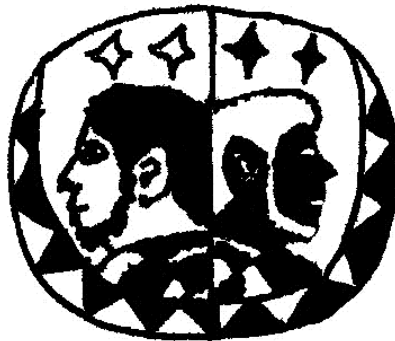
Sincerely,

Adam Ciapponi
President and CEO
Janus Technologies

Enclosure: *Post-Mortem for the SolarMax Wireless Gateway Device*

Janus Technologies

Post-Mortem for the SolarMax Wireless Gateway Device



Project Team: Adam Ciapponi
Matthew Giassa
Daniel Hilbich
Rob Szolomicki

Contact Person: Adam Ciapponi
ensc440-darm@sfu.ca

Submitted To: Patrick Leung – ENSC440
Steve Whitmore – ENSC305
School of Engineering Science
Simon Fraser University

Date Issued: April 19, 2009

Revision: 1.2



Table of Contents

List of Figures	iii
Glossary	iv
1. Introduction	1
2. Current State of the Prototype	1
2.1. Features Currently Implemented	1
2.1.1. Tier 1	1
2.1.2. Tier 2	2
2.1.3. Tier 3	2
2.2. Deviation from Design Specification	2
2.3. Challenges Encountered.....	3
3. Future Plans	4
3.1. Data Logging.....	4
3.2. Full Integration of the Ethernet board	4
3.3. USB connectivity.....	4
3.4. Digital control of Antenna power.....	4
3.5. Reduce physical dimensions	5
3.6. Reduce cost	5
4. Budgetary and Time Constraints	5
4.1. Budget.....	5
4.2. Time	5
5. Interpersonal and Technical Experiences	6
5.1. Adam Ciapponi.....	6
5.2. Matthew Giassa	6
5.3. Daniel Hilbich	7
5.4. Robert Szolomicki	8
6. Conclusion	8
7. References.....	10



List of Figures

Figure 1: SPI Clock out - Incorrect frequency	3
Figure 2: SPI CLK out - Slow discharge	3
Figure 3: UART to USB design	4



Glossary

BFSK	Binary Frequency Shift Keying
BPSK	Binary Phase Shift Keying
CRC	Cyclic Redundancy Check
DHCP	Dynamic Host Configuration Protocol
DNS	Domain Name System
DPST	Double-Pole Single-Throw
ECC	Error Correction Code
FAT	File Allocation Table
FCC	Federal Communications Commission (US)
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
LCD	Liquid Crystal Display
PCB	Printed Circuit Board
PIC	Programmable Intelligent Computer
RC	Resistor-Capacitor
RoHS	Restriction of Hazardous Substances Directive
USB	Universal Serial Bus
TCP/IP	Transmission Control Protocol / Internet Protocol
WAP	Wireless Access Point
WGD	Wireless Gateway Device



Janus
Technologies

School of Engineering Science
Burnaby, BC V5A 1S6
ensc440-darm@sfu.ca

Wireless Device

An electronic device capable of communicating with a similar such device through a wireless medium, such as through the use of modulated radio waves.



1. Introduction

2. Current State of the Prototype

The following sections compare the current device features to those outlined in *Design Specifications for the SolarMax Wireless Gateway Device* [1] and *Functional Specifications for the SolarMax Wireless Gateway Device* [2].

2.1. Features Currently Implemented

The functionality of the device was broken down into three tiers. Tier 1 consisted of fundamental features required for completion of the project. Tier 2 consisted of functionally relevant features that would be implemented if time permitted. Tier 3 consisted of optional features that were not very necessary but would have provided additional value to the project.

2.1.1. Tier 1

All of the Tier 1 features were implemented and tested, which was required for successful completion of the project.

The pushbutton interface was successfully completed. Currently only one of the buttons is required for cycling through the LCD menu which replicates the functionality of the SolarMax Remote once the SolarMax device setup has been completed.

The LCD output system was successfully completed and shows the current state of the device as received over the wireless. LED feedback was also completely implemented for the user to confirm when the buttons were pushed.

The wireless transceivers were successfully implemented and can operate within the specified range, though reliability of data transfer has provided some complications. Although error checking does work as outlined in [1], with large, 72 byte packets too many characters tend to contain a single byte with an error in them due to the bit error rate of the wireless channel. We have begun work on a system with both smaller packet size and ACK/NAK control to provide additional reliability beyond that outlined in the design specification. The ACK and NAK will be of a custom format where the data includes a checksum. If this checksum is not verified, a timeout can initiate a resend. In addition to added verification of the received signal, we will be implementing a communication standard where a 2 byte header, along with the length, packet number, data and checksum will be included in each transmission to ensure reliable data is reformed at the 'master PIC' from the SolarMax.



2.1.2. Tier 2

Some of the Tier 2 functionality was implemented, which was acceptable as these features were optional.

The Network Interface system is very close to completion. It currently can access the Internet and provide a web page with the current device stats and an AJAX interface for modifying the device parameters. All that remains is to completely incorporate it with the main board PIC using I²C, which is not anticipated to take much time as we have fully functional and tested I²C libraries for PIC-to-PIC communication.

The SD card data logging system is currently not operational. Extensive work was done on the SD card through use of Microchip's provided libraries, but unfortunately the feature still remains incomplete. All the pins are currently wired on the board for the device and it remains a feature for future work. Electrically, the feature is complete but it remains to be shown that the SPI communications can function between the SD device and the master PIC.

2.1.3. Tier 3

Some of the Tier 3 functionality was implemented, which was acceptable as these features are purely optional. No work was done on the USB RS232 interface and as such that module has not been implemented.

RoHS compliance was implemented through careful choices in selection of parts. All parts used in the fabrication of the board are RoHS compliant. Lead solder was used for the creation of the prototype but silver solder is planned for the finalized design, ensuring full RoHS compliance.

2.2. Deviation from Design Specification

The only deviations of note from the design specification for implemented features were with the pushbutton interface and the network interface board. As testing progressed it became clear that there was an intolerable lag between when the processor discovered a button was pushed and how long the user had to press the button. When removing the hardware de-bouncing, the button sensitivity increased. This led to the implementation of pure software de-bouncing where upon the positive edge detection on the button pin, the microprocessor would initiate a 80ms delay timer which would then query the possible button pushes. This improved reliability substantially and false button pushes were never detected. With difficulties using SPI, we have changed the network interface board to work with I²C which turned out to benefit the design greatly as with the number of external peripherals increased, the number of pins necessary to coordinate communications stayed the same. The same could not be said about the implementation of SPI used as for each peripheral introduced to the design, an additional slave select line had to be introduced. The LCD board initially used an 8-bit mode of operation but due to an inherent flaw in the LCD module, only 4-bit mode was supported



which lead the design to no longer require 8 output lines to the LCD. This in-turn allows for the next revision to use fewer PIC microprocessors.

2.3. Challenges Encountered

Significant difficulties were encountered with the serial peripheral interface (SPI) that was planned to be used both for PIC-to-PIC communications as well as the SD card data logging capability. After two weeks of attempting to initialize SPI on our PICs using both code from Microchip and other sources, we were forced to use alternative methods. Because of this, data logging with an SD card was put on hold. Below in Figure 1 and Figure 2 are examples of the aberrant waveforms observed when testing SPI.

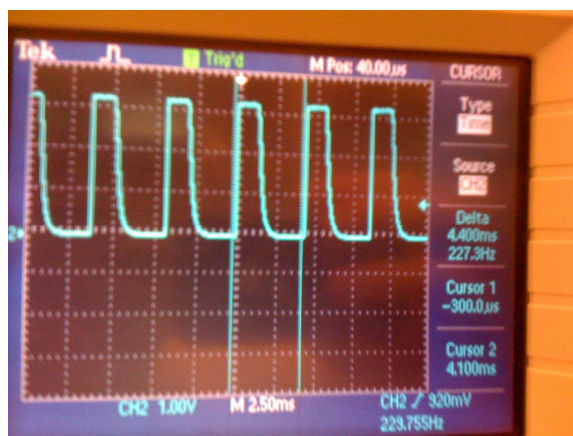


Figure 1: SPI Clock out - Incorrect frequency

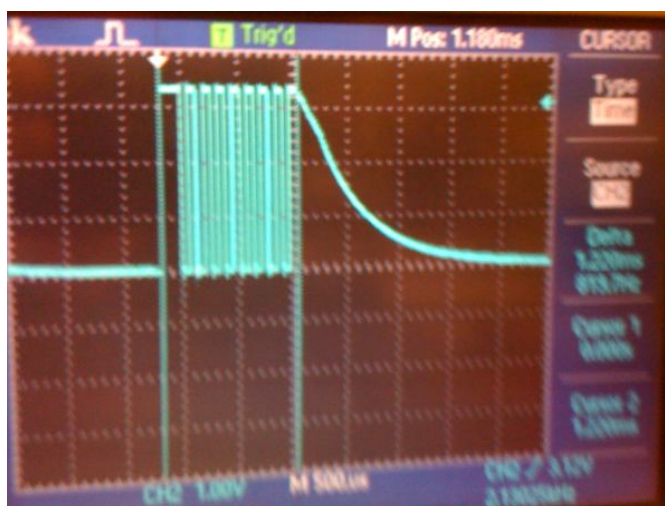


Figure 2: SPI CLK out - Slow discharge

Since PIC-to-PIC communication was vital to the success of our project, we decided to use I²C instead. In order to ensure that we could get I2C working, we split into two groups. Each group went through the Microchip documentation as well as many other



sources on the internet and created an independent solution to I2C. These two solutions were then integrated together and tested. The integrated code worked very well needing only minimal changes.

3. Future Plans

Our future plans for this project are outlined in the following sections.

3.1. Data Logging

Data logging is one feature we hope to have implemented in the future. If we still cannot find the problem with our SPI code, alternatives do exist such as use of a USB mass storage device or SD card libraries that operate with I²C.

3.2. Full Integration of the Ethernet board

This module is nearly complete and only needs to be configured to work with our existing I²C libraries.

3.3. USB connectivity

This is a feature we would like to have implemented so the SolarMax could be easily updated without access to an internet connection. This addition can be done with the following chip design shown below in Figure 3. The chip labeled U3 is the FT232BM.

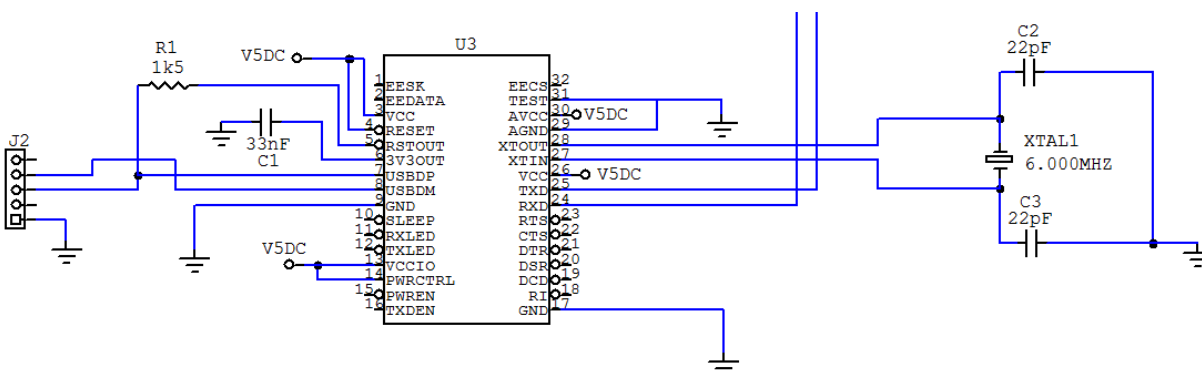


Figure 3: UART to USB design

3.4. Digital control of Antenna power

A biasing resistor is used to establish the range of the wireless transceiver. If this could be controlled digitally with the PIC and optimized, it would result in significant power savings. For instance, the device would only transmit up to 20 feet instead of the maximum range when it is close to the gateway device.



3.5. Reduce physical dimensions

The overall device could be reduced in size through creation of a PCB encompassing the whole device and use of surface mount chips, capacitors and resistor. It is also feasible to replace the three independently operational PICs to one large PIC that used a Quad Flat Package. The PIC24F QFP contains a larger number of I/O pins and communication modules. That can facilitate all the operations necessary to replicate the current design without the DIP modules.

3.6. Reduce cost

Refinements to the individual part selection as well as using surface mount chips would significantly reduce the cost of the entire device.

4. Budgetary and Time Constraints

4.1. Budget

The current implementation of our wireless gateway device, which was presented at our project demo, did not exceed allocated budget. Costs were also as expected, and we anticipated the costs shown in our bill of materials well in advance of the initial stages of project development.

We are currently able to design the actual main board and enclosure for our wireless gateway device for under \$80 (CAD) per unit. Although this is more expensive that we would have hoped, we are already able to keep the individual wireless transceiver/RS232 boards to under \$35 (CAD) per unit. Both devices can be further reduced in cost by further research into different chip packages, board development techniques, and so on.

Analytic Systems has agreed to reimburse Janus Technologies for the cost of components and parts in advance of project development, so no team members will incur any financial losses as a result of this project.

4.2. Time

Although the majority of our product features were implemented without issue, our initial GANTT chart did not reflect project progress very accurately. Due to several persistent, unexpected bugs, project progress was often sporadic. Fixing certain bugs almost merits a project milestone, due to the complexity of some of them.



5. Interpersonal and Technical Experiences

5.1. Adam Ciapponi

I really enjoyed being a part of our ENSC440 project team because it gave me real insight into working with people with different ways of looking at the same problem. I think one of the assets of our group was that everyone seemed to go about solving technical problems in different way resulting in multiple solutions to choose from. As far as working with the rest of the team goes, it was a blast working with them and we never really had any fights or problems with each other despite some intense frustration with technical problems such as SPI.

ENSC440 gave me considerable experience with low-level firmware programming and hardware design. No other course really taught that kind of valuable programming knowledge that will no doubt help me during my coop at PMC-Sierra in the summer doing firmware. Furthermore, ENSC440 was the first course that I really learned how to do overall hardware design from designing basic boards with PICs to creating our own PCBs. Additionally, I came into the course with only a basic knowledge of soldering and I greatly increased my skill with a soldering iron.

Although in retrospect it was fun, I'm very relieved it is over. The pressure to finish the project for the demo deadline led to many long days in the lab mainly as the result one persistent bug. Fortunately, we planned a fair bit of time for integration and were able to fully explore alternative solutions that ended up being more efficient overall.

Overall, the project provided me with valuable experience and I look forward to working further with the rest of the team to get the product ready to sell to Analytic Systems.

5.2. Matthew Giassa

Throughout the semester, ENSC440 frequently challenged me and kept me motivated to continue development on our project. We chose a very ambitious project, and even further increased the difficulty by insisting that all development take place from the ground-up: no daughter boards or product evaluation boards were to be used to speed up development. This allowed each of us to gain considerable insight into the complete development lifecycle for a single system.

Working with the team I did was an excellent experience. Every team member was very dedicated to the project, and a very no-nonsense approach was shared by all, allowing the project to continue without any disturbances, even during midterm season.



With the skills I have gained from this course, I feel that I am ready to take on more difficult independent projects. This course has greatly expanded my skill set in many respects. This will no doubt prove very useful in future development of our wireless gateway device.

5.3. Daniel Hilbich

ENSC 440, for me, has been nothing less than bitter sweet: bitter, in the sense that I don't think any person could remain sane given the amount of stress and technical challenges experienced in such a short time, and sweet in the sense that this truly has given me an experience which makes my engineering degree personally rewarding. I cannot say that I enjoyed all of my time in the lab, or that I felt good about every day that I spent working away on our project, but I can say that amalgamating all of my knowledge and previous technical experience into one project has been something that I am very proud of.

From a technical standpoint, this project has been quite challenging; often I felt that, while I did have a diverse skill set from previous courses, I really would be lost when trying to tackle a technically challenging project from start to finish. How will you know what parts you will need? How will you estimate the cost? How can you be sure it will even work?! Experiencing 440 has given me the confidence and know-how to tackle these types of difficult problems in their entirety, such that instead of feeling lost, I now know how much a dedicated group of individuals can actually accomplish. Firmware design has always been a challenge for me, and the amount required for our project has greatly increased my proficiency and will no doubt aid me in my upcoming coop centered around embedded C firmware.

I have also learned a great deal about group dynamics. Fortunately for our group, we did not suffer any interpersonal 'blow-outs'. I think we demonstrated some prudence in the beginning by choosing a group such that, although we weren't all friends at the time, each of us had worked with at least one other member and knew that each and every one of us was reliable. Often in other courses you find that individual styles may clash, and expectations may not be fulfilled; by this time in our respective degrees, I think we all realized what we each needed to bring to the table, and we had the ability to deal with situations in both a logical and sensitive manner. I also am greatly appreciative of my team mates; I have trouble expressing just how nice it is to be working on one component and have another member tell you they've just completed another. These individual contributions towards the group kept us all quite satisfied.



All in all, I'm just glad it's over. We have a project that we can all be proud of, and one that we can even sell! No one should have to work for extended periods of time like we did on 440, but at least we can all look back and be proud of what we accomplished.

5.4. Robert Szolomicki

ENSC 440 was an eye opening experience for me as it allowed me to discover how much could be accomplished in such a short period of time when you're working with a group that really has the ability to produce results.

It's also nice to experience having that second (third or fourth) opinion when tackling a problem. It was also interesting to observe the power of multiple people independently producing a solution and finding the optimal parts of both designs to produce a synergetic result. In addition, I learned how to produce circuit board PCB's with the toner transfer method of manufacturing. This sped up the time it took to make a complicated circuit and provided an element of elegance to the design. It also sharpened my skills for PCB layout with an entirely new software package, KiCad, as it actually served a purpose to produce the said layout.

As I mentioned in the presentation, this course provided us with a greater sense of urgency because the opportunity for failure was palpable. In addition to that, we are producing something that eventually needs demoing to a third party. This adds an extra layer of difficulty because if something doesn't work, there's more to lose than what there was at an institution. This added vested interest had pushed us to work harder than we would have if we expected this to be tossed aside when we were finished. The fact we were encouraged to make it marketable for use outside of ENSC 440 had really made the project more 'real.' This goes for every project in ENSC 440 in general as it feels like we, as engineers, have the power to make something for the world and sell it!

By doing this project and jumping over all of the hurdles of its design, I was able to establish a sense of confidence that, from start to finish, I am capable of producing a functional product that serves a purpose and can be marketable. I always note ideas I would like to build in the future and after ENSC 440, I absolutely see myself producing them.

6. Conclusion

The SolarMax Wireless Gateway device is nearly ready for a demonstration to Analytic Systems, but for the time being remains a work in progress; we have completed the essential components of the design, along with some non essential components, and have a foot in the door on others. The wireless and Ethernet component are complete, but do require a few additions to become fully operational. The LCD interface is fully



Janus
Technologies

School of Engineering Science
Burnaby, BC V5A 1S6
ensc440-darm@sfu.ca

complete, and we do not anticipate any work of further significance in that regard. Data logging needs to be completed in the future, although we have completed a large portion of the development already. The experiences we have all endured have given us the technical prowess to not only create an outstanding WGD for Analytic Systems, but to also tackle any future problems we might encounter as engineers. ENSC 440 has no doubt been a challenge and at times physically exhausting, but it has given us not only a marketable product, but a truly rewarding experience as well.



7. References

- [1] Ciapponi, A., M. Giassa, D. Hilbich, and R. Szolomicki, *Design Specifications for the SolarMax Wireless Gateway Device*, 2009
- [2] Ciapponi, A., M. Giassa, D. Hilbich, and R. Szolomicki, *Functional Specifications for the SolarMax Wireless Gateway Device*, 2009
- [3] A Guide to Debouncing. 2009. *The Ganssle Group*. 4 Mar 2009. <<http://www.ganssle.com/debouncing.pdf>>
- [4] Patrick Leung, Informal discussion about hardware pushbutton debouncing solutions, 3 Feb 2009.
- [5] LT Series – Long Range RF Transceiver Modules. 2009. *Linx Technologies Product Catalog*. 20 Feb 2009. <<http://www.linxtechnologies.com/Products/RF-Modules/LT-Series-RF-Transceiver-Module/>>
- [6] ENC28J60. 2009. *Microchip Product Catalog*. 20 Jan 2009. <<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en022889>>
- [7] Ethernet Solutions Design Center. 2009. *Microchip Design Resources*. 6 Jan 2009. <www.microchip.com/stellent/idcplg?IdcService=SS_GET_PAGE&nodeId=1489>
- [8] Internetworking Basics. 2009. *Cisco Internetworking Technology Handbook*. 9 Feb 2009. <<http://www.cisco.com/en/US/docs/internetworking/technology/handbook/Intro-to-Internet.html>>
- [9] Standard SD Cards. 2009. *Sandisk Products Catalog*. 9 Feb 2009. [http://www.sandisk.com/Products/Item\(2363\)-SDSDB-8192-A11-SanDisk_Standard_SDHC_Card_8GB.aspx](http://www.sandisk.com/Products/Item(2363)-SDSDB-8192-A11-SanDisk_Standard_SDHC_Card_8GB.aspx)