March 9th, 2014
Dr. Andrew Rawicz
School of Engineering Science
Simon Fraser University
Burnaby, BC, V5A 1S6

Re: ENSC 440 Design Specification for an Advanced Function Maximum Power Point Tracking Battery Charger for 12 Volt Lead-Acid and 16 Volt Ni-Cad Batteries

Dear Professor Rawicz:

The attached document illustrates the Design Specification for an Advanced Function Solar Power Batter Charger for 12 Volt Lead-Acid and 16 Volt Ni-Cad Batteries proposed by Solar Solutions. Our product, Helios Mk-I allows the user to efficiently charge a battery using a solar panel as a power source by implementing an MPPT algorithm.

The purpose of the Design Specification is to provide a proof-of-concept model only. Future improvements for the design of Helios Mk-I is discussed and may not be implemented due to time constraints.

Solar Solutions consists of five members and is receiving funding from Analytic Systems, which is North America's fastest growing power conversion company. You may contact me by phone at 604-761-4568 or by email at rhargrov@sfu.ca if you have any concerns or questions about our proposal.

Sincerely,

Richard Hargrove

Richard Hargrove
President and CEO
Solar Solutions

Enclosure: *Functional Specification for an Advanced Function Maximum Power Point Tracking Battery Charger for 12 Volt Lead-Acid and 16 Volt Ni-Cad Batteries*

Design Specification for an Advanced Function Maximum Power Point Tracking Battery Charger for 12 Volt Lead-Acid and 16 Volt Ni-Cad Batteries

ENSC 440: Capstone Project, ENSC 305: Project Documentation

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Revision: *1.9*

Abstract

The design specification for the Helios Mk-I (HM1) provides a set of detailed descriptions for the design and development of our proof-of-concept model. The design specifications in this document are solely for the proof-of-concept model. Therefore, we will only discuss design considerations pertaining to the functional requirements as specified in the document *Functional Specification for an Advanced Function Maximum Power Point Tracking Battery Charger for 12 Volt Lead-Acid and 16 Volt Ni-Cad Batteries*[1].

The document provides an outline of the design and justifies the design choices as well as future implementations that can be made. The main component of the battery charger is the Printed Circuit Board (PCB) design of the cascaded buck boost converter. This will provide the switching necessary to step the voltage up and down to regulate the input voltage. The switch will be driven by a gate driver that is controlled by a microcontroller's pulse width modulation (PWM) outputs. Sensors will be placed throughout the circuit to monitor the current, voltage and temperature, providing information to the inputs of the microcontroller. The pulse width will be controlled by three separate control loops: a fast current loop (once per switch cycle), a slower voltage loop (to allow for minor fluctuations) and an even slower maximum power point tracking (MPPT) loop. The microcontroller will require current and voltage information from different parts of the HM1 for each loop, as well as temperature to ensure a safe derating of the output.

We have designed a sample state diagram that will require testing to ensure the MPPT and battery charging, as well as the various protective circuits all function correctly. We expect Helios Mk-I to have demonstrable hardware by the end of the four-month semester. To ensure proper design of the power supply we will begin by designing a voltage-mode control loop. When this is stable under most conditions we will add the current-mode control loop on top of it; the current-mode loop will ensure quick transient response. After both loops are fully functional the MPPT control-loop will be added on. Due to time constraints it is unreasonable to assume the current-mode and MPPT loop will be fully functional by the end of the semester so we will attempt to find conditions to demonstrate how we could utilize sensor information to implement them.

Also note that Helios Mk-I and HM1 is used interchangeably throughout this document.

Table of Contents

List of Figures

List of Tables

Acronyms

A	amperes
A/D	analog-to-digital
ADC	analog-to-digital converter
AC	alternating current
CSA	Canadian Standards Association
DC	direct current
EMI	electromagnetic interference
ESR	equivalent series resistance
H	Henry
HM1	Helios Mk-I
Hz	Hertz
I	Current
IC	integrated circuit
I/O	input/output
k	kilo
LED	light-emitting diode
m	milli
MPPT	Maximum Power Point Tracking
NiCd	Nickel Cadmium
P	power
PbA	Lead Acid
PCB	printed circuit board
PIC	peripheral interface controller
PWM	pulse-width modulated
OCV	Open Circuit Voltage
RISC	Reduced Instruction Set Computing
RMS	Root Mean Square
RoHS	Restriction of Hazardous Substances Directive
SCC	Short Circuit Current
SMPS	Switched Mode Power Supply
SOC	State of Charge
TVS	Transient Voltage Suppression
u	micro
UART	Universal Asynchronous Receiver Transmitter
V	voltage
Vds	Drain Voltage minus Source Voltage
Vgs	Gate Voltage minus Source Voltage
W	watts
WEEE	Waste electrical and Electronic equipment Directive

Glossary

Op-Amp	Operational Amplifier

1 Introduction

The Helios Mk-I (HM1) is a solar panel battery charger that implements a maximum power point tracking (MPPT) algorithm to optimize power transfer. It will have a maximum output voltage of 20 V and maximum output current of 20 A. The specification for the HM1 was provided by Analytic Systems and was originally provided to them by a potential customer. The HM1 is a standalone product that will be versatile enough to be placed into any 12V (≈17V @ Max Power) Solar Panel system and potentially any 24V (≈35.5V @ Max Power) system (24V systems will be hard to achieve due to OCV's of 24V solar panels in excess of 42V [1]) to charge 12V PbA and 16V NiCd batteries. With a few modifications to the charging algorithm any battery that reaches 100% SOC under 20V should be usable with the HM1. The HM1 allows dynamic loads to be powered in parallel with the charging battery. The HM1 uses a cascaded buck boost converter to regulate the voltages providing an output voltage referenced to the input ground (the output is neither inverted nor isolated). Our goal for the HM1 is to provide energy for the future that is renewable, innovative, practical and sustainable. This design specification describes the technical details for the design of each block of the HM1 battery charger.

1.1 Scope

This document specifies the design of the HM1 battery charger and explains how the design meets the functional requirements as described in the Function Specification for a *Solar Power Battery Charger* [2]. This document will have all the requirements for design specifications and the functional requirements that will be met depending on the time restraint and unforeseen problems. Furthermore, the appendices include design layouts, and a state diagram to help implement proper designs of the HM1 battery charger.

1.2 Intended Audience

The design specification is intended for use by all team members of Solar Solutions and Analytic Systems. Moreover it is expected that each team member refer to the design specification throughout different phases of development to ensure overall design goals are met. Furthermore, this document will serve to assess the prototype after production by comparing the achieved functionality versus targeted functionality. Lastly, this document shall aid in testing HM1 as engineers will refer to it to design the test plan.

2 System Design

The HM1 consists of several different subsystems that produce the desired functionality. Many of these systems require sophisticated logic to perform so most of the control is being implemented by a microcontroller. The subsystems include:

- Input Protection
- Buck-Boost Power Stage

- Auxiliary Power
- Voltage Sensing
- Current Sensing
- Temperature Sensing
- RS-232
- LED Indicators
- Output Protection
- Microcontroller
- Aluminum Chassis

By the end of this document each block of the system will be fully specified.

Please note that specific batteries and solar panels are not part of the specification but will be customizable depending on customer needs. For testing we have access to a variety of PbA batteries and a single 70W Siemens 12V solar panel.

2.1 Mechanical Design

This section shall provide an in-depth overview of the mechanical design and fully specify size requirements for the HM1.

As no size requirement was imposed we arbitrarily determined the HM1 we decided to use a standard Analytic Systems extrusion. This provided a width for the PCB of 6.15in. Based on a quick review of similar devices we arbitrarily assigned a temporary length of 11in to the PCB and 12in to the enclosure to provide space for wiring and assembly. We believe the end product will require a significantly shorter chassis as Analytic Systems' current line of 300W DC-DC converters are 12in with isolated outputs [3].
Figure 1 provides an overview of the intended enclosure with the sample length. For more views and low level design please refer to Appendix A: Mechanical Drawings.

Figure 1: Top right angle view of enclosure for Helios Mk-I

The front and back panels will have accessible components for the user. The fins act as a heat sink to cool components on PCB.
Table 1 summarizes a list of components

Table 1: List of components on front/back panel of Helios Mk-I

Front Panel	Quantity	Back Panel	Quantity
On/Off Switch	1	Battery +/-	1
RS232 Input (DB9 Serial)	1	Load +/-	1
Battery Temperature Sensor (CAT3e)	1	Panel +/-	4
LED	5	LED	6

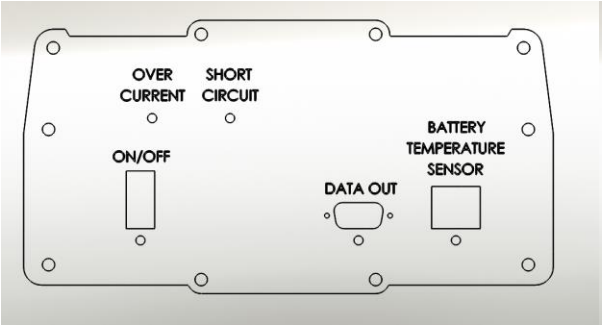


Figure 2: Front Panel of enclosure for Helios Mk-I

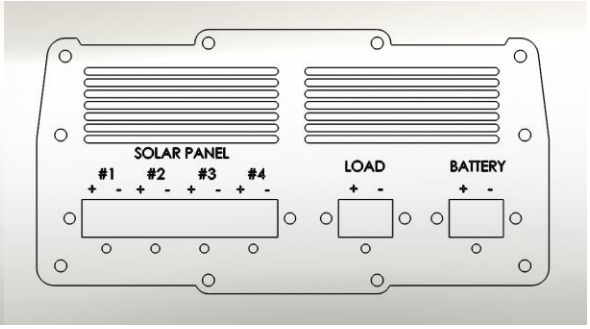


Figure 3: Back Panel of enclosure for Helios Mk-I

The front panel in Figure 2 contains inputs that users use such as the on/off switch, data out, and temperature sensor input. The data out will contain a RS-232 D9 Female connection for users to connect a male D9 cable. This will allow users to access the microcontroller whether it is to read data, change firmware, or check efficiency. A battery temperature sensor will be provided with each battery charger. It will utilize CAT3e to transmit the temperature to the battery. This sensor is a standard Analytic Systems product.

The back panel in Figure 3 contains vents that act as an additional cooling mechanism in addition to the heat sinking action of the chassis. Below the vents are +/- terminal blocks for the solar panel, load, and battery.

In additional to the chassis there are screw holes for components to mount onto and for the panels to mount onto the chassis and also the LEDs.

The uses of the LEDs are as follows:

- Determine if Helios Mk-I is on
- Show successful connection with RS23
- Battery Temperature Sensor connected and working
- Warning for overheating
- Battery connected and working
- Load connected and working
- Panel connected and working

There is no display or digital user interface for the Helios Mk-I so it is crucial to have system of feedbacks that user can use to easily determine the current operation of the device.

2.2 Electronics Design Principles

Methods used to design each electronics subsystem are described in this section.

2.2.1 Part Selection

Various criteria were used to determine what components to use for HM1. These criteria incorporate the following:

1. Cost effectiveness
2. Adherences to the cradle to cradle
3. Minimizes noise
4. Components that function during extreme weather conditions
5. Meets system timing criteria
6. Low quiescent currents and/or the ability to disable the part
7. Allows for rapid design (ensuring a demonstrable product by mid-April)

The HM1 was designed to be as cost effective as possible and components were chosen to adhere to the cradle to cradle concept due to group's belief in minimizing carbon foot prints. More importantly, because components that make up HM1 can produce electromagnetic interference, it is essential that this is taken into consideration when selecting components. It is anticipated that HM1 will be used in remote locations with unpredictable weather conditions therefore wide operating ranges are very important. Although we would like to adhere to the previous criteria we also need to have a prototype. SMPS's, especially one utilizing an MPPT algorithm, require fast transient response times so components will be selected to ensure stability. When there is no solar power available it is advantageous for a battery charger to run on a low standby current, Analytic Systems has asked for 1mA RMS. Since we have a significant budget and limited time some of these constraints may be overlooked.

2.2.2 Noise

Noise can arise from components that make up a battery charger such as inductors, MOSFETs and rectification diodes (or synchronous rectification MOSFETs). One of the most noise polluting sections of the converter is the switching components because when DC from the panels is chopped into square waves the parasitic capacitances and inductances in circuit resonate and generate high frequency harmonic. These oscillations can disturb the control loop when sensor data is affected in addition to generating EMI that can interfere with nearby electronic systems. Some methods that will be used to reduce the effect of noise are:

- Snubber circuits
- Filters
- Common mode chokes
- Shielding of inductor
- Intuitive layout of PCB
- Component selection

Once again, for our current design, not all methods will be used. This list merely ensures EMI will not be ignored in future design iterations.

2.2.3 Safety

The safety of a user or field technician is of utmost importance to Solar Solutions. To ensure no one is injured, and no equipment is damaged by the HM1 we have taken the time to design sophisticated protection circuitry.

If a solar panel is connected in reverse there is a circuit to prevent the reverse voltage from destroying the converter; in theory the reverse connection will cause no sudden sparks because all current will be blocked. Additionally the input is fused, and has a clamping diode to protect the HM1 from overvoltage events. Unfortunately this will disable the device.

The output of the charger has two separate connections: one for the battery and one for the load. They are protected by similar circuitry. When a battery is connected it will bypass the protection circuitry if the converter is off (no panel voltage); the current design has the load immediately connected to the battery but this will be changed. The battery or load can be disconnected by the microcontroller anytime; additionally both outputs are fused with a clamping diode for worse case scenarios.
The current protection circuitry is attached in Appendix C: Circuits thus far (not complete).

2.3 High-Level System

This section provides a high-level overview of the entire system and describes the placement of components on the battery charger

A block diagram is displayed in Figure 4. It shows the relationships between the subsystems and what the inputs and outputs are.

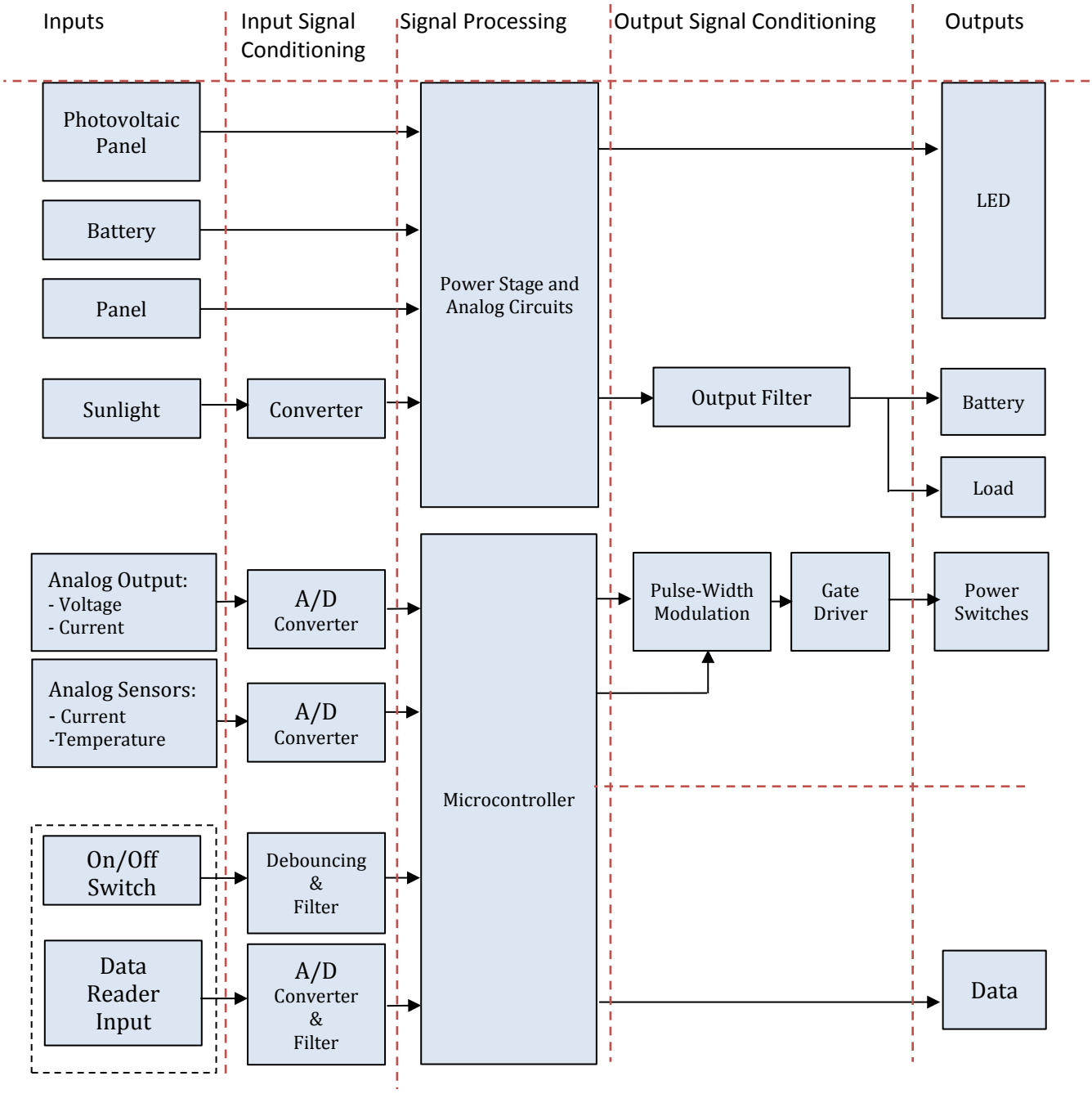


Figure 4: System Block Diagram

System inputs include the input button, which is a user button for the on and off switch. Data reader inputs include a temperature reader and data statistics reader. Other inputs include the panel, temperature, voltage and current sensors, battery, load, overvoltage, overcurrent.

The signal processing stage consists of the microcontroller and hardware circuits. A MPPT algorithm will be incorporated in the microcontroller to optimize power transfer. A/D conversion stages will allow the microcontroller to interpret the data. The protection circuits are activated on certain conditions to protect the device as a whole.

The output filter includes the system receiving the processed output signals and interpreting the data. Pulse-width modulation will be sent to the gate drivers, which will drive the switches to run the converter. The LEDs act as an output to determine if the devices are working properly. Finally the microcontroller outputs data to external devices that are connected to HM1.

2.4 Sensor Placement and Function

The following types of sensors will be used in the Helios Mk-I battery charger:

- Current sensor
- Voltage sensor
- Temperature sensor

Current will be sensed for two reasons: the first is for the current mode control of the converter, ideally midway through each switching cycle. The second current measurement will be used for data logging of power and ensuring the current being consumed by the battery and the load falls within specified limits.
These have not been picked yet. Difficulties selecting current sensors include:

- Picking a high side sensor that utilizes an auxiliary power supply as the high side voltage will frequently level shift within the Buck-Boost and the sensor may turn on and off sporadically
- Ensuring the rate of measurement can provide a signal that is relevant to the particular switching cycle
- Ensuring a reasonable range of currents can be measured (as low as 250mA to as high as 30A)
- Keeping the ESR of the sensor under 1-2mOhm to reduce power dissipation and increase converter efficiency

Voltage sensors are used to ensure the target voltage is maintained in addition to measuring power for data logging. Currently we intend on using the same op-amp that we would use to amplify the current signal to buffer the voltage signal.

The temperature sensors are used to monitor the main switching MOSFETs, inductor and microcontroller temperatures. We intend on using a LM50C integrated temperature sensor instead of a thermistor to save time- a thermistor requires a look up table to be mapped out (and often found experimentally) and is too large of a time commitment for our project. The LM50C output range is 0.1V to 1.75V with it's output given by the following equation:

$$Vo = \frac{10mV}{^{\circ}\mathrm{C}} + 0.5mV \quad (1)$$

Because temperature changes slowly we are running the output through a cheap rail to rail non-inverting op-amp with a gain of 1.75.

2.5 Power Supply (Buck-Boost Converter)

2.5.1 Introduction

The HM1 is utilizing a non-inverting buck-boost converter. The non-inverting buck-boost was chosen for three reasons:

1) The solar panel may be at a higher voltage then the output voltage- this requires a buck topology
2) The solar panel may be at a lower voltage then the output voltage- this requires a boost topology
3) The design specification required a common ground between the solar panel and the battery- this requires a non-isolated, non-inverting topology

There are three main operating modes for our power stage: buck, boost, and buck-boost. The charger can be operated in any one of these modes because the buck is cascaded with the boost. Ideally the converter will run in buck mode for high input voltages, boost mode for low input voltages, and buck-boost mode when Vin ≈ Vout as both the buck and boost perform poorly in this region. For demonstration purposes we may opt to implement only the buck mode as it will cover most operating modes.
The following equations govern the various operating modes. Vout is the battery charging voltage, Vin is the solar panel voltage and D is the duty cycle:

$$Buck: \frac{Vout}{Vin} = D \tag{2}$$

$$Boost: \frac{Vout}{Vin} = \frac{1}{1-D} \tag{3}$$

$$Buck-Boost: \frac{Vout}{Vin} = \frac{D}{1-D} \tag{4}$$

Our derivation of these formulae can be found in Appendix B: Buck-Boost, Buck, and Boost Duty Cycle Derivations.

2.5.2 Switching Frequency and Gate Drive

We chose a frequency of 65 kHz because it offers a variety of advantages:

1) Analytic Systems has a legacy of designing marine products. Since many marine radios operate in the 100 kHz range it is optimal to avoid 100 kHz as a harmonic of your switching frequency. 65 kHz has a harmonic at 130 kHz, far enough from 100 kHz to ensure no interference.
2) The 50 kHz range of frequencies is easier to switch at because the control loops are less constrained than higher frequencies.
3) The lower the switching frequency used the greater the inductance and capacitance in your circuit needs to be. For a 300W battery charger, approximately 50 kHz provides a sufficiently high frequency to avoid gigantic capacitance and inductance values.

4) Higher frequencies can cause larger switching losses. However 65 kHz is sufficiently low to avoid this. A diagram and discussion of switching losses can be found in Appendix D.

For both low and high side switches, we have chosen to use isolated DC-DC converters to provide a Vgs of 12V. For the high side, a use of an isolated DC-DC converter is rational because it is a quick solution to providing a sufficient gate voltage to a gate drive chip.

We have chosen the PSD1-S5-S12-M-TR DC/DC 12V as our isolated power supply; it provides an isolated 12V and 84mA with an input of 5V.

Other methods include a bootstrap capacitor or a charge pump. Both have difficulties supporting the 100% duty cycle required to bypass the buck or boost stages. These options were not available to us regardless of the stated difficulties due to time constraints (there is no extra time to debug a circuit as important as the gate drive).

The isolated DC-DC converter was selected for the low side gate drive as well to reduce our part count. It is an abnormal choice but it meets all of our needs and eliminates the need to source another component. In production, each component needs to be loaded into a pick and place machine; our choice eliminates one component.

The gate drive circuitry can be found in Appendix C: Circuits thus far (not complete).

2.5.3 Inductor and Capacitor Selection

To select an inductor we ran a simulator, Power 4-5-6 for all our operating conditions. The software provided a working value of 48uH. When designing the 48uH inductor we followed several engineering rules of thumb to ensure the core never goes higher than a specified value of Tesla's and thus never saturates. Core saturation is a major cause of SMPS failures.

Capacitance values and ESR compensation were handled by additional simulation and engineering rules of thumb. ESR is a parasitic value in an electrolytic capacitor that causes the capacitor to dissipate power when an AC signal is passed through it. The ripple current of a SMPS is an AC signal that causes the capacitors to heat up thus introducing losses and causing a potential failure mode. To avoid problems with capacitors heating up it is advisable to add ceramic capacitors in parallel which have a low ESR.

2.6 Real-Time Controller

The following sections introduce the structure of the firmware and the selection process for the microcontroller.

2.6.1 Introduction to the Overlaying Structure and Operation

The fundamental functionalities of the firmware are structured into three layers. The quickest layer is on the bottom while the fastest is on top. The MPPT is the slowest control loop and will likely be run every two to ten cycles depending on experimental results. The voltage loop is the next slowest control loop and ensures the voltage does not exceed, or sink below the target

voltage. The voltage-mode loop will be run every two to five cycles. The fastest control loop is the current-mode control. We will be implementing an average current loop as opposed to a peak current mode loop because the average mode is versatile enough for our needs in addition to being simpler to implement. The current-loop will respond in a single cycle.

The supporting functionality requirements of the controller are logging of data and low voltage disconnect of the battery from the load.

2.6.2 Microcontroller Selection

Due to time constraints we have selected a microcontroller with internal flash memory to ease the storing of charging data. The microcontroller also has several PWM outputs, ADC inputs, and UARTs that allow it to be versatile and functional. The microcontroller itself is a dsPIC33FJ64GS606; this is the microcontroller that Analytic Systems recently decided to integrate into several battery chargers and it meets all of our requirements.

2.6.3 Real-Time Hard Deadlines to Ensure Battery and Component Protection

The first design requirement is always the general safety of people, safety of the environment, and safety of the equipment—this section discusses the firmware role in safe performance of the equipment and the prolonging of battery life. The hardware ensures many safety measures that are discussed in previous sections of design; however, the firmware determines the operational lifetime and performance of the components. The following is a list of critical deadlines, and the design choices associated with meeting each of them.

- Battery Charge Voltage

  The output voltage needs to be extremely accurate when in trickle charge. Having PID control operate at every PWM cycle ensures minimal error from the desired output voltage. A high speed analog comparator will be used to trigger reduction of voltage if necessary.

- Maximum Output Charging Current

  A threshold will be established for the maximum output charging current, which will be monitored by a high speed analog comparator. The built in voltage reference to the microcontroller will be scaled and used for comparison with the measured current. The comparison will be implemented with the high speed analog comparator, which will trigger a reduction in current within the preceding duty cycle.

Due to many transients involved with switching, blanking periods may be used where momentary large currents are ignored by all the control circuitry. This will only be done if they are determined to be insignificant, since every underdamped switching system has some level of ringing associated with its second order response.

2.6.4 Maximum Power Point Tracking Design and Algorithm

To better explain control and design, we will examine how different switching parameters affect one another. The duty cycle (D), frequency (f), input voltage (Vsol) input current (Isol), output voltage of the buck-boost (Vout) and impedance of the solar panel and buck-boost (Zsol, Zbuck). For starters, what is Zsol and why does it matter? From the V-I characteristics of the solar panel, you can derive the following Zsol versus Vsol characteristic of Figure 5. By varying the input impedance we can accommodate for MPPT. The inductor provides the strongest source of impedance, which is proportional to the switching frequency of 65 KHz.

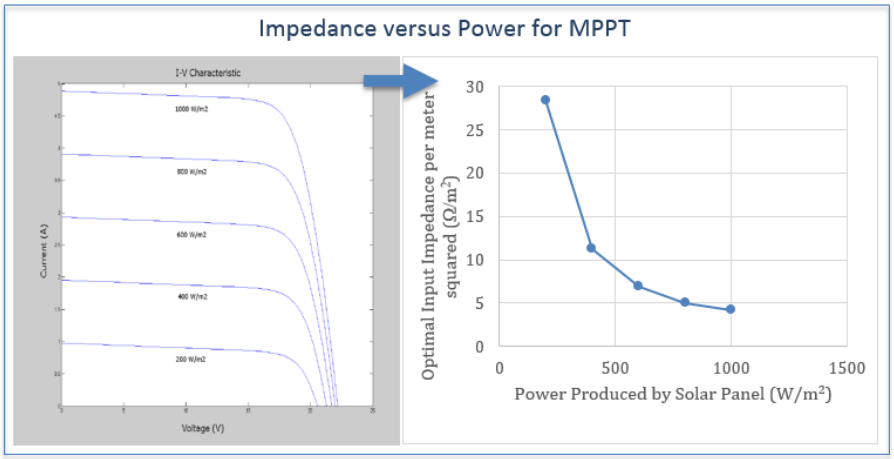


Figure 5: Decreasing impedance trend for increases in power when impedance matching the Solar Panel [4].

For general control, firmware needs to be aware of the following relationships between the parameters. These only apply for the common ranges of operation, and exclude the exceptions of the duty cycle (D) being close to zero or one. It is invalid for the microcontroller to have a D equal to one or zero, but only within that range.

Table 2: Control Parameter Relationships

Relationship	Sensitivity	Reasoning/Importance
Switching frequency proportional to input impedance	Low	Useful to know, however will not be modified due to ER
Voltage gain proportional to D	Medium	Need to establish correct charging voltage
Output voltage proportional to D Output current proportional to D	Medium High	For modifying output voltage and current
Input current proportional to D Input impedance inversely proportional to D Input voltage inversely proportional to D	High Medium Medium	For modifying input voltage, current, and impedance for MPPT implementation.

Since the power provided by a solar-panel is not rapidly changing, the MPPT algorithm has soft timing constraints. It is implemented in the main loop of the firmware, and it is implemented in C as opposed to assembly (as opposed to the current-loop which will need to be in assembly),

and it is continuously interrupted by more urgent deadlines. The MPPT algorithm to be implemented is in Figure 6. The target voltage itself is achieved in a different file using PID control.

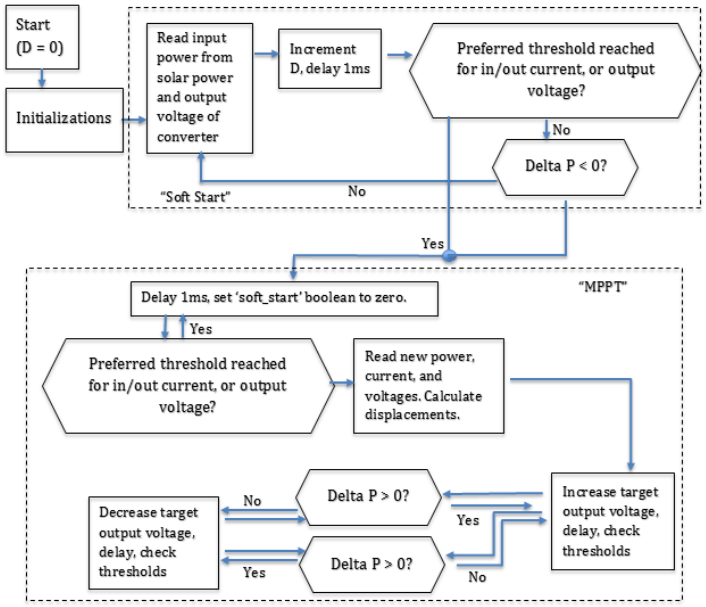


Figure 6: MPPT Algorithm Implementation in Main.c

2.6.5 Overall Functional Design of Firmware

Real-time constraints determine the underlying structure of firmware. The switching frequency is 65 kHz, which is the fundamental starting point for discussing all real-time constraints. PID control is to be completed following the settling of transients that precede the PWM-high rising edge (this is for the ON stage of buck-boost), or the falling edge of PWM-low falling edge. It is to be completed exactly one half-way through the duty cycle, which allows for a reading of the average voltages and currents within that cycle. All instructions are single-cycle since PIC uses a RISC architecture. Exceptions are conditional branch statements and instructions executed on the program counter, which are two cycles. Each single-cycle is four clock cycles. If we run the clock frequency at 40 MHz, we have time to complete 153 instructions within the 15.4 uS period. These are important figures for debugging and designing the firmware. If we have trouble, we can do PID control for every second or third cycle, giving us plenty of extra time (we lose transient response performance if we do this). We cannot have the PID consume more than 70% of the computational load, since the processor still has more to complete.

To increase speed, the power calculation may be completed in hardware with an analog multiplier, and then sampled with an ADC pin by the controller. Hardware manages the charging of the battery, so long as the output voltage is significantly high. The following is the overall resulting architecture of the firmware.

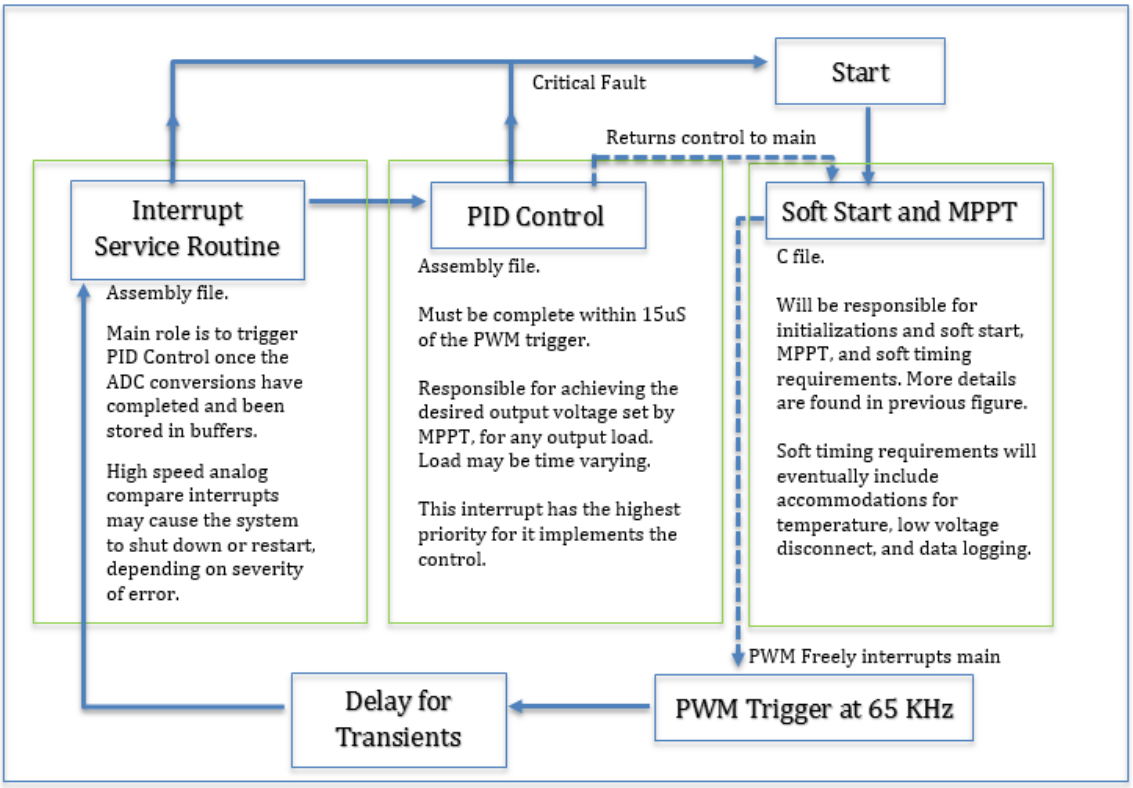


Figure 7 Overall structure, timing, and interrupt calls relating to firmware.

Why is this so difficult? Programming in RISC assembly language is incredibly tedious, and debugging such a project is incredibly challenging.

2.6.6 List of Registers Accessed by Each Function

Registers determine the implemented functionality of the microcontroller. To prevent bugs, defining which roles of the registers to be used, along with when they will be modified, allows for easy understanding of the code. Refer to Table 3 in Appendix E: Microcontroller Registers for the details.

3 System Test Plan

The components will be tested for their safety, reliability, efficiency, and correctness of numerical values as stated on datasheets. The more important components shall warrant a more intense testing.

Once assembled, point-to-point testing will be conducted on the prototype to ensure expected values are achieved throughout the circuit. Further testing on parts includes the following.

- Inductor: Efficiency of energy conversion
- Auxiliary Power Supplies: Ensure it supplies enough power to the active components
- Current Sensors: Sensed current is accurate with little variance

- TVS: Correct break down voltages
- Fuse: Fuse will open during over currents and will not have false triggers
- Crowbar: Crowbar will activate upon overvoltage and will not have false triggers
- Microcontroller: Fully operational

Because of the harsh climate in British Columbia, temperature testing is important. The PCB will be tested in a temperature chamber; efficiency of operation throughout the required specified operating region shall be tested. EMI levels will also be tested in an EMI chamber.

By applying different input voltages we will test the MPPT algorithm and observe changes in the Duty Cycle. The algorithm is the key component to the project, as it will dictate the overall efficacy of the device.

Once the device has been thoroughly tested in a lab environment, the device will be placed outdoors and monitored to check for MPPT effectiveness, component temperatures and overall ruggedness. Outdoors testing is slightly more difficult to conduct because of time restrictions. Without testing the system for extended periods of time in typical environments, it is difficult to gauge the true long-term performance of the device.

4 Conclusion

The purpose of the design specification is to provide clear goals for the development of the HM1 as well as to meet the functional specifications. During the development of the product, these design specifications shall be followed as closely as possible. The test plan included shall be followed by the test engineers to use as guideline to prepare for all contingencies. We shall ensure that the end product of HM1 shall have all the functionalities present as described in this specification.

Appendix A: Mechanical Drawings

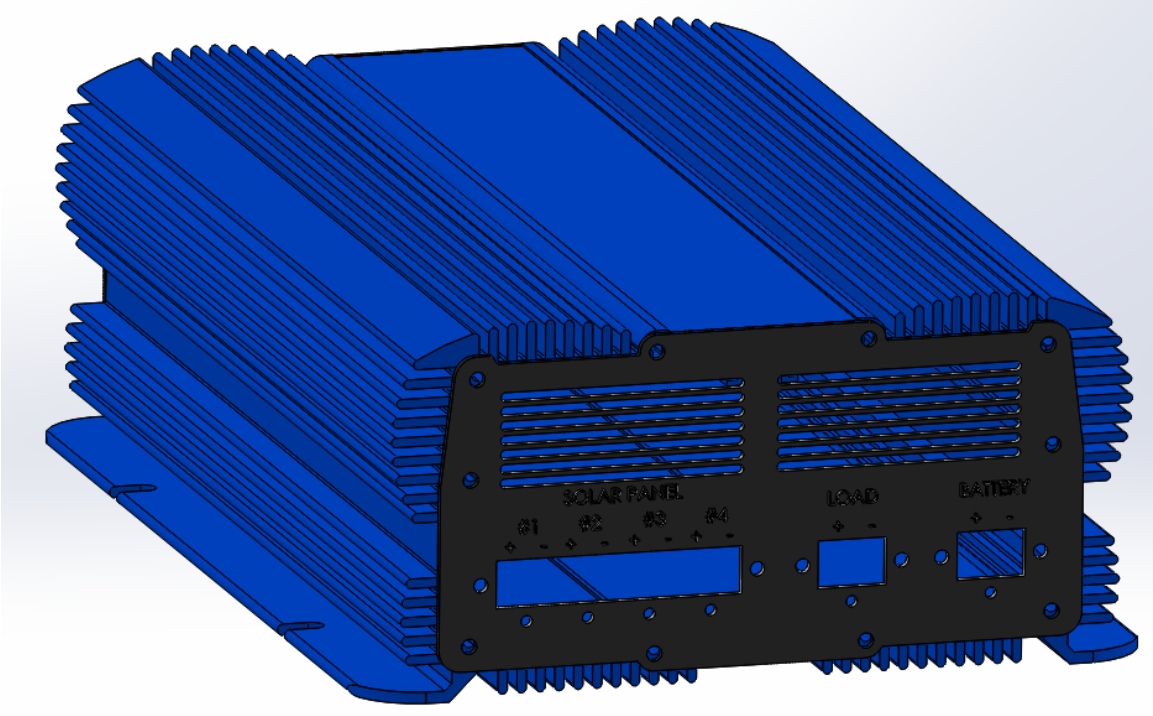


Figure 8: Back left angle view of enclosure for Helios Mk-I

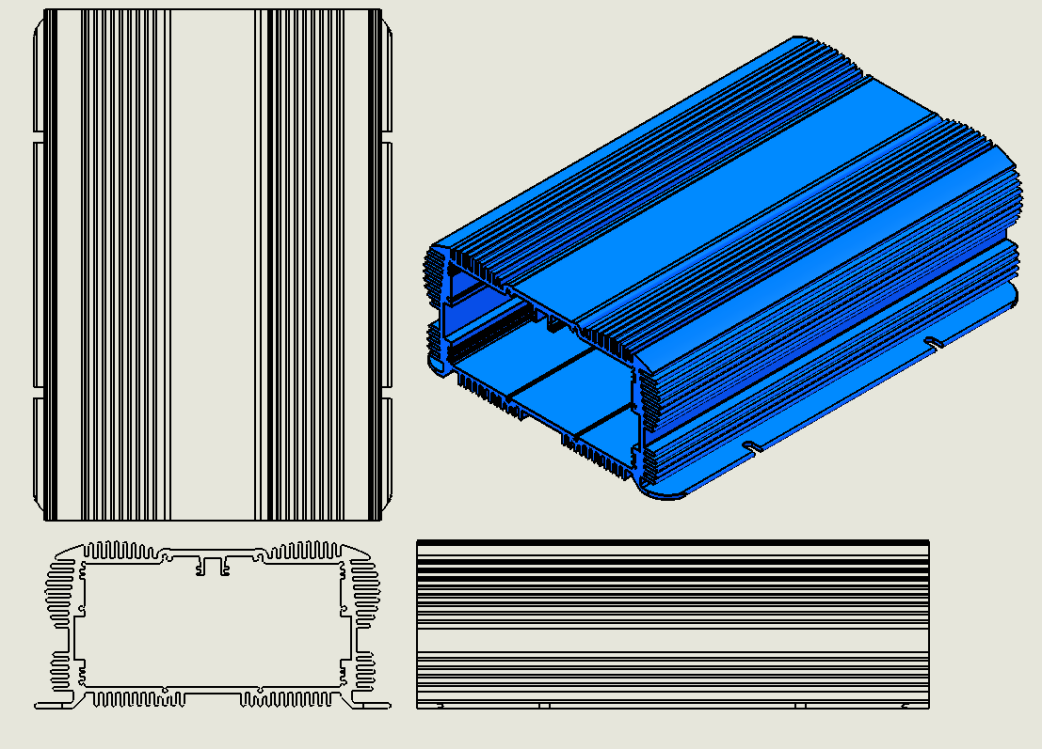


Figure 9: Standard 3 View of Chasity with an isometric view of Helios Mk-I

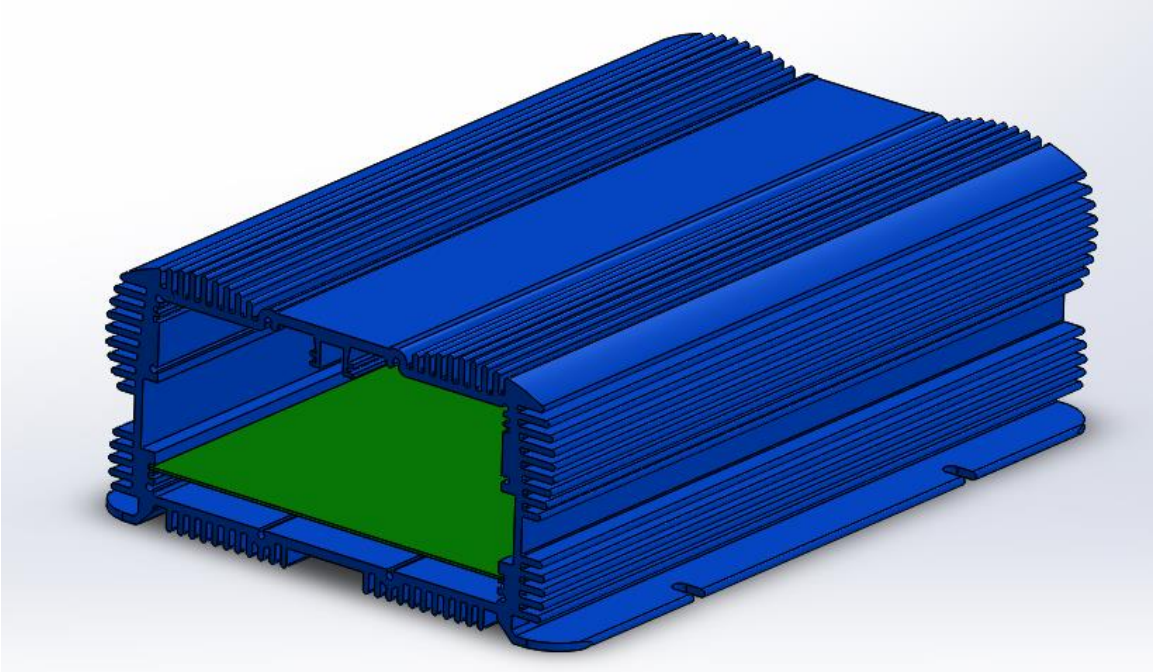


Figure 10: Chasity for Helios Mk-I with PCB slotted inside

Appendix B: Buck-Boost, Buck, and Boost Duty Cycle Derivations

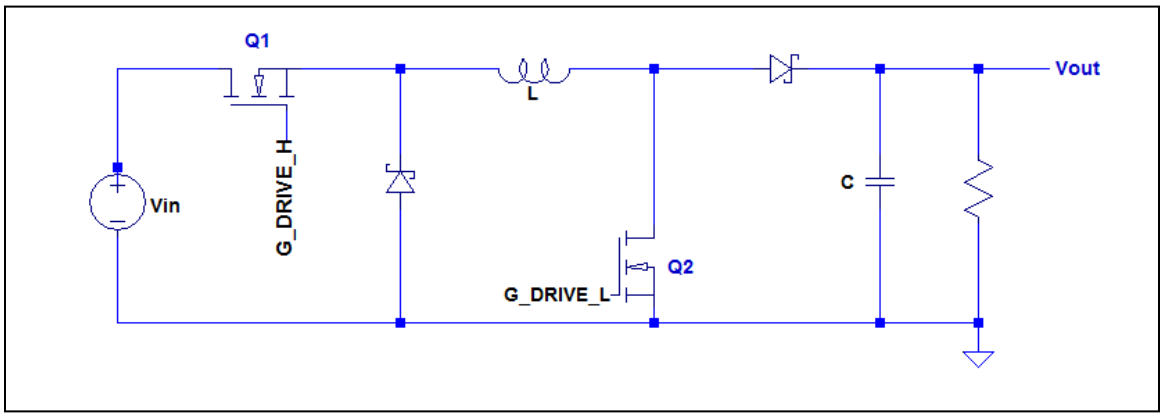


Figure 11: Simplified Buck-Boost circuit

Figure 11 is the stripped down version of the DC/DC topology we have chosen to use. To understand the essence of this particular topology, features such as control or protection has been omitted.

In order to carry out this analysis we must keep in mind a few things. The inductor equation:

$$V = L\frac{di}{dt} \tag{4}$$

dictates that if an average inductor voltage is present, a current ramp will be produced in the inductor given by the equation

$$\frac{V\Delta t}{L} = \Delta I \tag{5}$$

where we have simply replaced $\frac{di}{dt}$ with $\frac{\Delta i}{\Delta t}$ and split the differential equation. This proves that if the voltage balance across the inductor is not maintained, the current in the inductor will quickly reach infinity. In short, in steady state, the average voltage across the inductor must be zero. We can exploit this fact to realize our voltage transfer ratio. To ease analysis, assume that the diodes have zero forward drop.

Furthermore, the chosen converter shall operate in continuous conduction mode. By using this operating mode, the current in the inductor never falls to zero, but ripples around a bias point. To conduct steady-state analysis, the voltages on the output capacitors and currents across inductors can be assumed to be constant during the switching cycles.

Recall that there are three modes of operation that exist: buck, boost, and buck-boost. These three modes pertain to different operating waveforms at the gate of the two MOSFETS in Figure 11. In boost mode, Q1 is permanently turned on while Q2 is modulated. Alternatively, Q2 can be left off and Q1 modulated, producing a buck circuit. The buck-boost mode is achieved when Q1 and Q2 are modulated in unison.

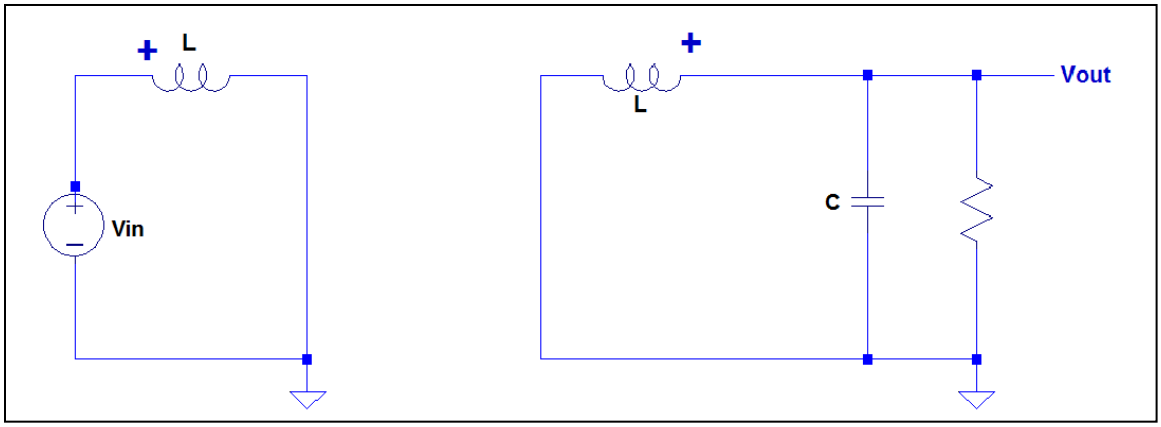


Figure 12: LEFT: Buck-boost during "ON" modulation, RIGHT: Buck-boost during OFF modulation

Figure 12 shows the two modes of operation of the buck-boost converter which exist during the switching cycles. When Q1 and Q2 are on the circuit on the left of Figure 12 is obtained. During this stage the inductor is in series with the input voltage and it's ripple current is increased slightly. The average voltage during the positive portion of the PWM can be computed as DV_{in}, where D is the duty of the PWM. When Q1 and Q2 are off the circuit on the right of Figure 12 is of interest. During this part of the cycle the average voltage across the inductor is now $-V_{out}(1-D)$. The average voltage across the inductor is negative because of voltage polarity reversal across it. As stated earlier, the average voltage across the inductor must equal zero. Thus we have the following equation

$$DV_{in} - V_{out}(1-D) = 0. \tag{5}$$

Solving V_{out}, we find that buck-boost mode gain voltage and D are related by

$$V_{in}\frac{D}{(1-D)} = V_{out} \tag{6}$$

Carrying out similar analysis will give us the buck and boost transfer ratios, will give us equations 5 and 6, respectively.

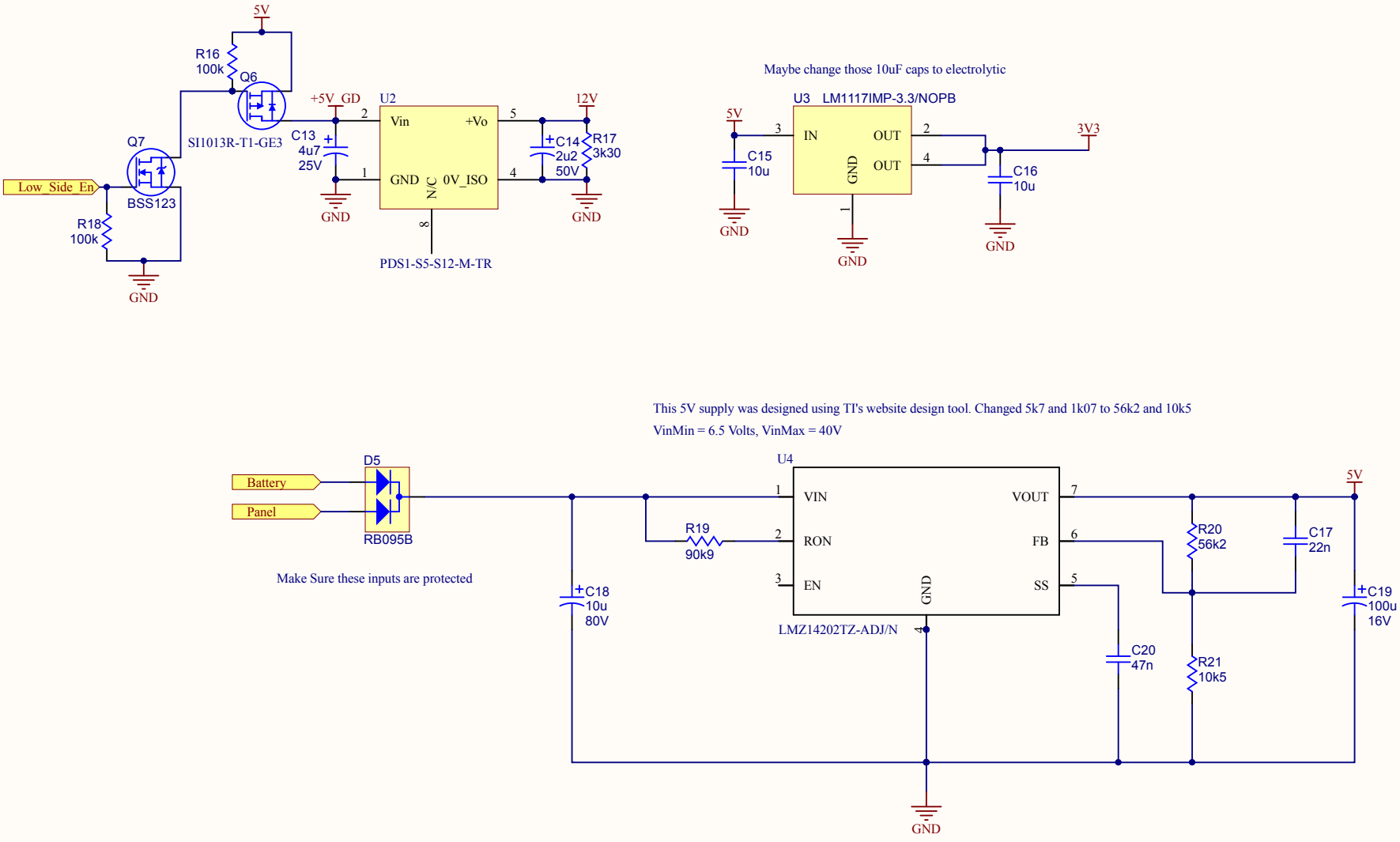
$$V_{in}D = V_{out} \tag{7}$$

$$V_{in}\frac{1}{(1-D)} = V_{out} \tag{8}$$

For our application, V_{out} is connected to a battery and is assumed to be fixed. Hence we can use the exact same equations derived above for the three different converters, but instead of having V_{in} fixed we have V_{out} fixed. Thus we can use the duty cycle to change V_{in}, the voltage across the panels, giving us control to set the maximum power point of the panel where we wish.

Appendix C: Circuits thus far (not complete)

Circuits are located in attached file Helios MkI Rev0-Mar 13.pdf.



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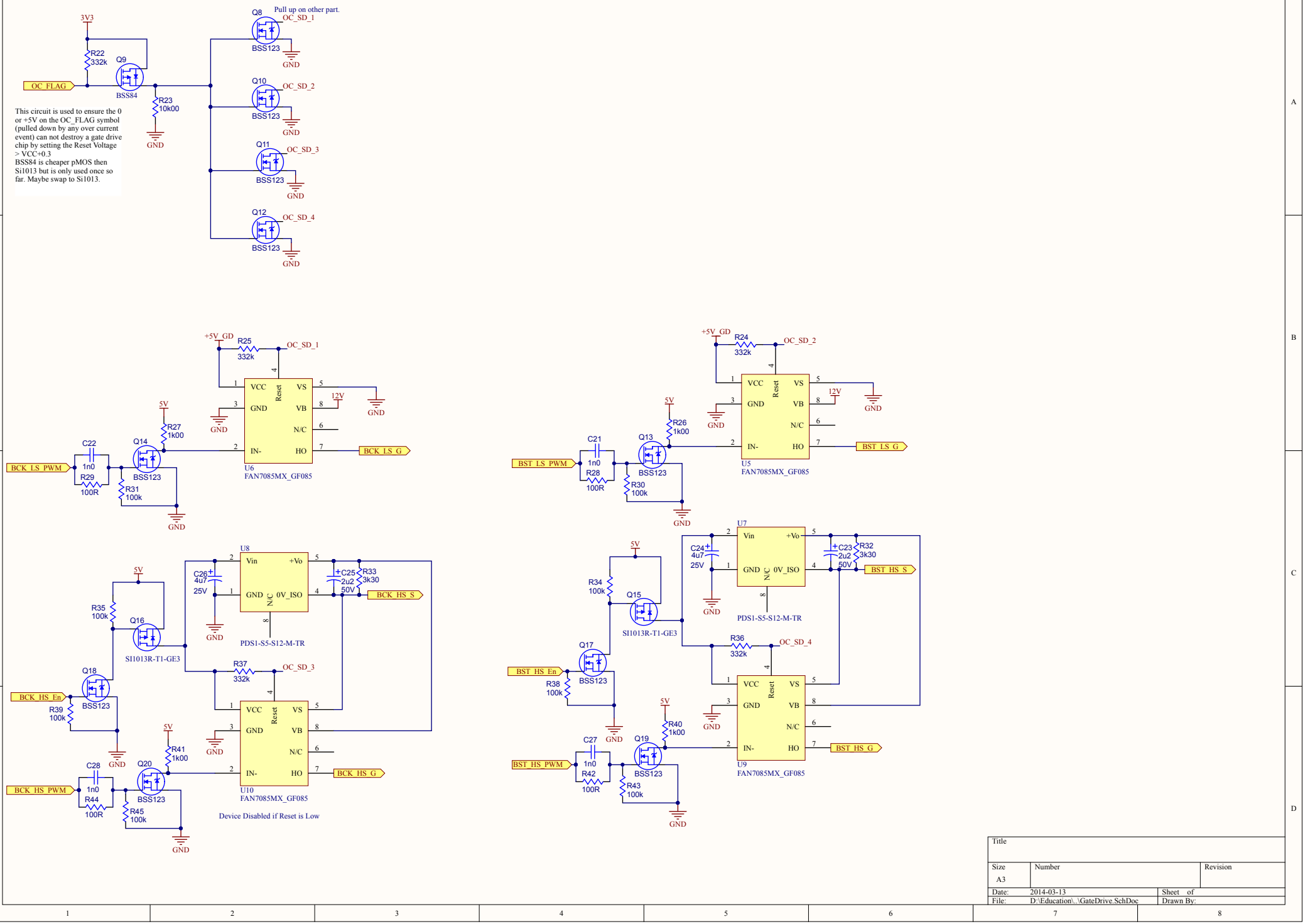
3V3
R22
332k
Q9
BSS84
OC_FLAG
R23
10k00
GND
Pull up on other part.
Q8
OC_SD_1
BSS123
Q10
OC_SD_2
Q11
OC_SD_3
Q12
OC_SD_4
This circuit is used to ensure the 0 or +5V on the OC_FLAG symbol (pulled down by any over current event) can not destroy a gate drive chip by setting the Reset Voltage > VCC+0.3
BSS84 is cheaper pMOS then Si1013 but is only used once so far. Maybe swap to Si1013.
+5V_GD
R25
332k
OC_SD_1
VCC
GND
Reset
VS
VB
N/C
IN-
HO
12V
5V
R27
1k00
C22
1n0
Q14
BCK_LS_PWM
R29
100R
R31
100k
BCK_LS_G
U6
FAN7085MX_GF085
U8
Vin
+Vo
GND
0V_ISO
N/C
C26
4u7
25V
C25
2u2
50V
R33
3k30
BCK_HS_S
PDS1-S5-S12-M-TR
R35
100k
Q16
SI1013R-T1-GE3
R37
332k
OC_SD_3
Q18
BCK_HS_En
R39
100k
R41
1k00
C28
Q20
BCK_HS_PWM
R44
100R
R45
100k
BCK_HS_G
U10
FAN7085MX_GF085
Device Disabled if Reset is Low
R24
332k
OC_SD_2
C21
1n0
Q13
BST_LS_PWM
R28
100R
R26
1k00
R30
100k
BST_LS_G
U5
FAN7085MX_GF085
U7
C24
4u7
25V
C23
2u2
50V
R32
3k30
BST_HS_S
PDS1-S5-S12-M-TR
R34
100k
Q15
SI1013R-T1-GE3
R36
332k
OC_SD_4
Q17
BST_HS_En
R38
100k
R40
1k00
C27
1n0
Q19
BST_HS_PWM
R42
100R
R43
100k
BST_HS_G
U9
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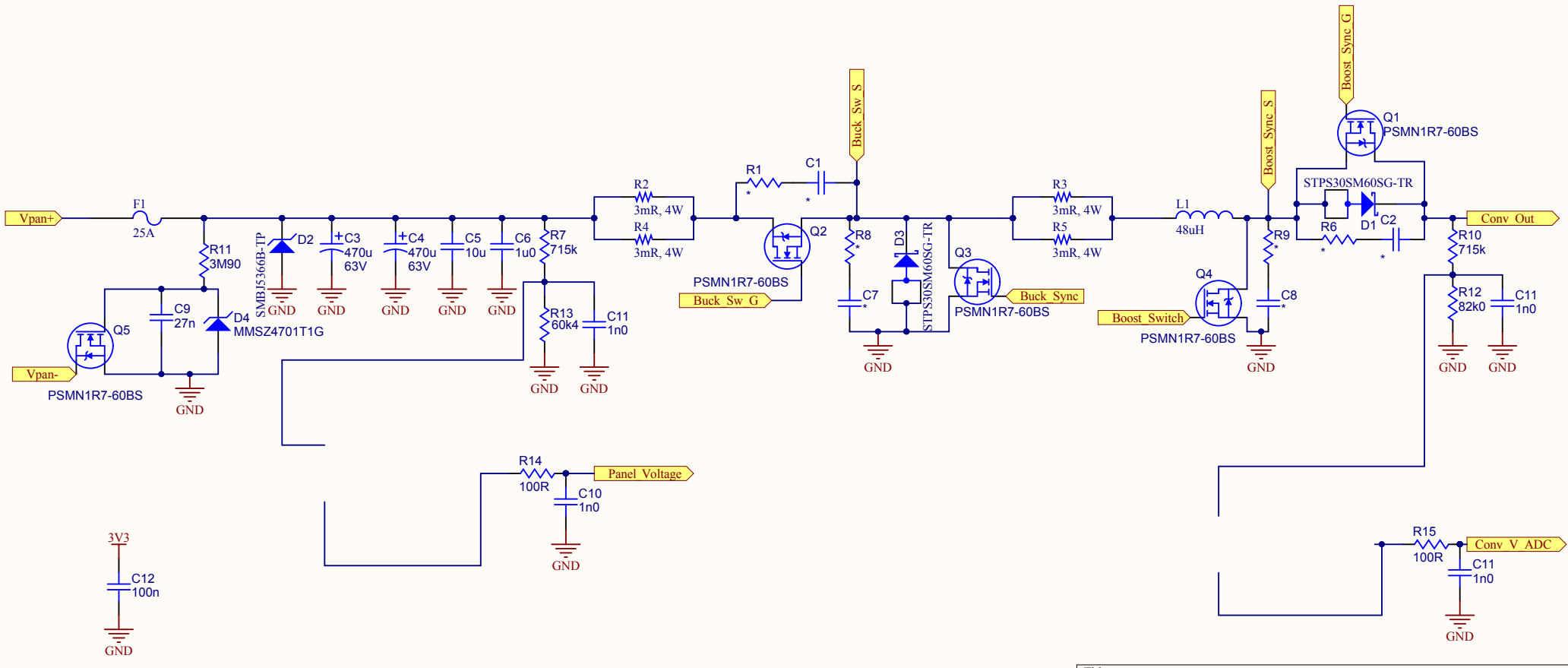
Design Notes:
-Need to replace inductor
-Need Snubber values



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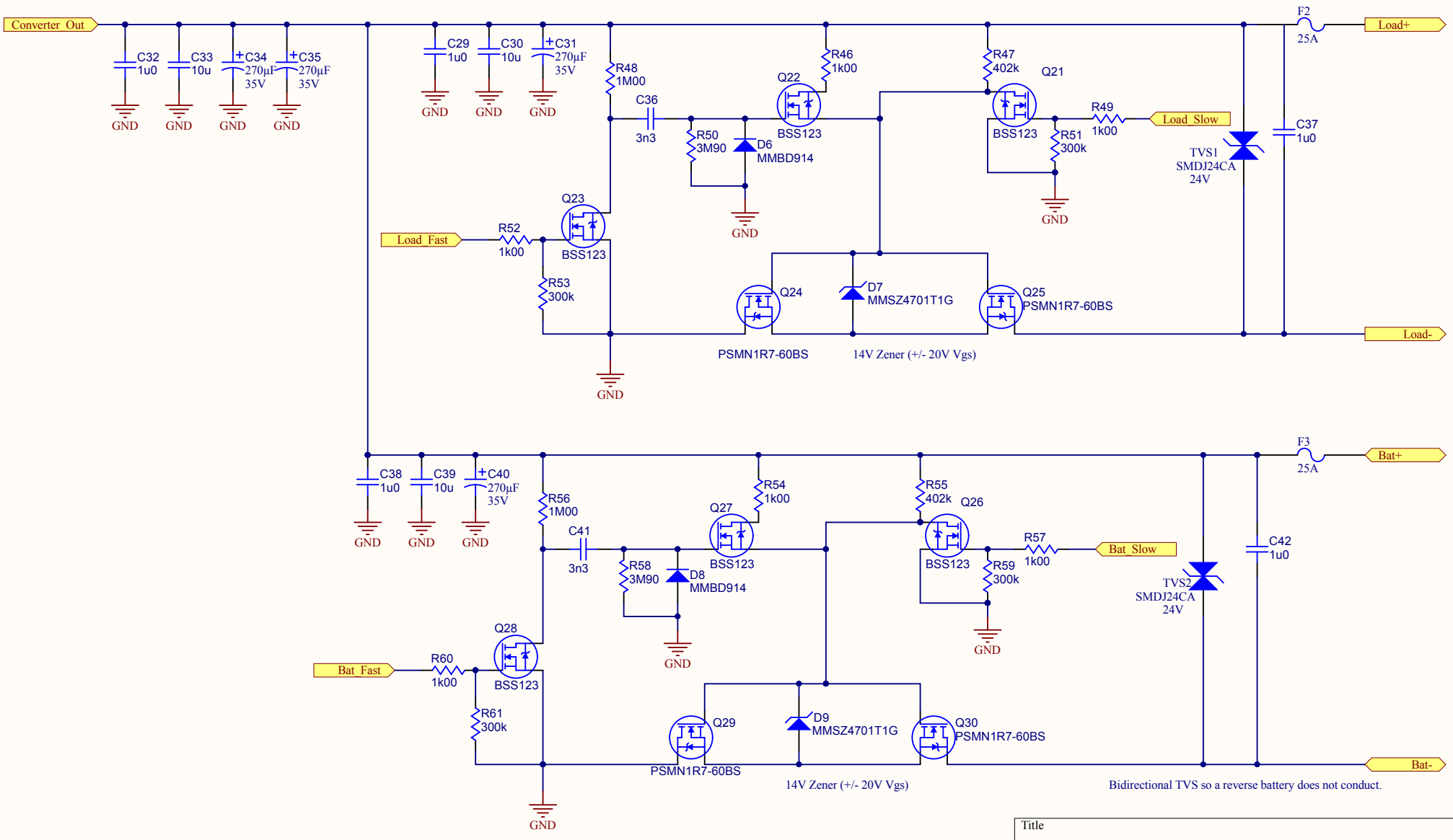

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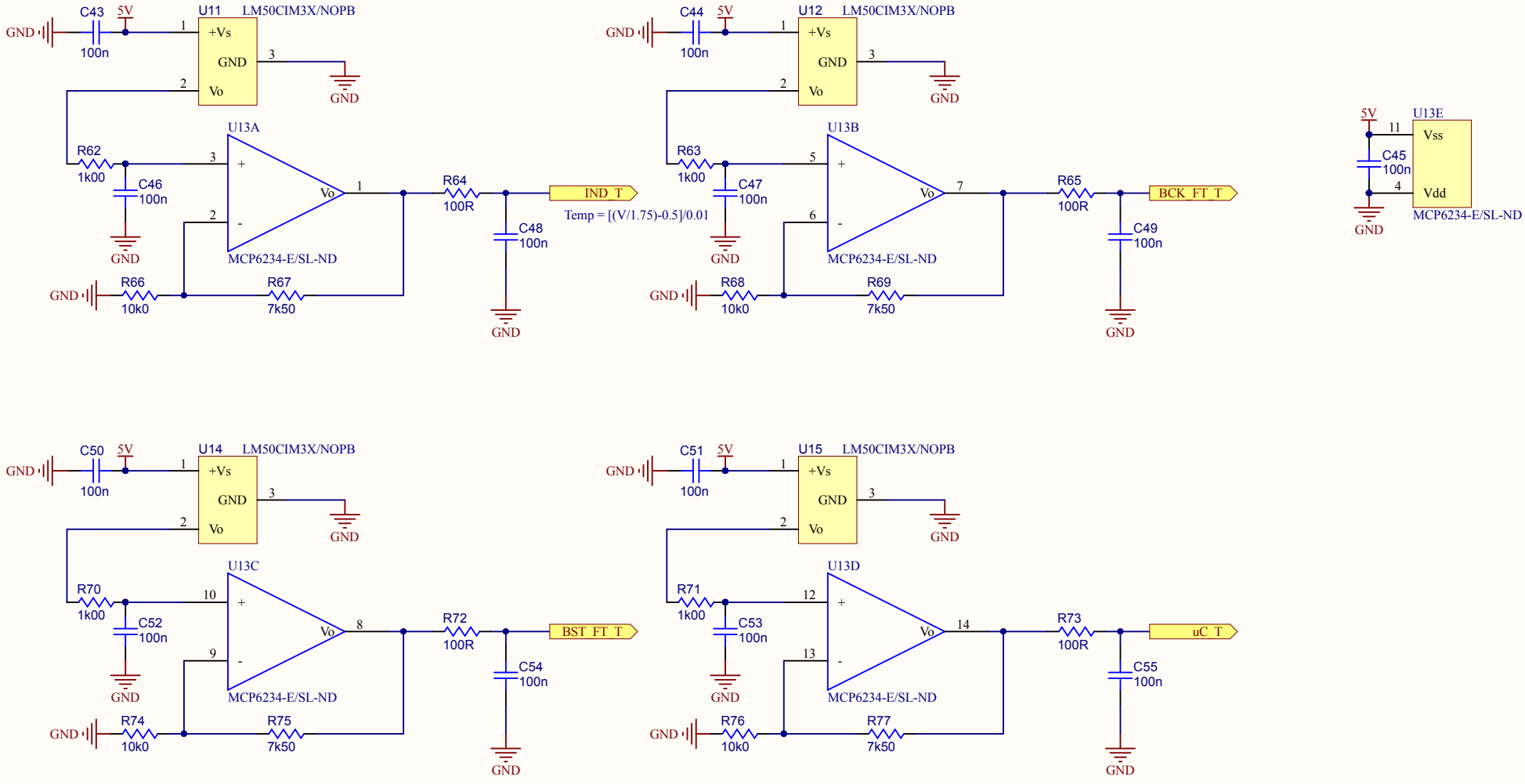
Vo = 10mV/C x Temp (C) + 0.5V
1.750V @ 125C, 0.1V @ -40C



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Appendix D: Switching Losses

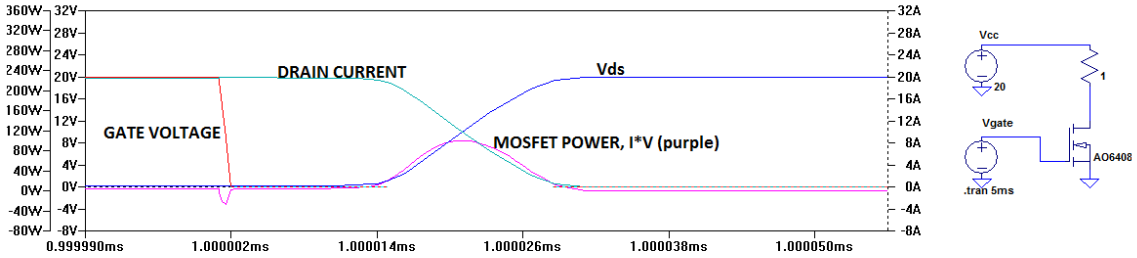

Figure 13: Switching Losses of a A06408 MOSFET

Figure 13 illustrates losses during a switching cycle. The red graph shows the gate voltage of a A06408, a similar MOSFET to one we have chosen, being lowered from 20V to 0V, analogous to ON to OFF cycles of PWM for our case. Notice that the MOSFET current conduction does not change instantaneously, rather it tails off slowly. Moreover, the voltage across the MOSFET does not build up instantaneously but rather it slowly ramps up. As current is ramping down and voltage is ramping to maximum blocking voltage, power loss is being incurred across the MOSFET. This power loss is directly proportional to the switching frequency.

Appendix E: Microcontroller Registers

Table 3: Important registers being utilized in the HM1 project.

Functionality	Important Registers Modified
Clocking	FNOSC: picks microcontroller oscillator. PLLDIV, PLLPOST, PLLPRE: scaling of main clock. ACLKCON: all the registers for configuring the PWM and ADC clocks. REFOCON: all the registers for outputting the clock to a pin.
Input/Output Pin Configuration	ADPCFG: analog inputs. TRISA, TRISB: tristate buffers. LATA, LATB: output latches.
PWM	PTEN: enabling of PWM. PDC1: dynamic duty cycle, as opposed to MDC which won't be used. PCLKDIV: division of clock with the prescaler. PTPER: period of the PWM signal.
ADC	ADON: enabling of ADC. FORM: integer data. ORDER: even channel first. SEQSAMP: simultaneous sampling, very important. ADCS: speed of conversion relative to aux clock. PCFGO: analog mode. ADSTAT: status register to clear when data is ready. ADCPCx: triggering of ADC set on rising edge of every PWM cycle. TRIGx: Timing of the trigger, which will be set at the middle of the duty cycle. STRIGx: secondary trigger. Likely will not be used but must know it is an option. TRIGDIV: set to trigger 1:1 ratio with duty cycle. TRIGSTRT: enables the triggering. DTR1, ALTDTR1: rising and falling dead-time for synchronous switching. IOCONx: pins controlled by PWM, will likely be setting this to active-low. PMOD: complementary PWM. TRGDIV: generate an interrupt each cycle. TRGSTRT: set triggers to start without waiting any more cycles. May later set to delay one cycle. PTEN: enable PWM.
Interrupts	SR: enable priorities. IFSx: interrupt bits. IPCxx: priority. IECx: enabling.
Timer	T1CON: timer configuration and setting of prescaler. PR1: amount of counts before a trigger interrupt. TON: enable timer IFSx: must be cleared in the interrupt for another interrupt to occur.

Works Cited

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