

# "SoundSocket"

## By



April 14, 2014

# Meet the Team

- Josh Ancill
- Andy Cheng
- Daman Dhillon
- Kim Izmaylov
- Laura Wiggins

# Technical Responsibilities

Firmware & Software Engineers:

**Laura Wiggins and Daman Dhillon**

Digital Hardware (FPGA) Engineers:

**Josh Ancill and Andy Cheng**

Analog Electronics Engineer:

**Kim Izmaylov**




# Overview

1. Background & Motivation
  - a. Existing Solutions
  - b. Problem
  - c. Market Analysis
2. System Overview
3. High Level System Design
  - a. System Block Diagram
  - b. Breakdown of Modules
4. Timeline
  - a. Deviations
5. Business Case
  - a. Cost and Funding
  - b. Actual Cost
  - c. Production Case
6. Project Details
  - a. Team Dynamics
  - b. Communication
7. Future Plans
8. Sources
9. Acknowledgements
10. Questions

# Background

- Wireless-centric age
  - WiFi, Bluetooth
- Portability: no wires!
- Recent development: Wireless Audio Streaming

# Existing Solutions

- Bluetooth: 
  - low range
  - expensive for high-end models (\$300~600+)
- WiFi and Bluetooth both use 2.4 GHz 
- Example service: AirPlay 
  - Locked to Apple devices

# Problem: Interference

Spectrum interference is introduced by:

- Microwaves
- Wireless phones
- Routers/WiFi networks

More devices = More interference

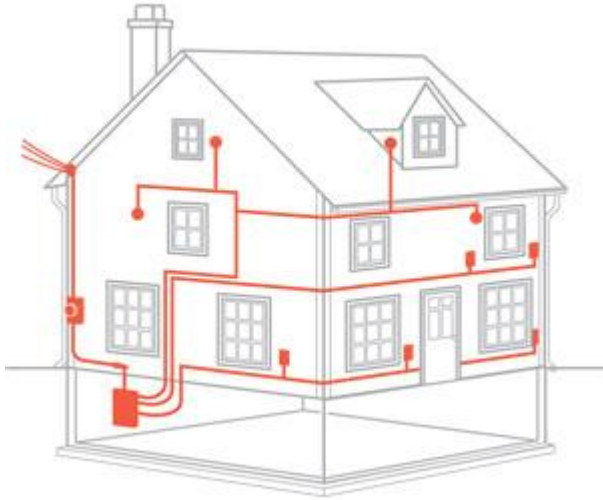
# Problem: Interference

- Oversaturation of the 2.4 Ghz channel
- Dropped signals and distortion



Is there a way to bring the  
best of both worlds?

# Consider a typical home...



- Existing network of copper wiring
- Idea: use this network of wires to transmit audio

# Market Analysis

## Direct Competition:

- IOGEAR Powerline Stereo System (\$740)
- Simple Audio Roomplayer (UK only)

## Indirect (non-powerline):

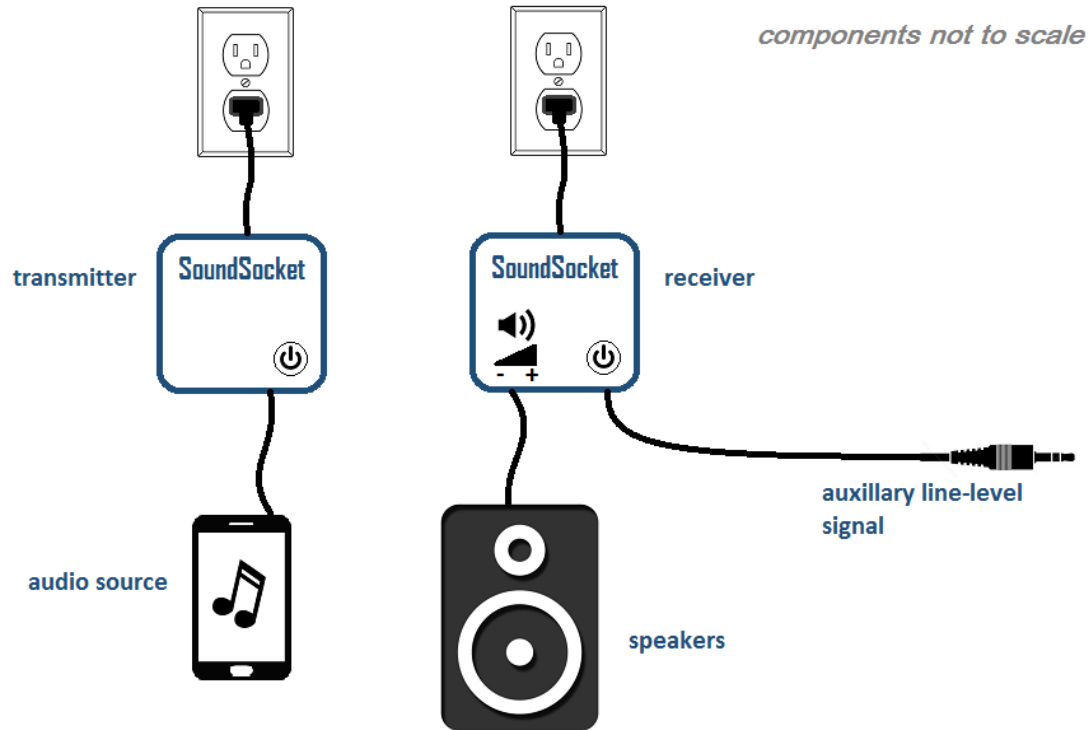
- Apple AirPlay, Bluetooth speakers

# Major Design Obstacle

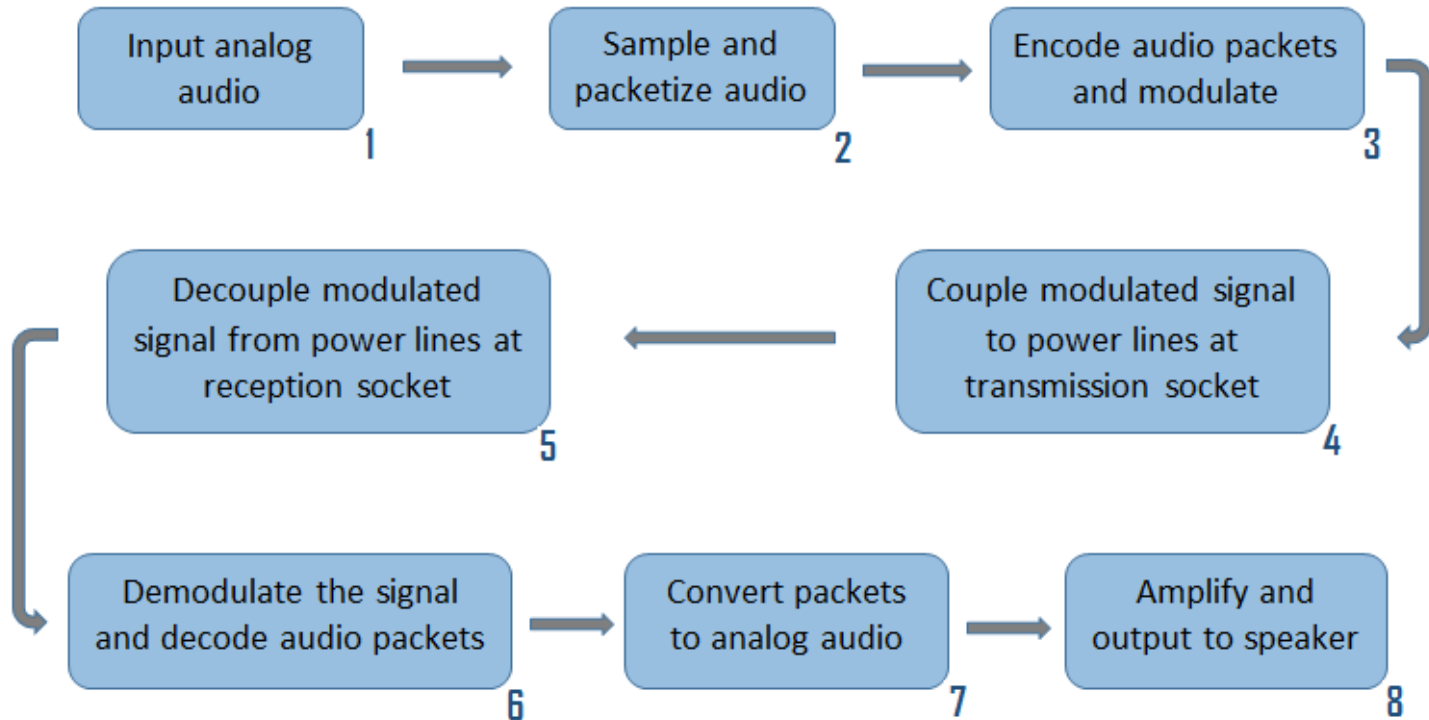
Home wiring:

- Designed for power transmission
  - Lossy wires
  - 120V 60Hz existing signal
- Cause of most design requirements
  - Packetizing
  - Modulation

# Visual System Overview



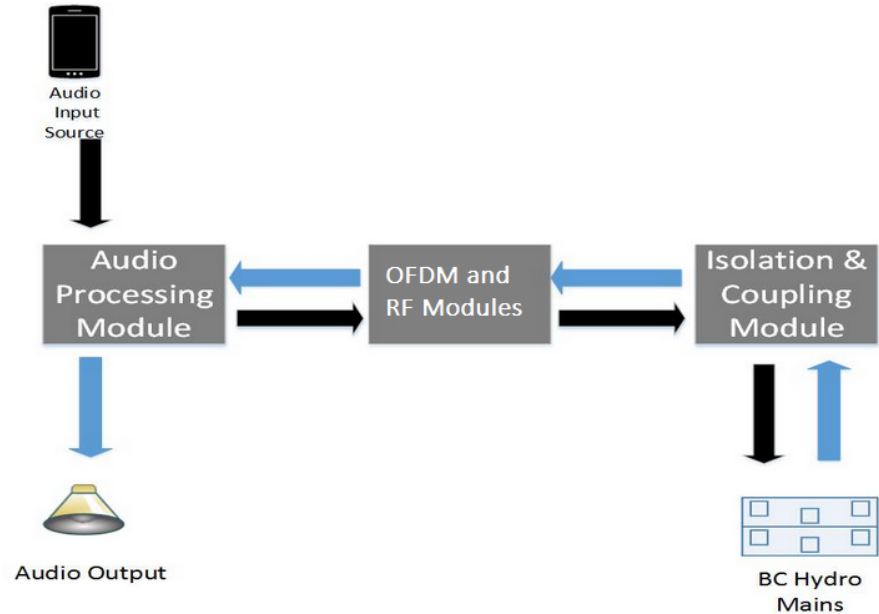
# Functional Block Diagram



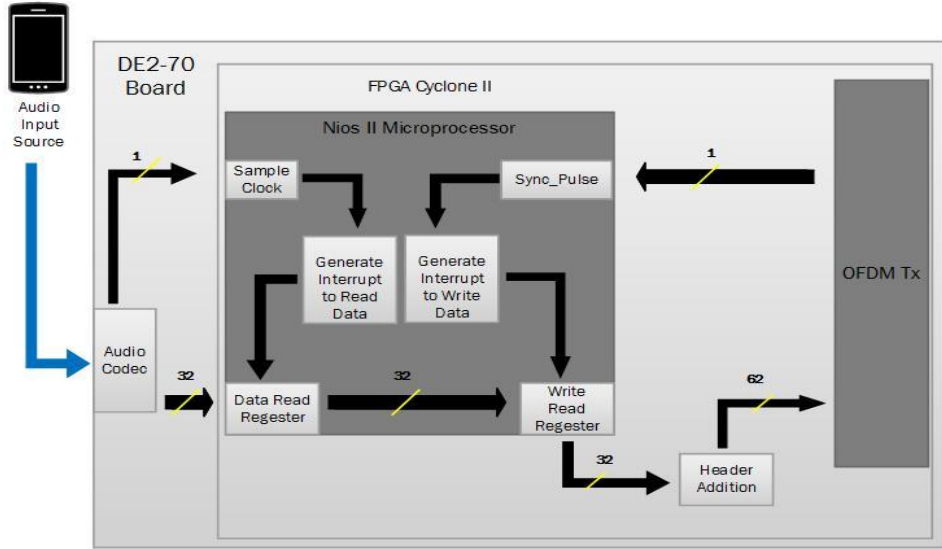
# System Overview

4 modules:

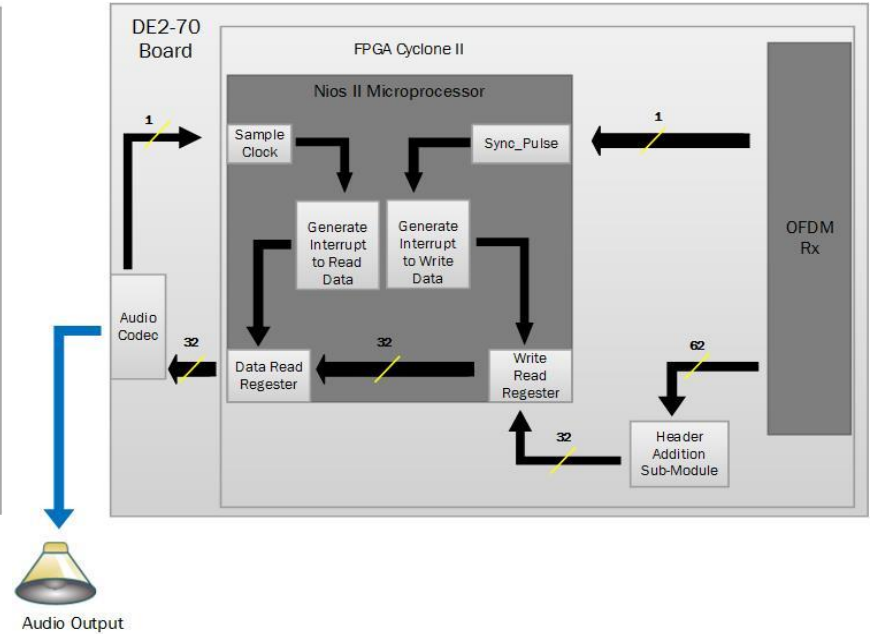
- Audio processing module
- OFDM module
- RF module
- Isolation & coupling module



# Transmitter/Receiver Pair (RF and isolation/coupling omitted)



**Transmitter**

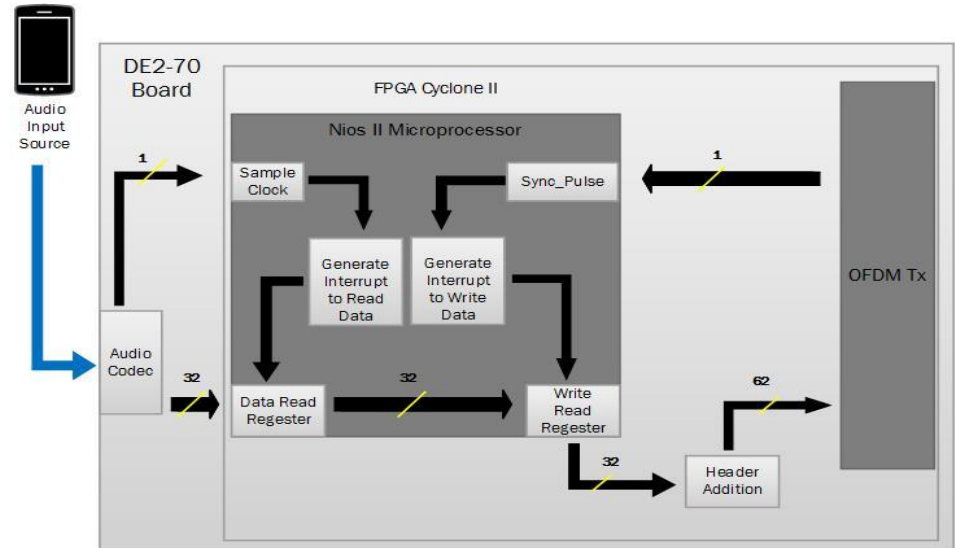


**Receiver**



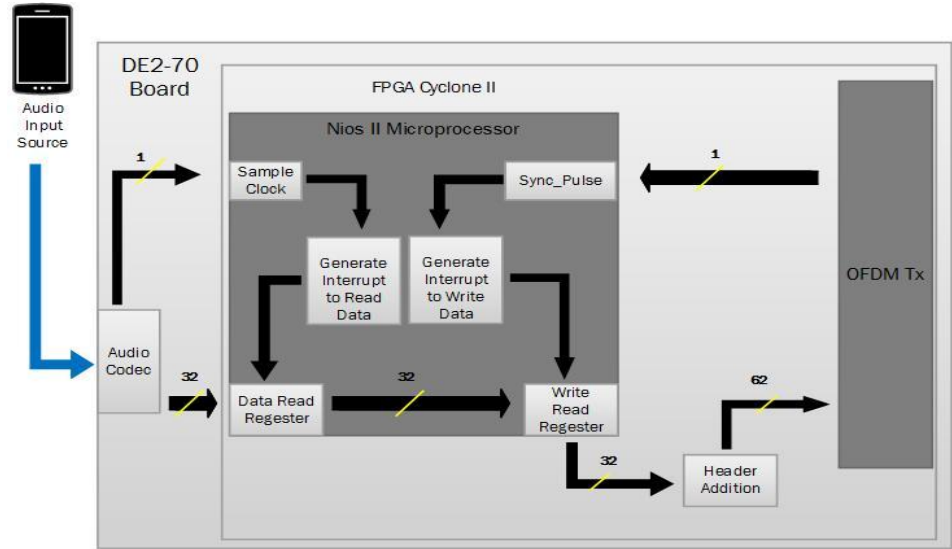
# Input and Output Specifications

Sub Module	Input	Output
Audio CODEC	Analog audio signal	32 bit digital data (16 bit left and right channel)
Nios II Processor	32 bit digital data	32 bit digital data
Header Addition	32 bit digital data	62 bit digital data



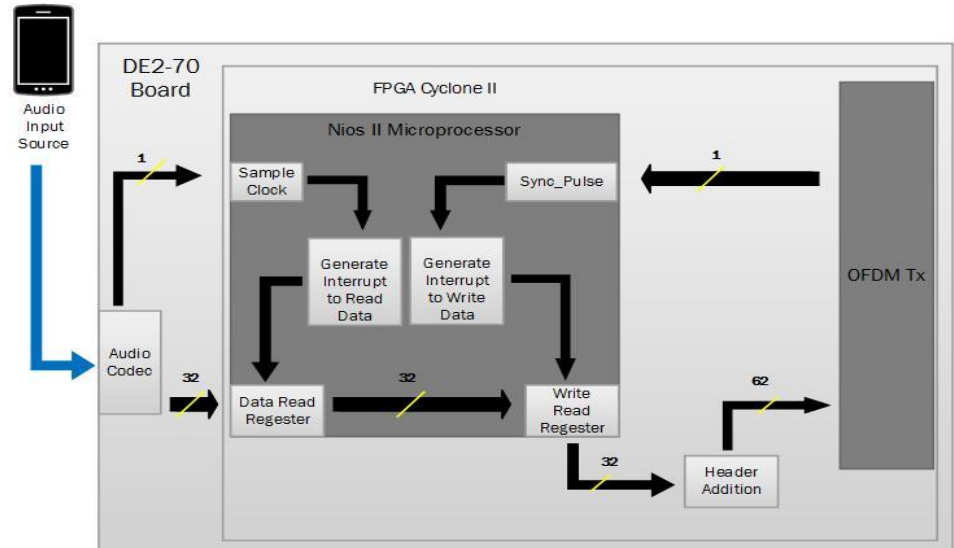
# Audio CODEC Sub Module

- Wolfson WM8731 Audio CODEC
- Data sampling rate ~40 kHz
- Implemented in VHDL



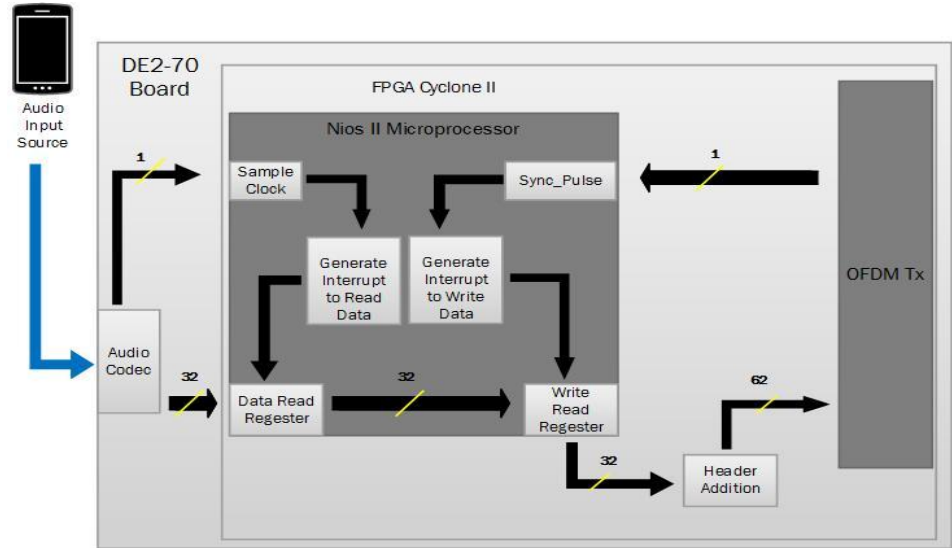
# Nios II Processor Sub Module

- Used Nios II embedded processor
- Implemented functionality via interrupt service routines
- Used different clocks for data read and data write registers



# Header Addition Sub Module

- Implemented in VHDL
- Uses a 10 MHz clock to facilitate synchronization

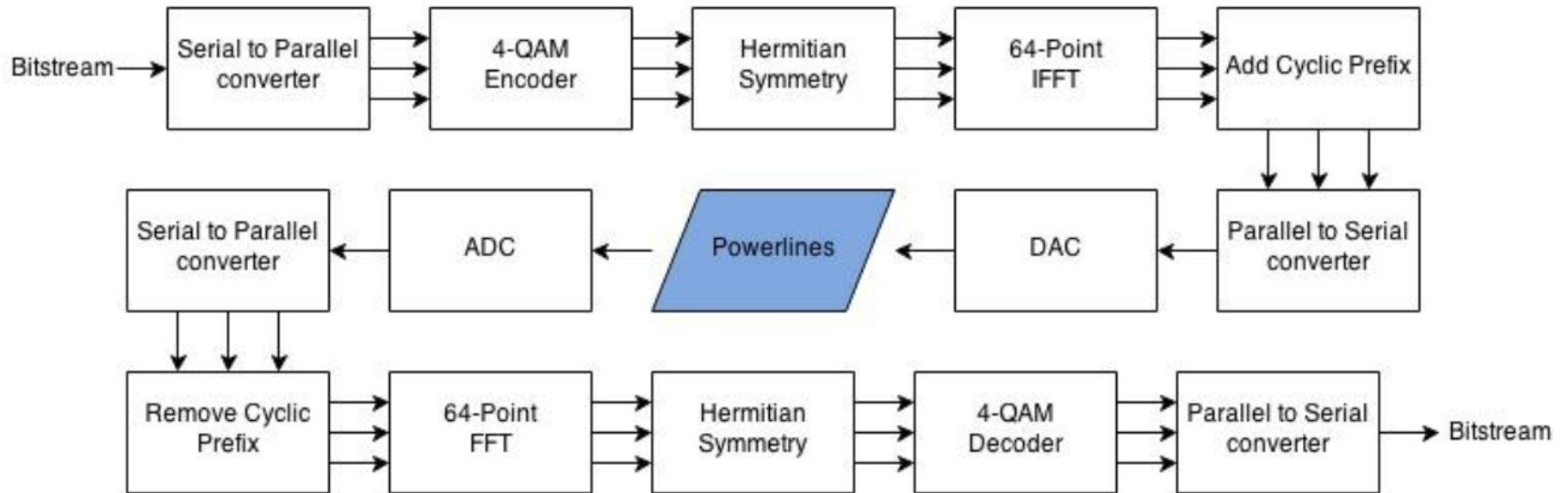


22	L	...	0	L	0	L	0	R	...	0	R	0	R	0
1's	(15-12)			(7-4)		(3-0)		(15-12)			(7-4)		(3-0)	

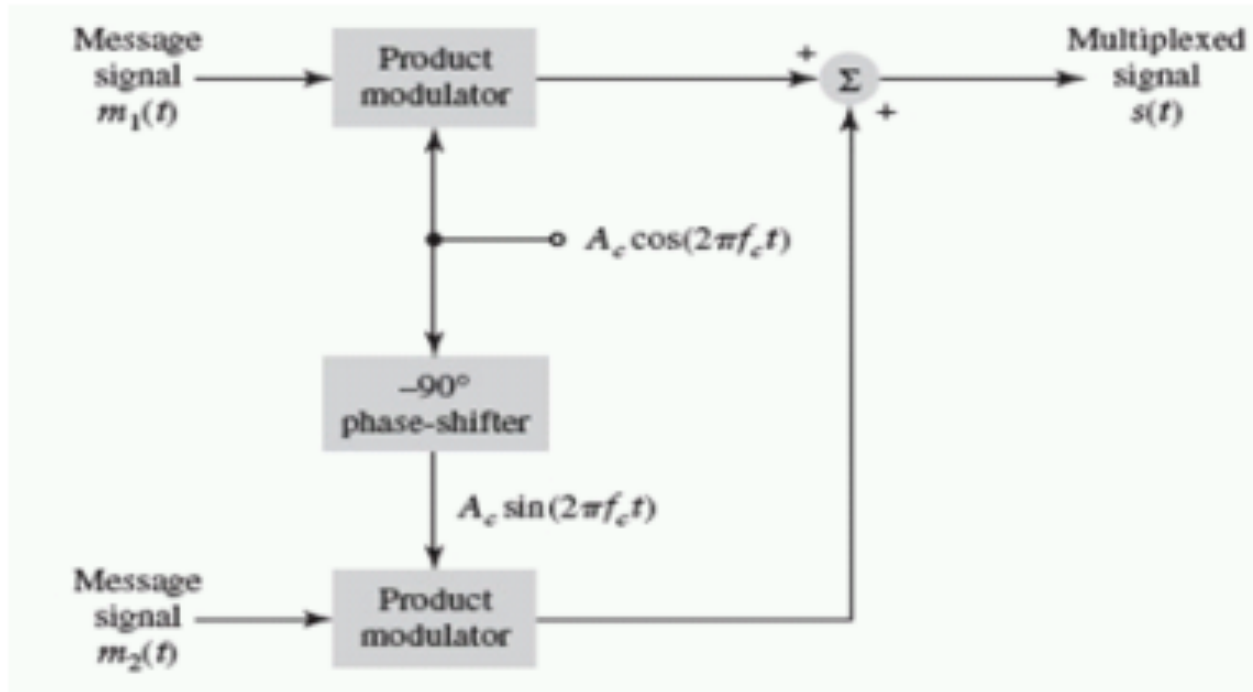
# Why OFDM?

- Bandwidth efficient (overlapping orthogonal signals)
- Resistant to channel fading
  - Probability is lower than single carrier
  - Better audio quality
- Robust against Intersymbol Interference (ISI)
- Robust against Subchannel Interference (ICI)

# OFDM Module High Level Diagram



# RF Module (QPSK)



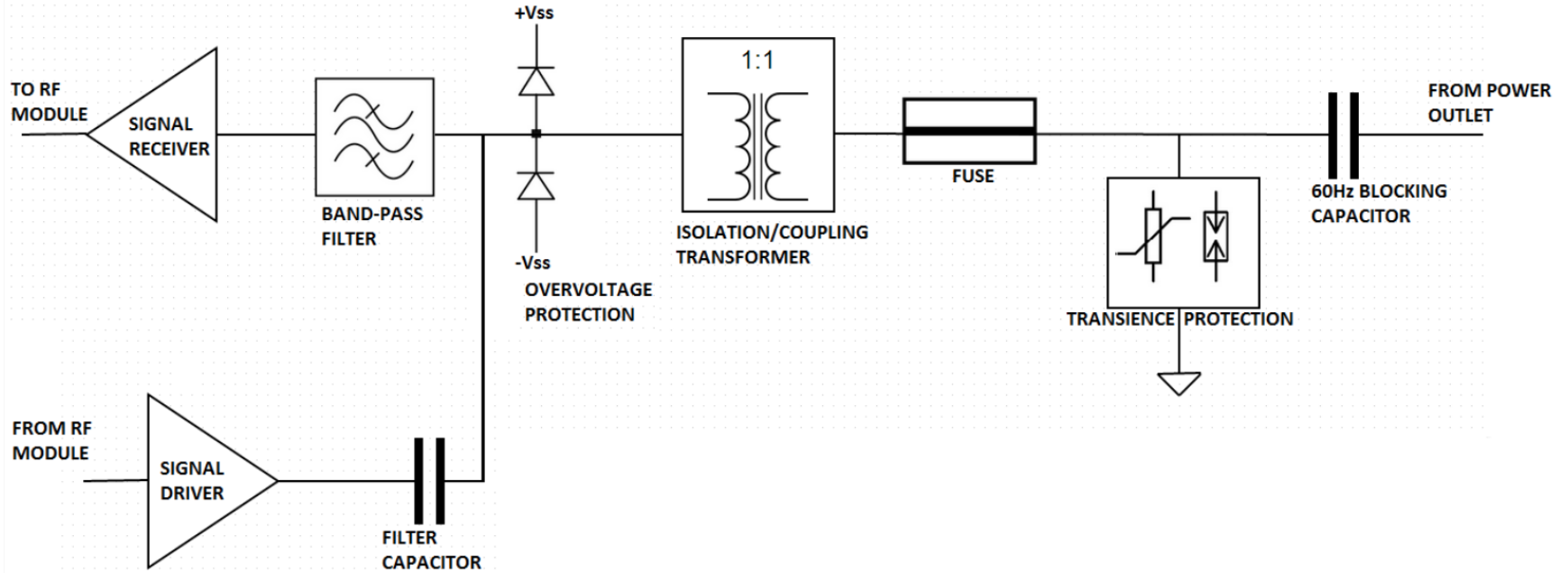
# Isolation & Coupling Module

Unusual communication medium

- Protect from 120V @ 60Hz
- Drive and couple the signal



# Isolation & Coupling Module



# Projected Timeline

Task Name	Duration	Start	Finish	'14 Jan 19							'14 Feb 02							'14 Feb 16							'14 Mar 02							'14 Mar 16							'14 Mar 30						
				S	W	S	T	M	F	T	S	W	S	T	M	F	T	S	W	S	T	M	F	T	S	W	S	T	M	F	T	S	W												
Primary Research	35 days	Fri 14-01-03	Thu 14-02-20	[Gantt bar from Jan 3 to Feb 20]																																									
Proposal	6 days	Thu 14-01-16	Thu 14-01-23	[Gantt bar from Jan 16 to Jan 23]																																									
Sourcing/Ordering Parts	26 days	Mon 14-01-20	Sun 14-02-23	[Gantt bar from Jan 20 to Feb 23]																																									
Functional Specification	18 days	Thu 14-01-23	Mon 14-02-17	[Gantt bar from Jan 23 to Feb 17]																																									
Design Specification	27 days	Sat 14-02-01	Mon 14-03-10	[Gantt bar from Feb 1 to Mar 10]																																									
Assmebling and Testing Modules	21 days	Mon 14-02-10	Mon 14-03-10	[Gantt bar from Feb 10 to Mar 10]																																									
Integration and Prototype Testing	21 days	Mon 14-03-03	Mon 14-03-31	[Gantt bar from Mar 3 to Mar 31]																																									
Debugging	13 days	Thu 14-03-13	Mon 14-03-31	[Gantt bar from Mar 13 to Mar 31]																																									

# Deviations from the Timeline

- Ongoing R&D
- Ongoing parts acquisition/replacement
- Assembly of modules mostly complete
- Integration not fully complete

# Initial Projected Costs & Funding

Parts List	#	Cost
DE2-70 FPGA Board	2	\$0 (ESSEF Parts Library)
AFE7225 Evaluation Module	2	\$998
Miscellaneous	-	\$100
Subtotal		\$1098
Tax		\$131.76
Total		<b>\$1229.76</b>

## Funding:

ESSEF Fund: \$700

Anticipated Remaining Cost: \$529.76

# Final Project Cost (approximate)

Parts List	#	Cost
DE2-70 FPGA Board	2	\$0 (ESSEF Parts Library)
ASLK Pro Boards*	2	\$0 (Part of ENSC 425 Lab)
ADC/DAC Boards	2	\$350.00
Miscellaneous Parts**	-	~\$250.00
Subtotal		\$600.00
Tax and Shipping		\$100.00
Total		<b>\$700.00</b>

New Design:  
Significantly Lower Costs

\* Not used in final design

\*\* Mostly isolation/coupling circuit and powerline model

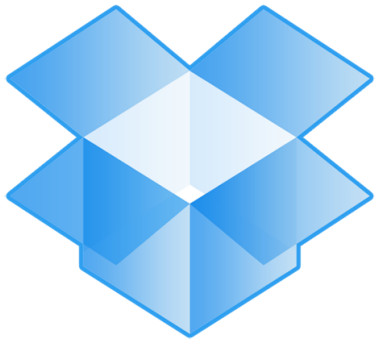
# Production Costs

- ASIC chips (no FPGAs)
- Enclosure
- Hard to estimate overall cost
  - Exactly what/how much resources used in FPGA?

# Team Dynamics & Workflow

- Engineering work divided by modules
- Non-engineering tasks:
  - Documentation: overseen and finalized by Kim
  - Scheduling: Laura
  - Budget & finances: Andy
  - Purchasing: Josh and Kim

# Communication tools



Communicate and collaborate  
through the cloud





# Things we learned

- Difficult to integrate new members
- Large ambitions
  - Address member concerns early and with care
- Make use of time spent together

# Future Plans

No current plans for the overall project

Individual plans:

- Transmission over actual power lines
- Lossless transmission over OFDM + RF modulation

# Sources

- [1] G. Zhou, J. A. Stankovic and S. H. Son, "Crowded Spectrum in Wireless Sensor Networks," *IEEE*, pp. 4-5, 2006.
- [2] Wolfson Microelectronics, "Portable Internet Audio CODEC with Headphone Driver and Programmable Sample Rates," 2004. [Online]. Available: <http://www.altera.com/education/univ/materials/boards/de2-70/unv-de2-70-board.html>. [Accessed March 2014].
- [3] P. P. Chu, *Embedded SOPC Design with Nios II Processor and VHDL Examples*, John Wiley & Sons, Inc., 2011.
- [4] P. m. Tmsiqueira, "OFDM modem :: Overview," OpenCores, [Online]. Available: <http://opencores.org/project,ofdm>. [Accessed 28 January 2014].
- [5] Wikipedia, "Orthogonal frequency-division multiplexing," [Online]. Available: [http://en.wikipedia.org/wiki/Orthogonal\\_frequency-division\\_multiplexing](http://en.wikipedia.org/wiki/Orthogonal_frequency-division_multiplexing). [Accessed February 2014].

# Acknowledgements

- Fred Heep
  - Modifying the ADDA circuit
- Lucky One
  - DE2-70 board and consulting
- ESSEF
  - Second DE2-70 board
- Jameson and Guinness
  - Therapeutic and relaxation aid

# QUESTIONS

