ELECTRAUDIO

Introduction

SoundSocket, an innovative product from Electraudio, is an audio system which utilizes the concept of power line communication to transmit an audio signal. With SoundSocket, the user simply plugs the transmitter unit into a wall outlet and may utilize another outlet as both the audio and power source for the receiver unit. SoundSocket is a reliable product that transmits CD quality audio. Our design is split into 4 modules: Audio Processing, OFDM, RF and Isolation/Coupling. This document describes the progress and current state of the project. The financial status, scheduling issues and the solutions to current problem are outlined.

Financial Status

Initially, we started with a budget of $1230, $700 of which is provided by the ESSEF and the remaining $530 to be covered by personal member funds and the Wighton Fund. We planned to use the AFE7225 Evaluation module which would take up $998 of our budget, but it made it a huge risk if we ran into issues including part failure and or accidents. However, as of March we have decided that the component was no longer needed and went with an alternate design which utilized cheaper components. The current breakdown of parts used is shown below.

Table 1- Current Expenses

Parts List	Quantity	Unit Cost	Sub Cost
DE2 70 FPGA boards	2	$ -	$ -
ASLK Pro boards	2	$ -	$ -
ADC/DAC boards	2	$ 175.00	$ 350.00
RF Cable SMA M/M 6"	2	$ 12.24	$ 24.48
RF Cable SMA/BNC RG174 18"	2	$ 12.89	$ 25.78
IC OpAmp VFB 70MHz 8DIP	4	$ 5.44	$ 21.76
XFRMR 1:1 FOR Cirrus Logic T/H	4	$ 3.73	$ 14.92
CAP CER 0.047uF 250V 10% Radial	10	$ 0.38	$ 3.84
Shipping, Duties and Taxes			$ 78.89
		Total =	**$ 519.67**
Preliminary Budget Allotted	**$1,230**		
ESSEF Funding	**$700**		
Personal Funds + Wighton Fund	**$530**		
Current Expenses	**$ 519.67**		
Current Remaining Budget	**$710**		

The DE2-70 FPGA boards remain cost free as they were borrowed from the ESSEF Parts Library. We also managed to eliminate the cost of the ASLK Pro Boards by borrowing them from a Professor. By eliminating the AFE7225 modules, we now have roughly $710 left. There are still uncertainties in some parts of our design, but there should be enough room to cover any additional components necessary. Financially, we are in very good condition and do not foresee any issues related to possible future purchases of components.

Schedule

The initially proposed project schedule is depicted in Figure 1. The specified timings have been subjected to some adjustment as the initial scheduling choices were made under the premise that our demo would be as early as April 1st, but in reality it will occur on April 14th. The primary research and documentation was all completed on time, however, as construction and testing progressed, it was determined that some additional/substitute parts still remain to be purchased. The assembling and testing of the individual modules phase and the integration and prototype testing phase of the project have more overlap than what is depicted in the initial schedule as integration considerations are incorporated into the design of the individual modules. We have encountered some delay in the completion of the individual modules, but should be able to complete this phase by April 4th. We are essentially on track to complete the proof-of-concept model, given that the actual demo date is 2 weeks after the day we initially aimed for.

Task Name	Duration	Start	Finish
Primary Research	35 days	Fri 14-01-03	Thu 14-02-20
Proposal	6 days	Thu 14-01-16	Thu 14-01-23
Sourcing/Ordering Parts	26 days	Mon 14-01-20	Sun 14-02-23
Functional Specification	18 days	Thu 14-01-23	Mon 14-02-17
Design Specification	27 days	Sat 14-02-01	Mon 14-03-10
Assmebling and Testing Modules	21 days	Mon 14-02-10	Mon 14-03-10
Integration and Prototype Testing	21 days	Mon 14-03-03	Mon 14-03-31
Debugging	13 days	Thu 14-03-13	Mon 14-03-31

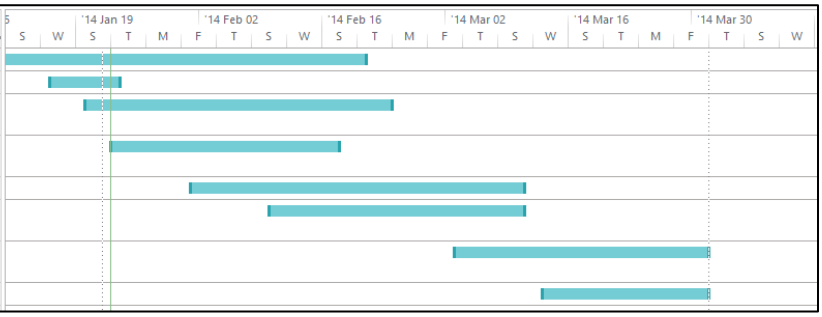

Figure 1: The original project schedule

Audio Processing Module

The audio processing module is composed of three sub modules: the audio CODEC sub module, the Nios II processor sub module, and the data serialization sub module.

Progress

The implementation of the audio CODEC sub module has successfully been completed. The testing of this module has been successfully completed via processing the incoming and outgoing audio signal on the receiver and transmitter modules, respectively. The implementation of the Nios II processor sub module is approximately 80 % complete. The remaining steps to implement this sub module includes communicating with the data serialization module. The testing of this module is still under progress and will be completed when the data serialization sub module is fully implemented.

Remediation

The data serialization sub module is the last step in the development of the audio processing module. It is responsible for serializing the parallel data coming from the Nios II processor sub module and passing the data on to the OFDM module. This is the key component for communication between the audio processing module and the OFDM module. After research and consultation, it was determined that the timing constraints for serializing the data and passing it on to the OFDM module plays a very crucial role in the communication. Thus the implementation of this module will be done in collaboration with the OFDM module development team. Testing of the entire audio processing module will be done via inputting data to the audio CODEC module of the transmitter and outputting the data on the receiver.

OFDM and RF Modules

Progress: OFDM Modem

The OFDM modem is progressing along however a few major issues have been identified. The core component of the modem, a modification of an open hardware has been tested in ModelSim simulations with results confirmed in Matlab. This design has been successfully synthesized and downloaded to the DE2-70 FPGA board and signals measured and successfully compared to simulation results. We have also successfully tested both the DAC with test signals generated inside the FPGA and measured on an oscilloscope. The ADC was tested using a function generator and an FPGA internal logic analyzer. The next milestone was where we ran into some major problems. When we started to use the DAC to output our OFDM signal we noticed distortion in the analog output. The problem was with low frequencies because the DAC/ADCs are transformer. Other issues that remains pending are synchronization between transmitter and receiver however the distortion problem needs to be resolved first before significant work can go into synchronization.

Progress: RF Module

We have run experiments on the frequency multipliers that are included with the ASLKPRO boards from Ti and confirmed that they have a maximum output bandwidth of 10 MHz which may present a problem as it puts a limit on our maximum signal bandwidth.

Remediation

We are actively exploring multiple potential solutions to our unresolved problems. For the DAC/ADC distortion issue one solution is to move where the RF modulation will occur from the analog domain into the digital domain and perform the modulation on the FPGA before and after the signals reaches each of the DACs and ADCs respectfully. This allows us to bypass the low frequency limitations of the DAC/ADC and because they have very high sample rates this will not violate any Nyquist criteria. This solution would also save cost in replacing the frequency multipliers and simplify the analog design. Another road being investigated is an Altera reference design for implementing OFDM Modulation and Demodulation which provides another example design which will likely present design solutions and act as a solid plan B if the current design does not end up working correctly. The Altera reference design is currently being analyzed and tested in parallel with continued work on the original design.

Isolation and Coupling Module

Progress

In the very early stages of the project, we have researched the principles and methods of powerline communication, concentrating on the isolation and coupling issues as these were somewhat unique to the application. We have studied a few possible design variations based on different isolation and coupling solutions that were discovered during research. Based on availability of components and ease of implementation, we have comprised a method suitable for our needs. Using this method, we repeated the process of (re)designing the circuit, simulating and analyzing the results, until analysis proved the circuit to be operational. At that point, the components were sourced and ordered. With components available to us, the circuit was built and successfully tested at a proof-of-concept level; the circuit behaved as expected. However, there are 3 main issues that we have encountered:

1. In the process of ongoing research, after the first circuit was built, some components turned out to be less than ideal for our application.

2. As the OFDM and RF module still under development, their exact finalized operation isn't completely defined. Thus, it is difficult to predict if the receiver will be affected by the non-linear phase response of the isolation/coupling circuit at certain frequencies.
3. We've allowed an oversight to occur by testing the isolation/coupling circuit without grounds truly isolated from each other. This was due to the fact that the equipment in Lab 1 shares a common ground internally.

Remediation

The first issue was trivial to fix. Once the components list was overviewed, substitute components were identified. These are now sourced and ready to be ordered from a fast-delivering vendor.
The second issue will be resolved once the OFDM and RF module operation is fully defined. If the latter requires the phase response of the isolation/coupling circuit to be linear in a certain frequency range, modifications will be implemented to expand the linear phase region to accommodate the signal.
Finally, the third issue requires acquiring isolation transformers from our lab technicians and minimal modifications to circuit assembly. These will be made in next few days. The resulting circuit has already been successfully simulated in LT-spice; it is essentially the previously chosen design. Based on our educated guess, if any changes do occur due to true ground isolation, these will be of a positive nature (i.e, higher signal to noise ratio may be observed).

Conclusion

All the issues and the solutions that are being implemented have been outlined in this document. We are behind our initial schedule. However, given that it was initially planned with a premise of an early demo, the actual demo time gives us an extra two weeks. This is enough to compensate for our delay. In terms of the project integration, each module is developed and tested under close coordination with the specifics of the other modules. Thus, the integration is expected to be relatively simple once the modules are fully functional.