A Vector Light Sensor for 3D Proximity Applications: Designs, Materials, and Applications

by

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Abstract

In this thesis, a three-dimensional design of a vector light sensor for angular proximity detection applications is realized. 3D printed mesa pyramid designs, along with commercial photodiodes, were used as a prototype for the experimental verification of single-pixel and two-pixel systems. The operation principles, microfabrication details, and experimental verification of micro-sized mesa and CMOS-compatible inverse vector light pixels in silicon are presented, where p-n junctions are created on pyramid's facets as photodiodes. The one-pixel system allows for angular estimations, providing spatial proximity of incident light in 2D and 3D. A two-pixel system was further demonstrated to have a wider-angle detection. Multilayered carbon nanotubes, graphene, and vanadium oxide thin films as well as carbon nanoparticles-based composites were studied along with cost effective deposition processes to incorporate these films onto 3D mesa structures. Combining such design and materials optimization produces sensors with a unique design, simple fabrication process, and readout integrated circuits' compatibility.

Finally, an approach to utilize such sensors in smart energy system applications as solar trackers, for automated power generation optimization, is explored. However, integration optimization in complementary-Si PV solar modules were first required. In this multi-step approach, custom composite materials are utilized to significantly enhance the reliability in bifacial silicon PV solar modules. Thermal measurements and process optimization in the development of IMEC's novel interconnection technology in solar applications are discussed. The interconnection technology is used to improve solar modules' performance and enhance the connectivity between modules' cells and components. This essential precursor allows for the effective powering and consistent operations of standalone module-associated components, such as the solar tracker and Internet of Things sensing devices, typically used in remote monitoring of modules' performance or smart energy systems. Such integrations and optimization in the interconnection technology improve solar modules' performance and reliability, while further reducing materials and production costs. Such advantages further promote solar (Si) PV as a continuously evolving renewable energy source that is compatible with new waves of smart city technology and systems.

Keywords: spatial proximity; optical sensor microfabrication; silicon, Graphene and Multi-walled Carbon Nanotube composites, interconnection PV solar, IoT smart energy system

To my parents

For their love, support, compassion, and sacrifice. Thank you.

Acknowledgements

I would like to express my gratitude for Dr. Jef Poortmans for giving me the opportunity, twice, to work under his supervision and along world class researchers, experts, and students from various backgrounds and disciplines at IMEC, KU Leuven, UHasselt, and other universities and research institutes. It's a truly unique experience. The support and inspiration along with continued mentorship within the department in general and within the PVMS team has been truly aspirational.

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Disclaimer: I am not associated with any of the individuals at the school of mechatronics systems engineering at SFU, nor am I associated with their business ventures or activities. I did not authorize anyone at the school or university to claim or take credit for any capacity of my work. I am not privy to nor am I a participant in any activities that fringe The University Act, BC's Employment Standards Act, WorkSafeBC's The Occupational Health and Safety Regulation, any other federal or provincial acts or law, SFU policies, Tri-Agency's Framework for Responsible Conduct of Research, or any other public agencies' policies.

There is nothing more despicable than spineless hypocrites with questionable integrity and flexible morals who provide quasi-researchers with the sufficient intentional oversight and protection to mutually abuse their way into becoming academic ***winners***, suchcoolmuchwow.jpg. It wouldn't be surprising to find the same individuals prey on public tragedies to virtue signal their way into their self-proclaimed 5 minutes of academic fame, as they desperately cling onto career paths they are not qualified for.

SFU's Board of Governors and The University remain responsible and obligated to address the infringes brought forth to the school, department, faculty, and admins. It's

not a choice left to the self-proclaimed privileged in academia, it's a federal and/or provincial mandate.

Before enrolling into SFU grad studies, prospect students should be aware of the abuse that happens to grad students on a regular basis at SFU, with admin support and cover-ups. After an exhausting series of abuse throughout the graduate program at SFU, I defended my PhD dissertation on August 26th, 2021, 4.5 years too late, as confirmed by several external reviewers and the defence external examiner. The defence committee orally claimed that I have passed the thesis defence, with requests for minor edits. Yet, they refused to provide me with a written approval of the request. It took over 2 months, after the defence, to receive the Results, Approval & Degree Recommendation (RAD) form, or receive the notes and comments, which the defence committee members have based their evaluation on.

I've attempted submitting corrections to minor edits, which are mostly in the form of minor mistakes/changes and formatting errors (some of them were made due to personal preference of formatting). Yet, the university refused to process my submission. The minor edits are by all accounts, suggestions, which I, the author, am free to completely disregard. The total amount of time spent on the suggested corrections was ~5 hours, requiring a maximum time commitment from SFU faculty of ~2 hrs. Just like all other forms of abuse at SFU centered at deliberate delays, SFU has refused to provide the reasons for the unreasonable and unjustifiable delays.

I have also proposed alternative suggestions, where SFU admins and faculty won't do the bare minimum of their jobs, by out-sourcing the suggested corrections to a third party. SFU admins and faculty refused to respond to such a request.

SFU faculty members and admins have gone out of their way and stopped at nothing to steal my data and research work (and personal stuff), ruin my academic reputation, destroy any chances I have at transitioning out of this so-called educational institution into an academic or industrial role.

It became clear that the several other grad students have been the subject of all kinds of abuse. More information about such abuse was submitted to the Tri-Agency Council and the BC Ombudsperson's Office. The BC Ministry for Advanced Education suggested that the RCMP should be contacted for some types of abuse, while the BC Ombudsperson's Office should address the general systemic abuse.

It would be fair to say that grad student abuse at SFU is normal and expected. Keeping up with the abuse requires dedicated physical and mental resources. This will likely be a requirement to pursue a grad-level degree at SFU.

Public institutions and funds, operated and allocated through taxpayers' hard-earned income, must not be used to support abuse.

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List of Acronyms

VOS	Vector Optical Sensor
CMOS	Complementary Metal Oxide Semiconductor
VLS	Vector Light Sensor
3D	Three Dimensions/ Three Dimensional
2D	Two Dimensions/ Two Dimensional
PSD	Position Sensing Detector
CCD	Charged Coupled Devices
I-V	Current - Voltage
TIA	Transimpedance amplifier
KOH	Potassium hyrdoxide
EDP	Ethylene Diamine Pyrocatechol
TMAH	Tetramethyl ammonium hydroxide
IPA	Isopropyl alcohol
DI	De-ionized
Si	Silicon
SiO_2	Silicon dioxide
UV	Ultraviolet
BOE	Buffered Oxide Etchant
HMDS	Hexamethyldisilazane
P	Phosphorus
GO	Graphine oxide
MWCNT	Multi walled carbon nanotubes
TPO	Thermoplastic polyolefin
TPO-A	Thermoplastic polyolefin of type A
TPO-B	Thermoplastic polyolefin of type B
c-TPO-A	Composite material using thermoplastic polyolefin of type A
CTE	Coefficient of thermal expansion
EL	Electroluminescence
SWCT	Smart wire connection technology

List of Symbols

P_{facet}	Power that reaches a facet
A	Surface area of an active region
I	Intensity of light
β	Angle of an incident optical projection from the parallel line
θ	Incident projection forms an angle with the pyramid surface normal
α	Base angle of the pyramid
γ	Angle at which a triangle α β γ is formed
R_λ	Responsitivity of a photodiode
I_P	Generated photocurrent
I_D	Photodiode dark current
I_{SAT}	Reverse saturation current
q	Electron charge
V_A	Applied bias voltage
k_B	Boltzmann Constant
T	Temperature
I_{Total}	Total current in a photodiode at specific voltage value V
R	Ratio between the radiative powers
ϕ	Rotational angle
z	Height of the incident optical source
d	Distance between two pixels
a	Corner compensation structure, square with side ‘a’
H	Desired etched depth
D	Diffusion coefficient
D_0	Typical diffusion coefficient
E_A	Activation energy
ω_n^*	Natural frequency of the n^{th} mode in absence of perturbation
N_s	Surface concentration
N_B	Background concentration
x_j	Junction depth
I_{tn}	total noise current generated in a photodetector
I_{sn}	Shot noise

Δf	Noise measurement bandwidth
R_{SH}	Shunt resistance
NEP	Noise Equivalent Power
L_P	Characteristic diffusion length
τ	Tilt angle
$\mathrm{V_{oc}}$	Open circuit voltage
$\mathrm{I_{sc}}$	Short circuit current
FF	Fill Factor
$\mathrm{R_s}$	Series resistance

1. Introduction

1.1. Motivation

The Internet of Things (IoT) is the wider ecosystem that interconnects physical devices through the Internet. Typically, the physical devices include sensing components, allowing devices to acquire physical inputs or monitor changes in their environment, and an interface to relay the information to the network of sensors. The development of more robust communications and connectivity systems suitable for large scale transmission of data also emerged. Particularly low power systems such as LoRAWAN, Low Power Wide Area, and 5G NR, has facilitated the systems' operational transition towards cloud and/or edge computing components were standardized in some aspects. Moreover, a concurrent shift emerged with further demand for the rise of increasingly complex, and correlated, systems such as smart cities and Big Data applications. All of these elements have allowed for the deployment of wider networks of embedded sensing devices. For example, in real-time applications, the integration of low power, reliable sensors have played an instrumental role in providing delivering accurate results associated with split- second decisions, an integral stepping stone for the implementation of technologies such as autonomous vehicles.

Proximity sensors are non-contact sensing devices found in several real-time and feedback applications, as they offer controlled sensing capabilities without the need for physical contact. Such sensors are essentially used for localization, monitoring, and obstacle avoidance systems in robotics and autonomous systems as well as in dynamic

virtual and augmented visualization systems in medicine, as three-dimensional overlay projection imaging during surgery or as navigation tools during diagnostic medicine and robotic surgery. High quality embedded sensors are also required in other virtual and augmented environmental mapping applications, as well as allowing for 3D tracking and motion analytics, multi-level focusing in digital imaging, and remote surveillance [1]–[13].

Thus, there's a continuous appeal for less computationally insensitive, more power-efficient, reliable sensing systems which can be obtained at reasonable cost. Such optimization allows for easier integration of embedded sensors in all applications, as sensing choices are typically regarded as a trade-off between complicated, expensive and reliable systems or low quality basic systems which are unreliable. For certain specific applications, this trade-off is dealt with by the application of specific integrated circuits.

Following this approach, a 3D design for vector optical sensing (VOS) pixel system is introduced. Using a VOS, angular proximity can be estimated to provide spatial information of incident optical sources. Unlike planar pixel designs, a single VOS pixel system can be used to calculate the angular estimations and spatial proximity of incident light in 2D, and 3D in a limited capacity. Adopting a VOS pixel system would effectively replace planar designs, since multiple planar sensors are required to calculate the angular estimations and spatial proximity in 2D or 3D. An array of VOS pixels, compromised of at least two pixels, allows for the system to estimate the incident optical source position in 3D, thus, effectively reducing the computational and power requirements in systems, as fewer pixels than planar designs are required in array and non-array designs.

In addition to the unique design, a simple fabrication process is required as well as readout integrated circuits' compatibility. Such a 3D design offers directionality in detecting

the light source position, while maintaining the properties of multi-planar array systems. This ensures a fast and accurate response times. The inverse VOS pixel design should also be implemented in complementary metal oxide silicon (CMOS)-compatible processes, thus, allowing further integrations in integrated circuit fabrication processes. Combining the design with material optimization further allows the sensors to be utilized in specialized applications, such as thermal sensing and imaging.

1.2. Background: Proximity sensors

Proximity sensors are primarily non-contact sensors that are used for the detection of an object within a specific range. Depending on the type of the sensor and compatibility, the sensor may also provide informational analyses on objects' features. For example, a capacitive sensor, in which measured capacitance is proportional to the distance of the detected object, may be not be suitable for plastic targets, while an inductive proximity sensor requires detected objects to contain metal elements. Proximity sensors are frequently used as transducers, in which measured data is translated into a data form that can be readable by an instrument or device. Thus, sensors can be easily integrated into systems where translated output data may be used as triggers for other actions. For example, an electro-optical sensor can act as an optical switch in a system, where the electrical output is varied depending on the detected optical changes, thus, the switch may be used to trigger specific actions in a circuit relative to detected optical changes [1], [14]–[17].

Non-contact proximity sensors may be mainly categorized into optical and non-optical proximity sensors.

1.2.1. Non-Optical Proximity Sensors

(A) Ultrasonic proximity sensor

Ultrasonic proximity sensors employ high frequency sound waves to detect the presence or absence of an object. They operate by emitting sonic waves and measuring the time between emitted signal and target-reflected signals. The proximity distance is then calculated based on the elapsed time. Excluding sound absorbing or deflective materials, target objects' material, color, or transparency have little to no effect on the sensor's responsitivity, making them a popular choice for projects. The sensors are typically made with piezoelectric material, sometimes ferroelectric materials, where the sensor's size slightly changes when exposed to a magnetic field. However, ultrasonic sensors have a slower response time relative to photoelectric sensors. In addition, sensors with wide reading ranges have noise issues pertaining to reflected signals' interferences. Ultrasonic sensors are used in a variety of applications, particularly for long range detection and underwater applications [14], [15], [18], [19].

(B) Inductive proximity sensor

Inductive proximity sensors are another type of non-contact sensors. They are typically used to detect proximities of objects containing metals. The sensors usually consist of a coil that is driven by an oscillator, thus creating an oscillatory magnetic field around the coil. When a conductor is brought within the sensing range of the coil, electromagnetic forces induce eddy currents on the metal's surface, in a direction opposing the field of the exciting coil. Thus, the coil's inductance is reduced due to Lenz's law. The magnitude of inductance change can then be used to calculate the proximity of the conductor. The sensing range of the sensors vary depending on the type of metal being detected. These sensors are not as affected by contaminated environments such

as dirt or moisture, allowing them to be adapted into a wide range of applications, such as metal detectors. However, they are limited to sensing objects that contain metallic elements. They also have a relatively narrow sensing range, due to the magnetic field limitations [14], [20], [21].

(C) Capacitive proximity sensor

Capacitive proximity sensors are made of two parallel conduction plates, separated by materials, defined through their dielectric constants. Objects within the sensitive range of the capacitor, vary the sensor's capacitance changes. The change can be then used to determine several properties about the object, such as dimensions and conductivity. One advantage of capacitive sensors is that they can be adjusted to sense specific materials. However, the sensors' ability to detect most types of materials becomes an issue in the presence of materials not intended to be detected. In addition, they are generally affected by environmental factors including moisture and humidity [14], [17], [22]. A typical popular application of conductive sensors is touch screen in electronic devices.

1.2.2. Optical Proximity Sensors

There are various techniques in which non-contact optical sensors can be used to resolve properties about objects, such as the distance separating the sensor and object, surface profiles, velocities of moving objects, and vibrations. Photoelectric sensors provide a high range of detection, ranging from a few micrometers to few meters depending on the detection technique used, making them versatile and popular in industrial sensing solutions. They are mainly classified by the method in which light is emitted and delivered to the receiver. Despite differences in detection methods, all photoelectric sensors consist

of an emitting light source and a receiver, where supporting electronics designed are commonly used to amplify received signals. An emitting light source, in the form of an incandesce light source, a light emitting diode, or a laser diode for example, would emit an optical signal in the visible or infrared range. A receiver, in the form of a photodiode, a photo-resistor, or a phototransistor for example, would be used to detect emitted light [14], [23], [24].

Light detection for proximity sensing can be classified based on whether light is reflected, diffused by the target, or whether the target blocks emitted light from reaching the receiver. Among such methods are proximity detection based on interferometry, intensity changes due to light getting reflected from objects, triangulation, and time-of-flight.

(A) Interferometry:

Interferometry is a method, often associated with lasers, in which electromagnetic waves from a single source are split into beams that travel different optical paths, then get superimposed to produce interference patterns. The interference patterns can then be used to extract information about objects. Interferometers are widely used in spectroscopy, astronomy, and seismology, as well as in quantum mechanics and nuclear, plasma, and particle physics to extract information such as small displacements measurements, changes in refractive index, and surface topographies [23]–[25].

(B) Intensity

The intensity method of utilizing light detection for proximity estimations offers a relatively cheap alternative. Light beams are usually used to detect objects, in which the

emitter provides a constant beam of light to the receiver. Object detection occurs when the receiver indicates a reduction in light intensity following light reflections from detected objects. Thus, the distance between the light source and the detector can be estimated based on the intensity change. This method requires calibration, where distance and intensity of the light source must be first established. However, reflectivity of the target surface may result in higher intensity values due to reflections. In addition, intensity fluctuations in the light source due to dust layer buildup on either the emitter or transceiver or due to the light source leads to inaccurate distance estimations. Intensity based sensors can be used for long range sensing. However, installation and alignment requirements need to be taken into account. Intensity based sensors are used in commercial and industrial applications, such as obstruction detections or in inspection applications in the food industry [14], [23], [24].

(C) Triangulation

As mentioned in the previous section, utilizing intensity based methods to target rough or reflective surfaces, for example, may result with faulty readings. In addition, highly reflective objects in the background of areas of interest may be also sensed by the detector, thus, further contribute to readout errors. To address some of these limitations, triangulation, in which geometries of similar triangles, is used to estimate distance or position of detected objects. In this method, an optical light source emits a light beam projected towards objects, deflected or reflected beams are then detected by a receiver. With a known system geometry, unknowns such as angle of deflection or distances separating the detector from an object, or the object from the detector, can be calculated. Some triangulation systems use optical systems in order to refocus scattered light travelling towards the photodetector. Detectors in the form of position sensing detectors

(PSD) are often used in triangulation applications, where object location is determined based on the relative location of reflected light projections onto the photosensor [14], [23], [24], [26].

(D) Time of flight

In time-of-flight detection, light pulses are emitted towards objects, where the time taken for reflected light, from the surface of a detected object to reach the detector, can be used to calculate the distance of the object. This method works very well for longer ranges, where the time delay can be measured without the need for relatively expensive sub-nanosecond timing circuitry [23], [24], [27], [28].

1.3. Photodetectors

Optical PSDs can be used to collect three-dimensional coordinate data from object surfaces. This allows for PSDs to be useful in a wide variety of applications, including shape recognition and acquisition, digital imaging, motion and activity detection, as well as medical prognoses and diagnoses [6], [29]–[31]. Discrete PSDs rely on independent sensing elements such as charge-coupled device (CCD) or CMOS pixel arrays along with image processing software to measure target position. On the other hand, continuous PSDs, such as lateral photodiodes, use the difference in photocurrent ratios between detecting elements (photoconductors or p-n junctions) that are all connected to a single resistive layer. The resistive layer, together with the single p-n junction device, forms a variable resistive element. The element has a different overall resistance, based on the changes in the position of the incident light that illuminates the active area. Due to increased industrial demands for real-time detection and accurate object positioning in

dynamic and autonomous systems, as well as cost effectiveness in fabrication techniques, lateral PSDs have become favourable in many industrial areas. Furthermore, most current PSD systems that use planar array structure offer little to no direct means for angular measurements of the incoming light, thus, imposing limitations where the direction of the source object must be known. Faulty position estimations are mostly due to mismatches between device dimensions and incident light spot size [32]–[37].

1.4. Thesis Outline

The focus of this thesis is to demonstrate a new 3D design for optical sensing with the purpose of detecting angular and spatial proximity of an optical source in 3D. The photodetector design integrates photosensitive areas onto the slanted sides of a truncated pyramid, thus, creating a 3D design of the sensor. Geometry and intensity variations of photosensitive areas of the pyramid are utilized to estimate angular proximity.

A macroscale prototype using commercial photodiodes was used to validate the design. Macro-sized 3D printed mesa pyramids with commercial photodiodes on the pyramid facets were used to estimate the position of an optical source in 3D. Following prototype device performance validation, a microfabrication process was developed to fabricate micro-sized mesa and inverse pyramid pixel designs in silicon. P-n junctions were embedded into the inclined facets of the pyramids. Mesa pixel's sensing capabilities was demonstrated, where a single pixel system can be used to detect the inclination and rotational angles of radiation, thus, providing a spatial proximity of an optical source in 2D. In addition, the design's limitations for optical sensing at certain angles is discussed. The sensor's unique design and simple fabrication process allows the single pixel system to

successfully model and calculate the position, distance and angle of incidence of an incident light source. The fabrication details of inverse pyramid, CMOS-compatible, designs are also described.

Applying the 3D sensor design in applications that require optical responses in the low range IR regions instigated exploring thermoresistive materials as potential complementary materials to Si. Multilayered carbon nanotubes, graphene, and vanadium oxide thin films as well as carbon nanoparticles-based composites were explored for the fabrication of temperature sensitive resistors. Carbon-based nanoparticles were mixed with thermally and electrically insulating polymer composites, polystyrene, for film durability. Cost effective deposition methods were used to fabricate the films, and the materials' temperature coefficient of resistance were measured, compared, and discussed.

Finally, integration optimization in c-Si PV solar modules were first discussed. In this multi-step approach, custom composite materials are utilized to significantly enhance the reliability in bifacial silicon PV solar modules. Thermal measurements and process optimization in the development of IMEC's novel interconnection technology in solar applications are discussed. The interconnection technology is used to improve solar modules' performance and enhance the connectivity between modules' cells and components.

The structure of the thesis is as follows:

- Chapter 1: a general review of proximity sensing methods and the motivation behind the research are discussed.

- Chapter 2: the principles of operation for one and two pixel systems are introduced. The details about the prototype design are also discussed.

- Chapter 3: the microfabrication process of mesa and inverse VOS pixels, as developed by the author, is described and discussed with regards to CMOS compatible processing.

- Chapter 4: the experimental test setup for the prototype design and mesa VOS pixel testing are discussed. The design and analysis of fabricated devices are discussed, and a study about mesa pyramids' response to laser beam induced current is discussed.

- Chapter 5: carbon-based thin films and composites and their deposition process, for the fabrication of micro-bolometers are discussed.

- Chapter 6: optimization and reliability for the integration of IMEC's Si PV solar cell interconnection technology is discussed. Module preparation, thermal and electrical characterization of encapsulation polymer materials, and process optimization are discussed.

- Chapter 7: the thesis concludes with a brief summary and future development perspectives.

2. Vector Optical Sensor Macroscale Prototype

In this chapter, the design and principles of operation of a single vector optical sensor system as well as a two-pixel system are discussed, followed by a macroscale prototype validation, where 3D printing was used to fabricate mesa pyramids with a base angle 55°.

2.1. Principles of operation

2.1.1. Mesa Pyramid Design

For a plane wave of intensity I projection onto pixel's facets with surface area A, the unknown angle of incidence θ is proportional to the amount of power P that reaches the facets [38].

$$P_{facet} = A\, I\, cos(\theta) \tag{2-1}$$

The light source projected at angle β onto a pyramid surface with base angle α forms an incident ray at an angle θ with the pyramid surface normal. Thus, the complementary angle γ forms a triangle $\alpha\,\beta\,\gamma$, Figure 2-1.

$$\alpha + \beta + \gamma = 180° \tag{2-2}$$

It follows that using the trigonometry identity of cosine, the projected power onto the facet becomes,

$$P_{facet} = A\, I\, cos(\theta) = A\, I\, in(\beta - \alpha) \tag{2-3}$$

and projected power onto the opposing facet becomes:

$$P_{opposing\ facet} = A\ I\ cos(\theta) = A\ I\ sin(\beta + \alpha) \quad (2\text{-}4)$$

Photodiode characteristics [39]–[41] are proportional to the photocurrent. The responsivity, R_λ, of the photodiode is proportional to the photocurrent, I_P , generated due to incident intensity through

$$R_\lambda = \frac{I_P}{P} \quad (2\text{-}5)$$

When a reverse bias is applied, a small reverse saturation current appears. It is related to dark current as

$$I_D = I_{SAT}\ exp\left(\left(\frac{qV_A}{k_B T}\right) - 1\right) \quad (2\text{-}6)$$

where I_D is the photodiode dark current, I_{SAT} is the reverse saturation current, q is the electron charge, V_A is the applied bias voltage, k_B is the Boltzmann Constant and T is the absolute temperature at 273K.

When the photodiode is illuminated with optical radiation, the I-V characteristics curve (in the reverse bias region) shifts by the amount of photocurrent generated

$$I_{Total} = I_D - I_P \quad (2\text{-}7)$$

Where I_{Total} is the total current in the photodiode at specific voltage value V. Using normalized photocurrent readings from each photodiode, and taking into account the pyramid's base angle α, the ratio between the radiative powers received by the two opposing facets of a single mesa pyramid can be calculated as in the following:

$$R = \frac{I_{P\ (facet)}}{I_{P\ (opposing\ facet)}} = \frac{sin(\beta + \alpha)}{sin(\beta - \alpha)} \quad (2\text{-}8)$$

Where $I_{P(\text{facet})}$ and $I_{P\ (\text{opposing facet})}$ are normalized photocurrents at the facet at which light is projected and the opposing facet respectively. β is the angle at which incident light is projected from the parallel line, Figure 2-1. The inclination angle θ with respect to the facet normal at which light is projected can be calculated using

$$\gamma = \pi - (\beta + \alpha) = \frac{\pi}{2} - \theta \tag{2-9}$$

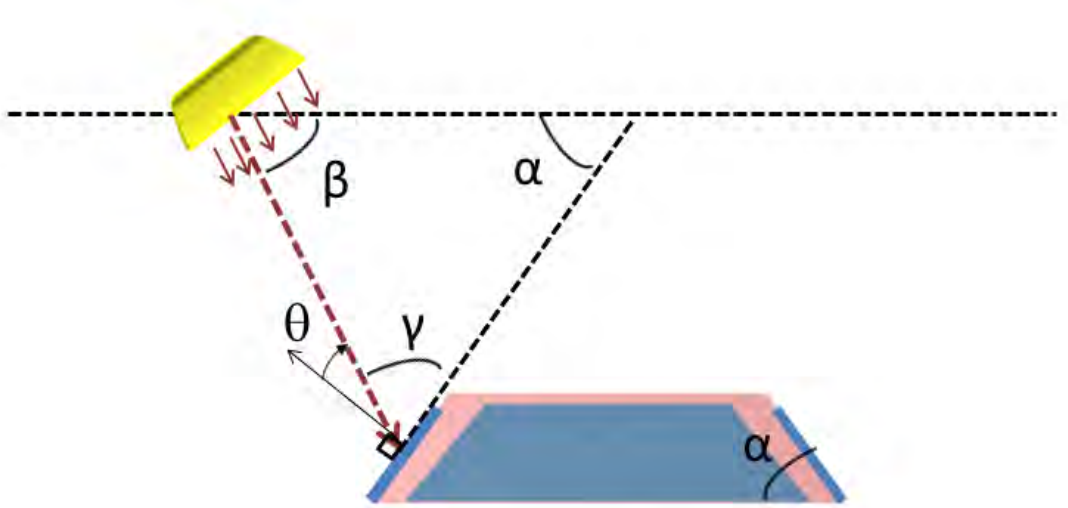

Figure 2-1: Schematic of a single pixel system with incident optical projection at an angle β from the parallel line, forms angle θ with the pyramid surface normal. Angles α β γ are trigonometrically relate.

Similarly, the principle can be extended to measurements using the relation between generated photocurrents in three adjacent facets to estimate the rotational angle ϕ in spherical coordinates to the incident light source. Starting from quad sensor estimations [35], [42], while taking into account that the incident light reaches all photodiodes as well as the photodiodes are an inclined surface,

$$R_{IP\ (adjacent)} = \frac{\left(I_{P\ (North)} + I_{P\ (West)}\right)sin(\beta + \alpha) - \left(I_{P\ (East)} + I_{P\ (South)}\right)sin(\beta - \alpha)}{\left(I_{P\ (North)} + I_{P\ (West)}\right)sin(\beta + \alpha) + \left(I_{P\ (South)} + I_{P\ (East)}\right)sin(\beta - \alpha)} \tag{2-10}$$

Where $R_{IP\,(adjacent)}$ describes a normalized ratio between photocurrents in two facets, taking into account the other facets' contribution.

$$R_{IP(next\ to\ adjacent)} = \frac{\left(I_{P\,(North)} + I_{P(South)}\right)sin(\beta+\alpha) - \left(I_{P\,(West)} + I_{P\,(East)}\right)sin(\beta-\alpha)}{\left(I_{P(North)} + I_{P(South)}\right)sin(\beta+\alpha) + \left(I_{P\,(West)} + I_{P\,(East)}\right)sin(\beta-\alpha)} \quad (2\text{-}11)$$

Where $R_{IP\ (next\ to\ adjacent)}$ describes a normalized ratio between photocurrents in two opposing facets, taking into account the other facets' contribution. The rotational angle ϕ can be estimated using:

$$cos(\phi) = \frac{R_{IP\,(adjacent)}}{\sqrt{\left(R^2_{IP\,(adjacent)} + R^2_{IP\ next\ to\ adjacent}\right)}} \quad (2\text{-}12)$$

Thus, the incident optical source's position in 2D is obtained. The computational requirements are substantially reduced, compared to other systems that rely on grids of arrays [43], [44], allowing faster response and less overall noise. There are obvious limitations arising from using a one pixel system, even though it may be sufficient in some applications. In Section 4.4, errors in estimations are discussed. As the light source approaches an inclination angle, facets fall within the shadow of light incident at an angle much lower than α, the pyramid base angle. Thus, generated photocurrent readouts jeopardize calculated ratios and consequent angle estimations.

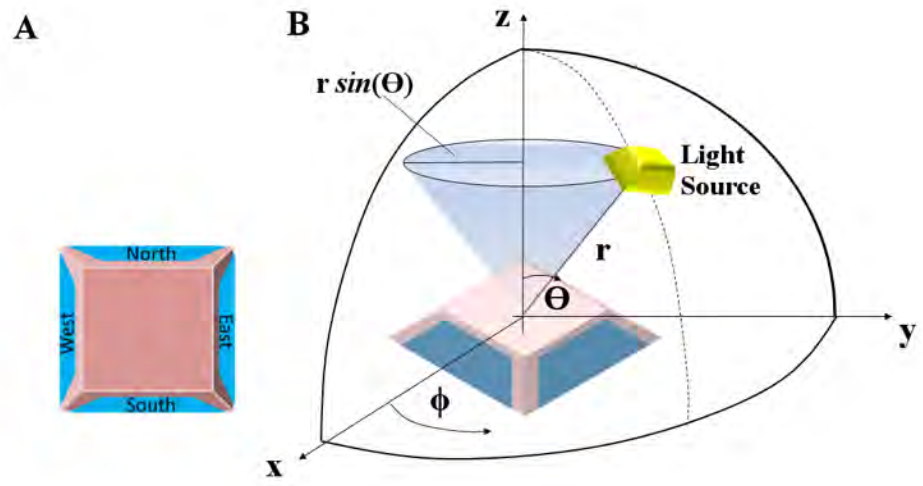

Figure 2-2: Top view (A) and side view (B) of a mesa single pixel design with a coordinate system relative to an incident light source.

In order to compensate for some of the errors, another pixel placed at distance "d" away from the first pixel is introduced, (Figure 2-3). The two-pixels system minimizes angle estimation errors, in which light that is not detectable by a facet in one of the pyramids is detectable by facets in the other pixel. In addition, the pixel system may be used to estimate the height of the incident optical source, z, thus, obtaining a 3D position of the light source.

$$z = \frac{d}{tan(\beta_1)) - tan(\beta_2)} \tag{2-13}$$

Where β_1 and β_2 are angles at which incident light is projected onto pixels 1 and 2 respectively, and d is the distance between the pixels.

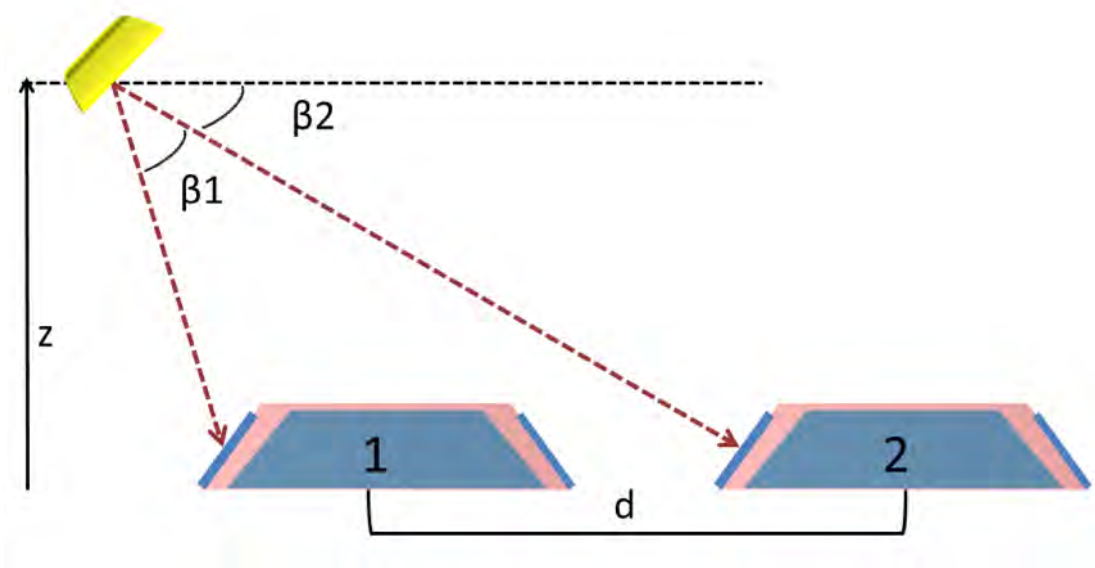

Figure 2-3: A two-mesa-pyramid system with separation distance d, the light source at height h the radiation is received at angles β1 and β2.

Therefore, the 3D distance between the incident optical source and the center of pyramid one is obtained. Introducing more pixels into the system further reduces the geometric issues that arise due to illuminations at lower angles.

2.1.2. Inverse Pyramid Design

The principles of operation for the inverted design are quite similar to the principles of operation of mesa designs discussed earlier, in which the ratio of normalized generated photocurrent is still utilized to estimate rotational and inclination angles of an incident light source for a one pixel system, and 3D for a two-pixel system, Figure 2-4.

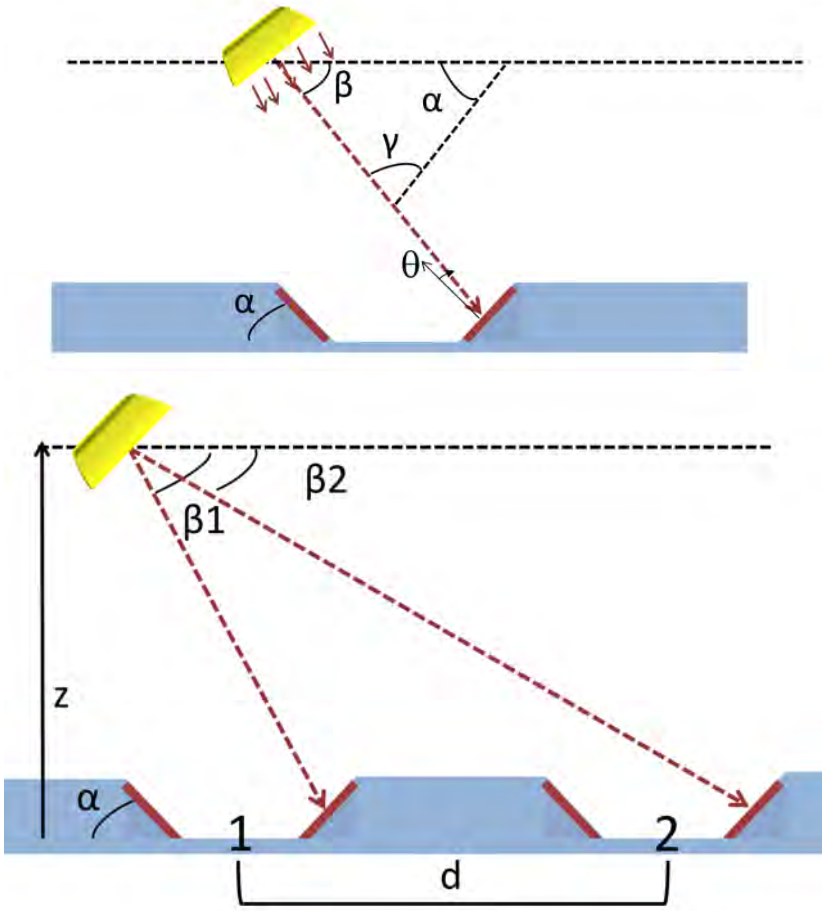

Figure 2-4: (Top) Schematic of a single inverse pixel system with an incident optical projection at an angle β from the parallel line, forms angle θ with the pyramid surface normal. Angles α β γ are trigonometrically relate. (Bottom) A two-inverse-pyramid system with separation distance d, the light source at height h the radiation is received at angles β1 and β2.

However, design limitations below a certain inclination angle θ, in which light would be blocked from reaching facets, are anticipated, as pyramids are fabricated by etching into the wafer. Figure 2-5 shows an image of an inverse pyramid design within a cylindrical coordinate system.

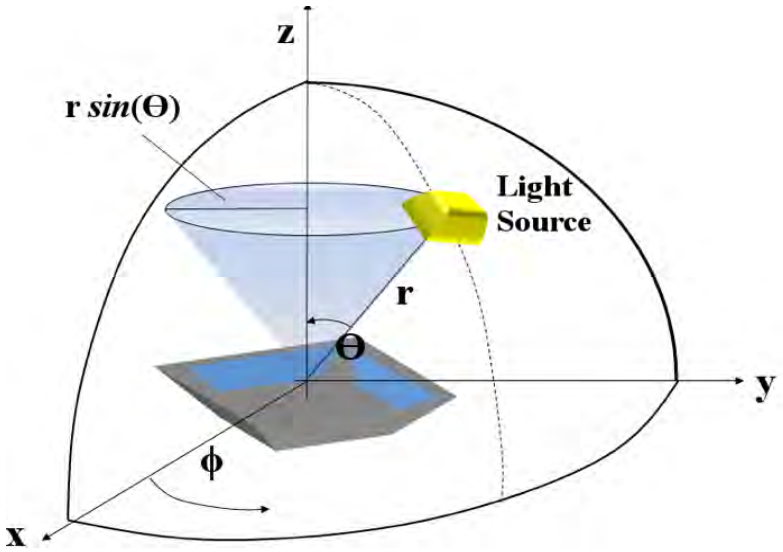

Figure 2-5: Side view of an inverse single pixel design with a coordinate system relative to an incident light source.

The inverted pyramid design may have advantages related to the manufacturing process, as producing wells requires the removal of much less material than the creation of the mesa, as low cost CMOS compatible processing is based around etching rather than additive process steps.

2.2. Macroscale Prototype

The first step taken for validating the principle of operation was to build a macroscale prototype. 3D printed designs were used to create mesa pyramids. Microfabricated devices are expected to have an angle of 54.7º, the angle formed between (111) and (100) planes in Si during anisotropic etching in alkaline solutions [45]. 3D-printed pyramids were created with pyramid base angles between 25º and 75º, as 3D printing allows for such customizability. However, in order to allow a prototyping design that can be realistically compared on a microscale, the base angle was designed to be 55º. The 3D printed mesa pyramid designs have a flat top area of 1cm x 1cm, and commercial Si based photodiodes in plastic packaging (BP104 PIN photodiode, Vishay Semiconductors) were used as the

photoconductive cells. The photodiodes were placed onto the slanted sides of mesa pyramids. The system consisted of two pyramids separated by a distance, d. Four photodiodes were used per pyramid, and one photodiode (D1) is placed on a flat surface, in order to provide reference for the rest of the photodiodes pyramid facets, Figure 2-6 [36].

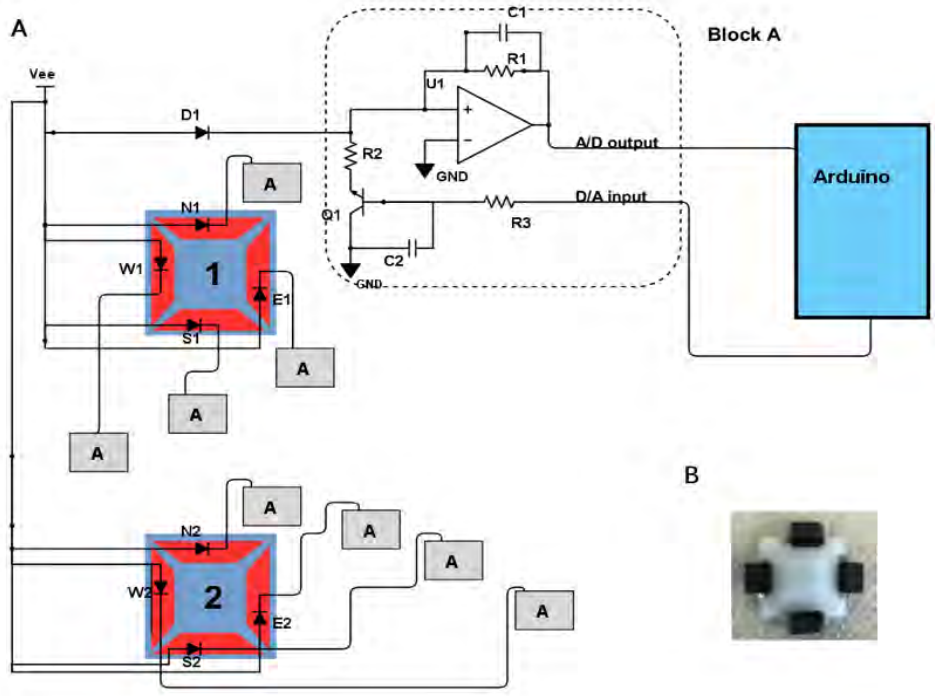

Figure 2-6: A. Schematic and circuit diagram of the overall detection setup. Photodiodes are connected in parallel through a TIA circuit (block A) to a power source Vee. One photodiode (D1) is placed on flat surface to provide reference for the rest of the photodiodes on the pyramid facets. B. Top image of the device [36] ©2016 IEEE.

Each photodiode is connected to a power source Vee at 5V and a transimpedance amplifier (TIA) circuit. The amplifier is used to convert the generated photocurrent to measurable voltage outputs, while an NPN bipolar junction transistor (BJT) is used to amplify the signals. Capacitors C1 and C2 are used to decrease the output noise as is typical for photo diode detector circuits and to facilitate the BJT-control of input current

respectively. The Arduino microcontroller is used to read the voltage outputs from the photodiodes as well as to provide a D/A input for D1, which is used to filter out background light. Initially, Arduino Due with Arduino IDE were used, however, graphing outputs in real-time and further analysis of acquired data proved to be a challenge using the limited capabilities of the Arduino. Substituting an Arduino Mega2560 allowed an easier integration with MATLAB®, in order to analyze acquired data and display outputs in real-time, (Figure 2-6) [36].

Generated photocurrents at the facets of each pixel are measured, and the generated I_P ratio of two opposite facets of both pyramids are calculated, the ratios are then used to estimate the incident angle of the light source β and, consequently, the inclination angle. At each pixel, I_P ratios of the West and East facets of the pixel were calculated as well as the I_P ratio of the North and South facets. Since there are slight variations in photodiodes' characteristics, the pixel measurements are calibrated by normalizing each facet's I_P measurement to its I_P measurement at inclination angle 90º with respect to the pyramid base, at a position right on top of the center of the pyramid. Thus, a photocurrent ratio equal to one indicates that the optical source is at a position equidistant from all facets, that is, at a location above the center of the pyramid. However, conditional logic statements need to be included during signal processing steps, such that the pixel distinguishes the relevant facets ratios for angle calculations. For example, when one of the ratios is reading a value close to one, while the other ratio indicates an error in

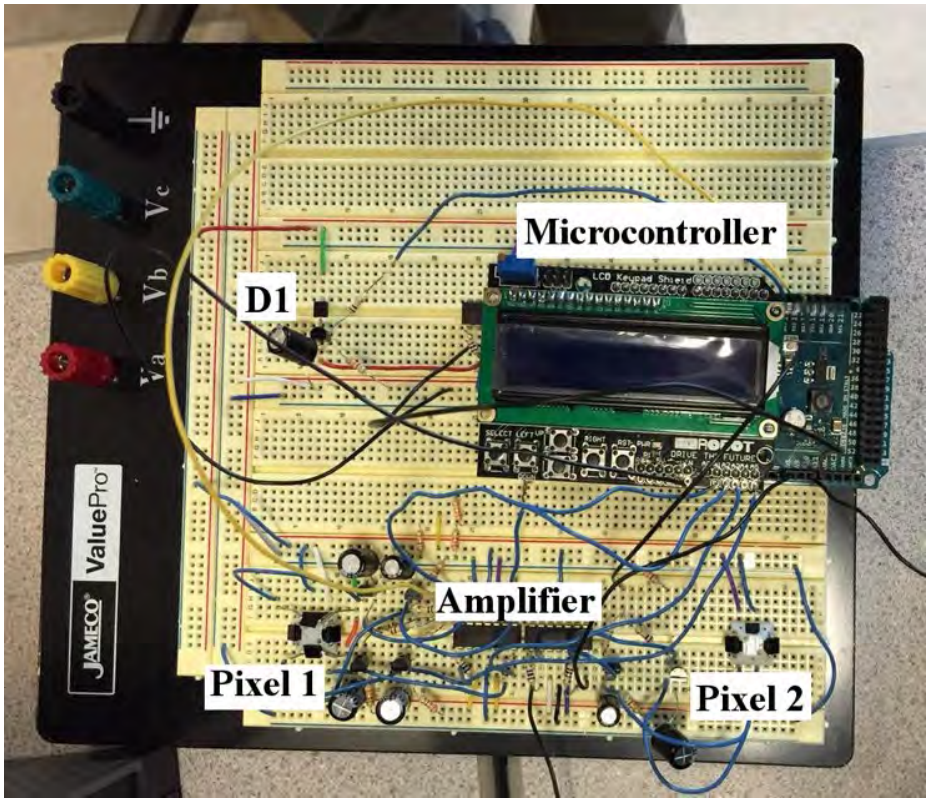

Figure 2-7: An image of the prototype device including the TIA circuit.

readings, mostly due to one of the facets not receiving enough illumination, the later ratio is disregarded, and is deemed non-relevant for the inclination angle calculation. The signal processing step is essentially a computationally filtering step to determine relevant readings before angle estimations are calculated. Concurrent to the inclination angle calculations, rotational angle calculations are determined using similar conditional statements. Figure 2-7 shows an image of the original macroscale prototype design including the TIA circuit. At a later stage, shorter wires were used and component rearrangements were made on the circuit board in order to not have any components or long wires acting as obstacles in the path of incident light. The circuit board was placed inside a black box (Thorlabs) designed to reduce the effects of unwanted background light that may be present in the environment. A single focussed LED was used to project light

onto pixel 1 from several locations within the box. The rotational angle ϕ is estimated from several locations. The averages of measurements at each point are compared to the real values, and are used to describe the rotation of the source of radiation about pixel 1. The correlation coefficient value is found to be 0.9986, indicating that the measured and real values are very close to each other, Figure 2-8 [36].

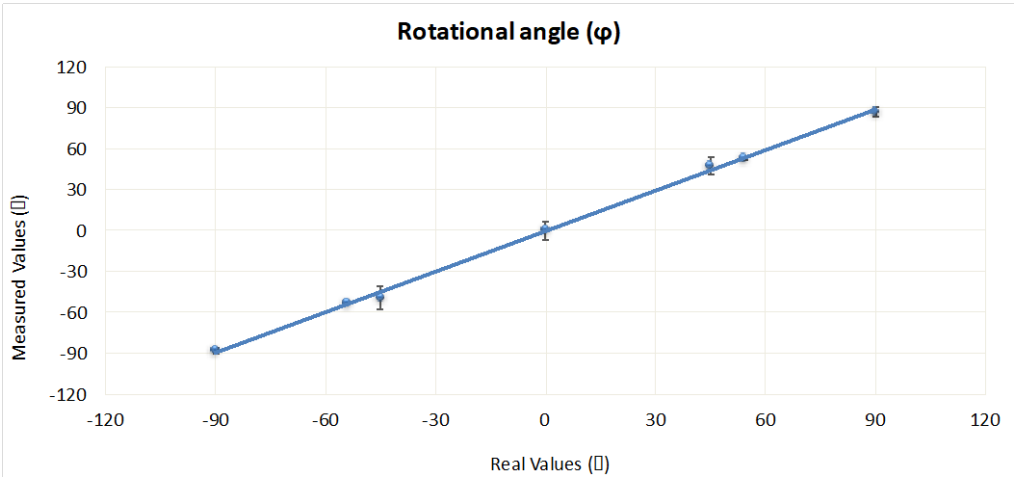

Figure 2-8: Estimation of the rotational angle ϕ of the light source with respect to the system of two mesa pyramids [36] ©2016 IEEE.

The 3D radius is estimated from several locations. The averages of measurements at each point are compared to the real values and are used to describe the 3D radius between the source of radiation and pixel 1. The R^2 value is found to be 0.887, indicating that the measured and real values are very close to each other, and the model can be used to estimate the position and spatial proximity of a light source, Figure 2-9. Using the single pixel's 3D design, it has been shown that photocurrent readouts, relative to intensity, at each facet can be utilized to estimate spatial proximity information about an incident light source in 2D.

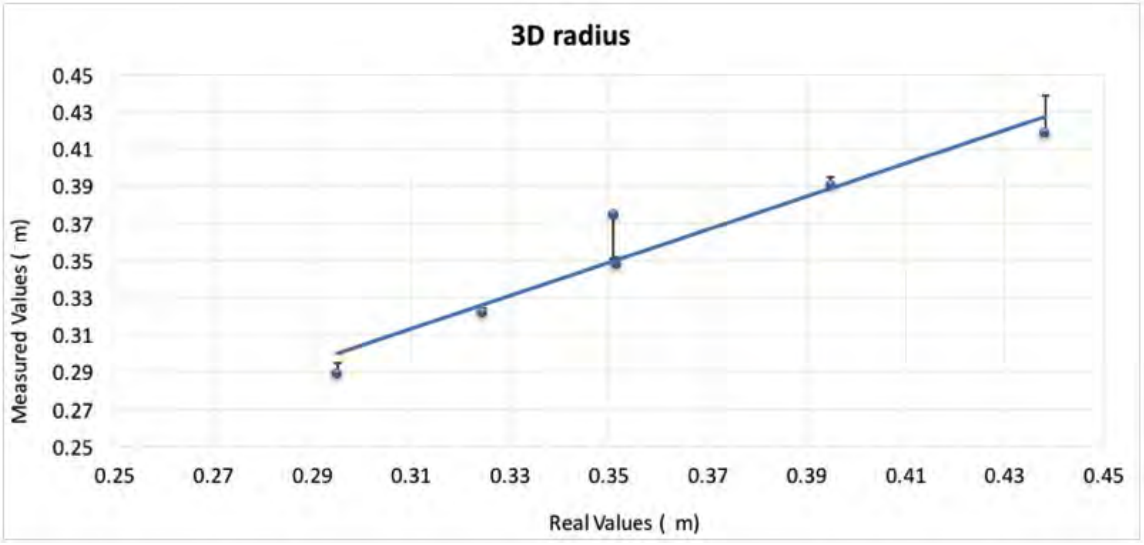

Figure 2-9: Estimation of the distance (3D radius) between the light source location and the centre of pyramid one [36] ©2016 IEEE.

Some limitations may arise when fabricated in Silicon in which some facets may not be receiving enough light, due to the facet falling in the shadow of the pyramid structure in the case of the mesa pyramid, or the wafer structure gets in the way of light due to the inverse pyramids being etched into the wafer. In order to decrease some of the limitations, other pixels can be added, in which if light doesn't get properly detected by one pixel's facets, it would be detected by other pixels' facets or by utilizing facets in more than one pixel, as illustrated here by results from the 3D printed prototypes. Another advantage arises from using a system which has more than one pixel, as the system can be used to estimate the height from which the light was projected. Once the height is obtained, the position of the light source can be estimated in 3D. Using a 3D printed design of a two-pixel system and commercial photodiodes, along with the hierarchical computation system of the Arduino MCU and MATLAB® on a PC, position estimations of a light source in 3D can be performed in real time are demonstrated.

3. Microfabrication of Mesa and Inverse Single Pixel Designs

In this chapter, a detailed fabrication process in presented, in which mesa and inverse pixel designs of various pyramid dimensions and depths are created while embedding p-n junctions onto pyramids' facets. The pn-junctions act as photodiodes, which are fabricated by diffusing phosphorus onto portions of the surfaces of four-sided mesa and inverse pyramids in p-type silicon substrate.

3.1. Overview of Fabrication Design

The 3D sensor structures are designed to include planar electrical circuits, for easier packaging, where the circuits are built into the sides of the pyramids. Pyramids, of top sizes ranging from 100umx100um to 200umx200um and depth of 15-50um, are etched from the Si substrate.

Further etching the pyramids to produce smaller pyramids sizes rendered the depth of the pyramids, and p-n regions, too small for uniform diffusion areas across all facets, leading to less accurate readings. In addition, producing pyramids with larger diode regions included fabricating larger area-sized pyramids, which could have led to area sizes comparable to arrays of sensors.

The pn junctions are created by diffusing phosphorus into the sides of the pyramid facets in Si, and just enough of the base of the pyramid in order to create discrete regions that can be easily connected to the planar circuit.

The main steps of the process flow are shown in figure 3.1:

1) A-C: Selective etching of p-type Si wafer using alkaline anisotropic etchants in order to create mesa and inverse pyramids with various dimensions and depths.

2) D: Utilizing spray coating deposition of photoresist to uniformly coat and pattern the 3D structures

3) E and F: Selective phosphorus doping of the angled facets.

4) G: Deposit metal contacts to fabricate functional devices.

Clearly, the 3D electronics complicates the processing considerably. In outlining the steps above, there remain areas where one step either complicates or eases the demands on the next step. A similar process flow of the fabrication process developed is also shown in Figure 3-1 for inverse pixel designs.

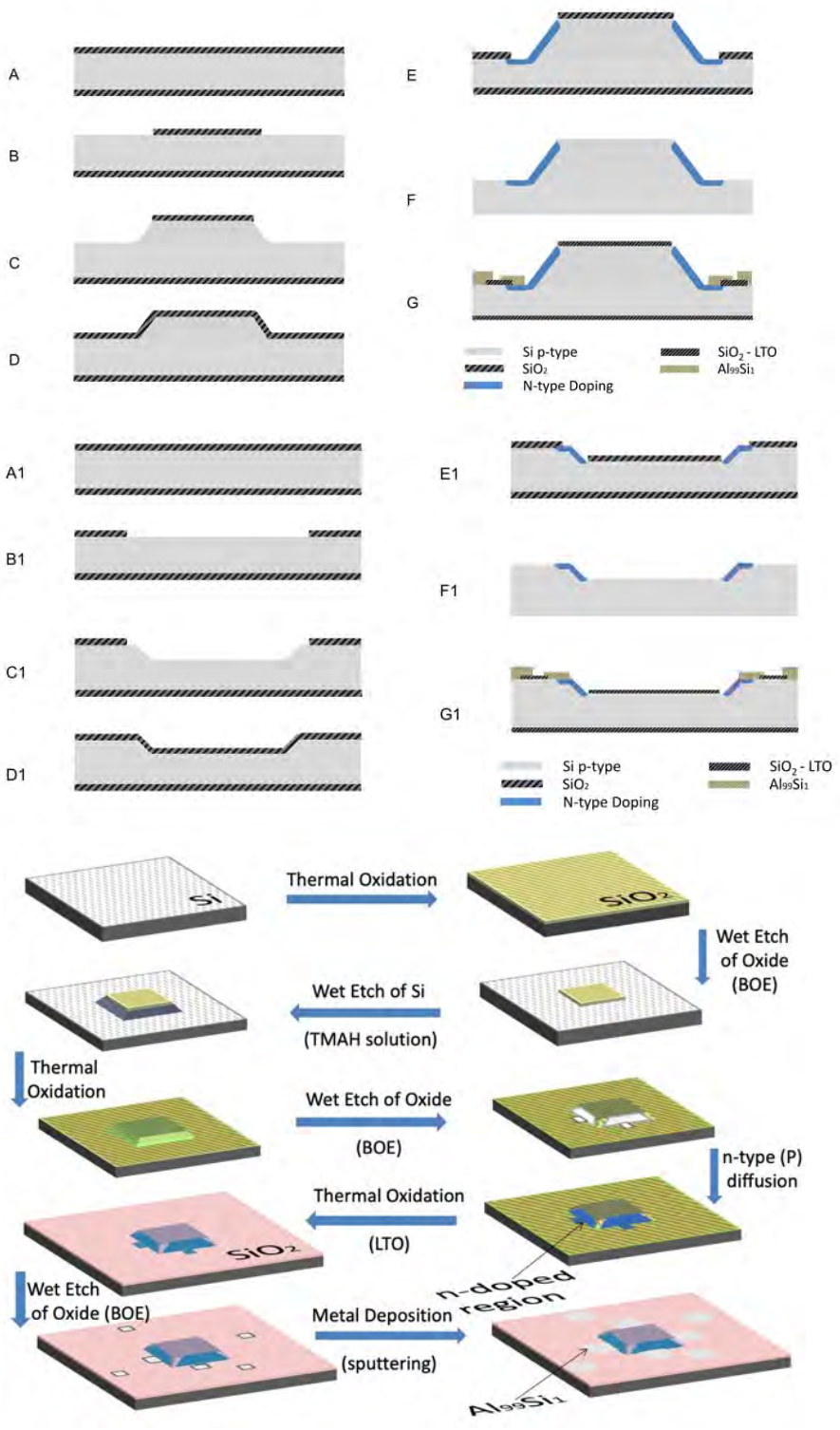

Figure 3-1: (A-G) Process flow of the fabrication of a mesa pixel vector light sensor design. (A1-G1) Process flow of the fabrication of an inverse pixel vector light sensor design. Bottom. Process flow in 3D.

The fabrication process is a 4-mask level process which includes patterning and selective etching processes to create p-n regions on the facets of the pyramids. Lithography masks are designed in a way to support various dimensions and depths of mesa and inverse device designs on a single substrate. This process has the potential to provide high yield fabricated devices, with the inverted pyramid design having the potential to be included in a conventional CMOS compatible process. Process steps and details of each step are described in following sections of this chapter and summarized in Appendix A.

All the process steps and design rules of the fabrication process are developed and optimized by the author at the Institute of Micromachine and Microfabrication Research (IMMR) facility in School of Engineering Science and 4D LABs at Simon Fraser University.

P-type <100> silicon wafers were used as substrates, summarized in Table 1. The resistivity of the wafer was measured to have an average of 1.45 Ωcm using 4-point probe measurement, which corresponds to a background dopant concentration of ~ $1x10^{16}$ cm^{-3} for p-type silicon.

Table 1: Characteristics of silicon wafers used as substrates.

Diameter [mm]	100
Substrate thickness [µm]	500-550
Type/ Orientation	p-type/ 100
Background Dopant	Boron
Background dopant concentration [cm^{-3}]	~ $1x10^{16}$
Substrate resistivity (average) [Ω-cm]	1.45

3.2. Fabrication of symmetric pyramidal mesas in Si

3.2.1. Anisotropic etching

Anisotropic etching of silicon is a crystal orientation dependent type of etching, in which Si planes are etched at different rates. Wet etching aqueous solutions including inorganic hydroxides of alkali metals solutions, such as KOH, NaOH, and organic ones such as Ethylene Diamine Pyrocatechol (EDP) and Tetramethyl ammonium hydroxide (TMAH) are among the popular etchants. The use of these etchants becomes important when wafers contain CMOS integrated circuits. While KOH offers very high selectivity in etching rates, 1:600:400 for (111):(110):(100) planes, as well as being able to be used with silicon dioxide etching masks, the presence of alkali metal (potassium, K) makes the solution completely incompatible with MOS or CMOS processing as it may introduce mobile potassium ions into the silicon dioxide. While EDP offers high selectivity to silicon dioxide and displays a selectivity ratio of 17:1 for the (100):(111) planes, it is highly corrosive and carcinogenic. On the other hand, TMAH presents a 37:1 selectivity between (100) and (111) planes in Si and excellent selectivity to silicon dioxide and nitride masks, as well offers MOS/CMOS compatibility, as the solution lacks alkali metals, such as Li, Na, and K. Depending on crystal orientation, the (111) planes form side-wall angles generally at 54.74º with the wafer's (100) silicon surface. However, etching rates for planes are extremely dependent on the aqueous solutions' chemical composition, concentration, and temperature of the etchant solutions used. Eventually, the choice of etching solution is conditioned by many factors including etching rate, anisotropy, selectivity to mask materials, such as silicon dioxide, silicon nitride, or metals, and surface roughness after etching [45]–[49].

In low concentrated KOH solutions, the etch rates for high-indexed planes is low. Increasing KOH concentration dramatically decreases surface roughness, along with increasing temperature, the addition of isopropyl alcohol (IPA), and increased agitation. However, increased KOH and IPA concentrations as well as increasing temperatures causes an increase in the etching rate for planes with crystallographic orientation (221), (331), and (441), as well as decreases the etching rate of (100) plane. Also, at sufficiently high KOH concentrations, the etching rate in pure KOH solutions is lower than KOH solutions with added IPA [45], [50], [51].

In TMAH solutions, with IPA added TMAH and IPA concentrations tends to reduce the etching rates in all planes, and used along with increasing temperature, decreases etched surface roughness. In addition, adding IPA to TMAH reduces undercutting as well as found to produce (100) and (110) planes, with excellent surface smoothness for (110) etched planes. However, the increase in TMAH concentration results in an increase in etching rates of (331) planes [48], [52], [53].

For the purposes of etching our pyramid designs, here the factors that mattered most were etching selectivity to planes and to silicon dioxide, which was used as a mask, as well as surface roughness post etching. There a KOH process was adopted. Initially, KOH, 5M (30%wt) KOH concentration at 80 ºC was attempted, without adding IPA. Adding IPA to 5M (30%wt) KOH concentration with 5% IPA at 80 ºC proved to achieve satisfactory smoothness of the etched surface, as demonstrated in theory [48], [50]. KOH solution (5M (30%wt) KOH concentration at 80 ºC) was used to etch Si anisotropically using a thick layer of oxide, 2.5 µm, as a mask. The KOH solution was prepared by dissolving KOH pellets in DI water at a ratio of 30g for 1000mL DI water. The 30% KOH solution has a theoretical etching rate of 1.1µm/min for etching Si in the <100> direction, and 7.7nm/min

for etching thermal oxidation SiO2 at temperature of 80 ºC [46]. The etching rate was measured by etching at different times (55min and 95mins) by placing 2 wafers in the solution and removing one of the wafers at t=55mins. Figure 3-2 show that Si has etched anisotropically to get slanted sides. Si is etched in the <100> and <111> planes at different rates, about 100:1 ratio [45]. However, severe undercuts are present as other planes are also etched. The oxide layer can be seen hanging from the corners of where once was a flat wall indicating that there was etching in the <111> plane.

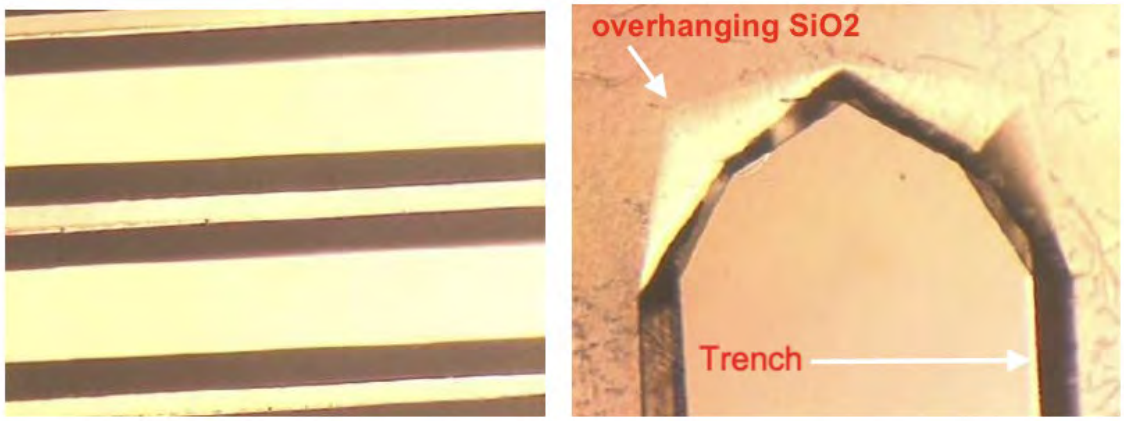

Figure 3-2: Optical images showing anisotropically etched Si using KOH for 55minutes at T=80 ºC. An Oxide layer can be seen overhanging on the sides of the etched areas.

SEM images show the oxide layer hanging, as well as how feature spacing affects the etch rate of Si,

Figure 3-3. The feature spacing effect on Si etching is more evident in Figure 3-4, where Si has been etched for t=95mins, sufficient uniform spacing between features has a higher etching than when features are closer to each other. There were no profilometry measurements to present surface roughness, however, etched walls appear to have been defected.

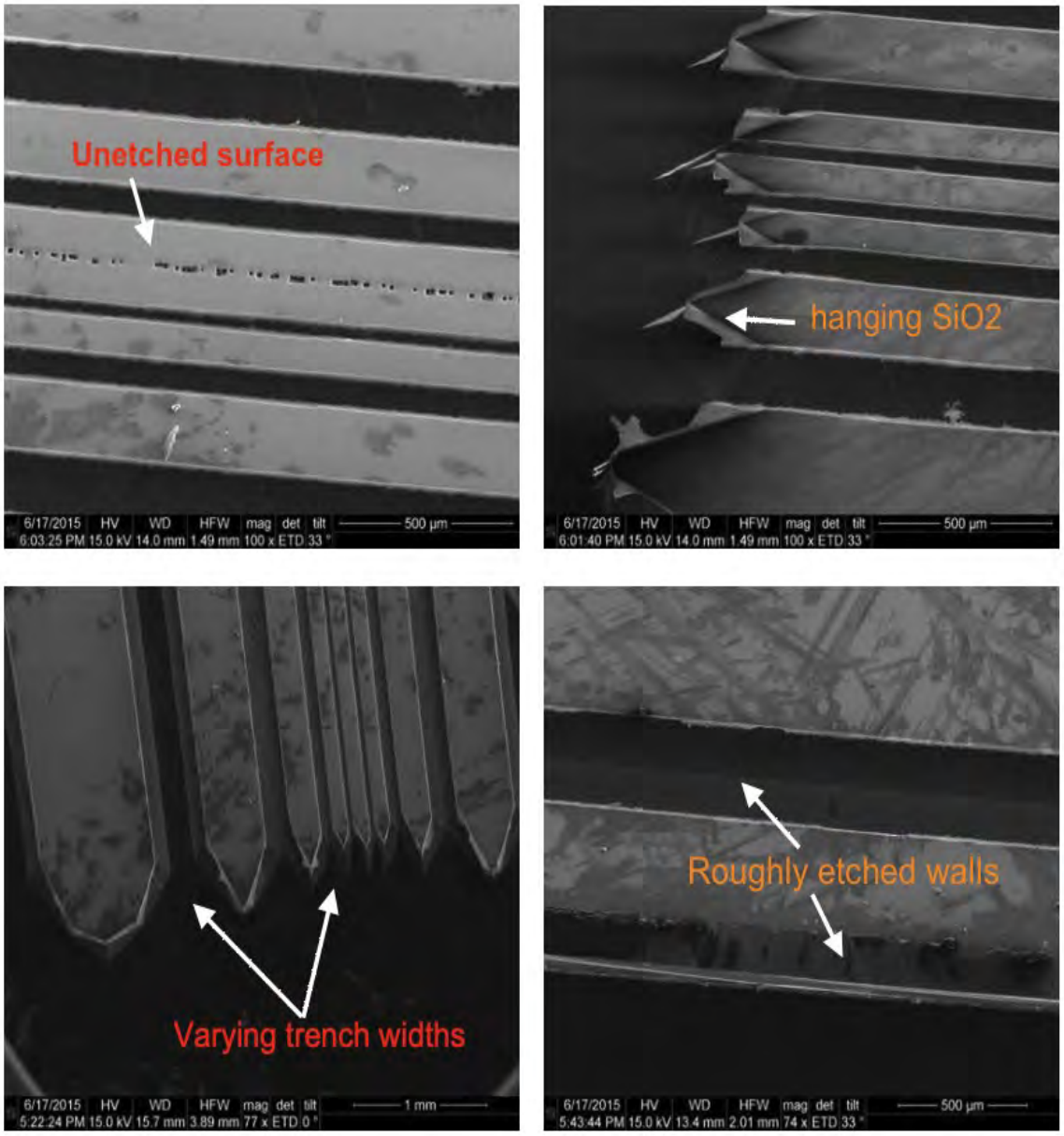

Figure 3-3: SEM of Si etched for 55mins in KOH solution at 80 ºC. SiO2 layer still shown hanging, with Si anisotropically etched from underneath (undercuts). The feature spacing causes Si to etch more rapidly where there is more spacing between the features.

Spin coated S1813, deposited using a spin coater, and spray coated S1813, deposited by a manual spraying method using a spray bottle, have an average thickness of 1µm, with the spray coating layer having a rougher surface. The spin coated layer has

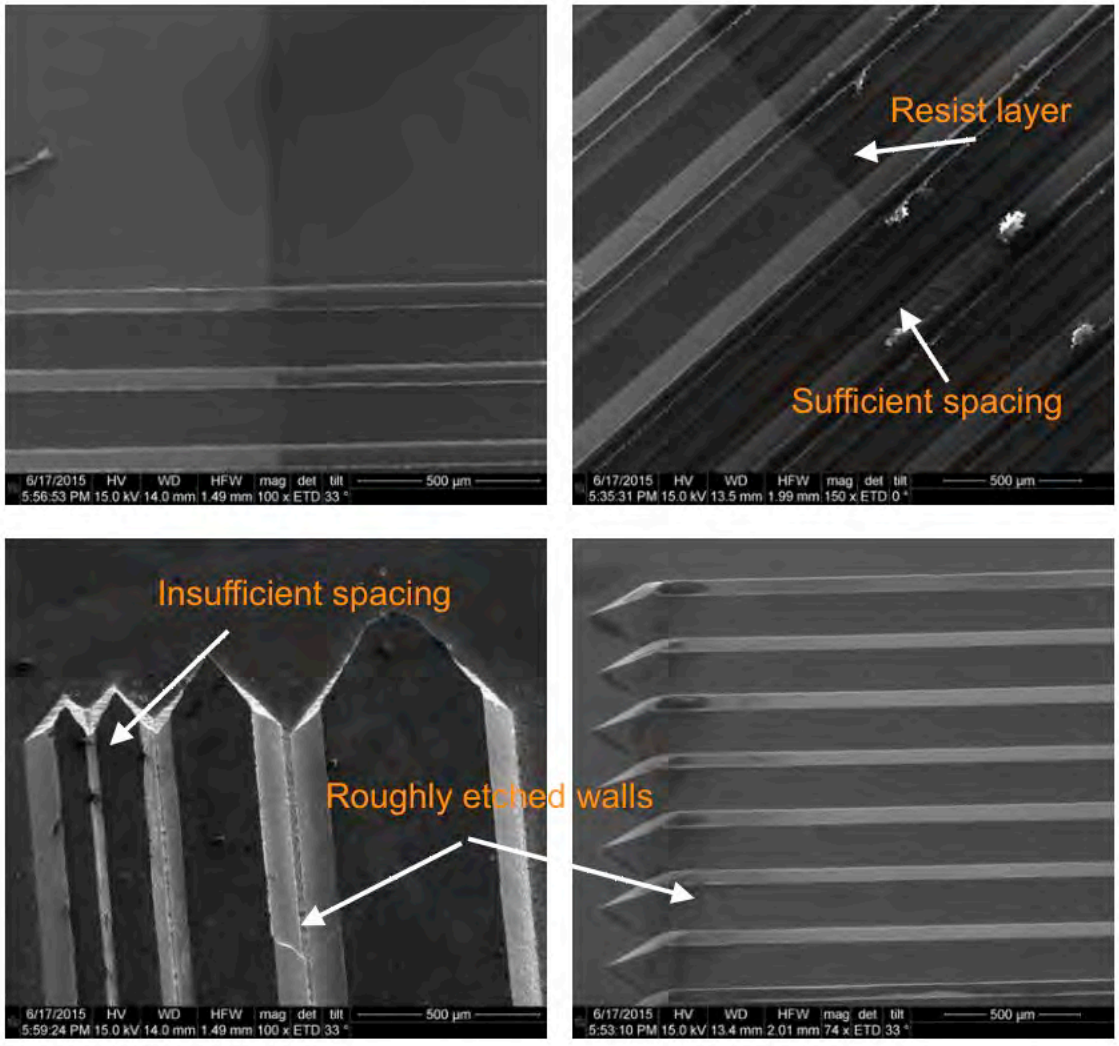

Figure 3-4: SEM images of Si etched for 95 mins in KOH solution at 80 ºC. Si is etched deeply further than the wafer taken out at t=55mins. Sufficient uniform spacing between features has a higher rate of etching than when features are closer to each other. The top images have a layer of deposited photoresist.

issues covering the whole 3D structure, as can be shown in Figure 3-4, as photoresist does not get deposited at the base of the slanted regions. There will be a more detailed discussion about photoresist deposition in a later section.

3.3. Mask Design to Create Pyramid Structures

During the mask design stage, it is essential to design patterns in such a way that the patterns are aligned with respect to the crystallographic directions on the wafer surface, as the alignment plays a significant role in controlling final etched profiles during wet etching processes. A small degree of misalignment may cause planes not intended to be etched to start etching, resulting in changes in etched regions dimensions and undercutting [54], [55]. In these designs, the primary flat is employed as reference, thus, the primary flat is aligned with the bottom of the container during the wet etching process. In addition, undercutting at convex corners was also taken into account.

The mechanism of undercutting of convex corners emerges due to some planes etching faster than others during the anisotropic etching process. Depending on the etchant and the etching conditions, several planes, such as {2 1 1}, {2 2 1}, {3 3 1}, and {4 1 1} tend to also etch at the corners of structures as {100} / {110} planes are etched away, thus, compromising the intended etched structures. As an approach to prevent the undercut at convex corners during the wet anisotropic etching process of Si, corner compensation structures are introduced at the corners of the designed structures. There were several designs that have been researched, starting with simple square designs at the corners to complex structures, taking into account the intended depth of the final etched structures and the possible etching of undesired planes. Several corner

compensation designs have been studied to prevent undercutting and realize desired convex corners [54]–[57].

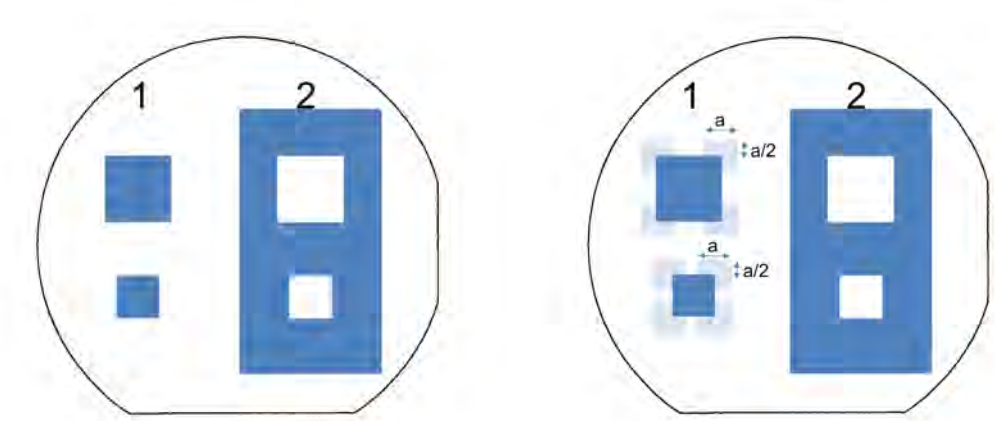

Figure 3-5: Mask design for anisotropic wet etching step to create mesa and inverse pyramids of several dimensions. (Left) mask design without corner compensation structures for mesa pyramid design. (Right) mask design without corner compensation structures mesa pyramid design.

By integrating corner compensation structures into the design of corners, the structures protect the corners against unwanted etching of planes that might affect the desired structure. Since the etching process initiates first at the added structures, the corners of the desired structures remain protected until the corner compensation structures are fully etched. Corner compensation structures are designed in such a way that they are completely etched away by the time the desired structure depth is realized. In the design, the mask is designed in such a way that both mesa and inverted pyramid structures would be created upon the wafer undergoing a wet etch process, as shown in Figure 3-5. Initially, corner compensation structures for the mesa pyramid design were not used, as the desired depth of etched structures of 15 µm would not have been likely to cause undercutting at the convex corners, as suggested in [54]. The corner compensation structure used is a square with side ‘a’, where the center of the square is at the center of where the desired angle would be. As discussed in [57], the square side is related to the desired etch depth, H, by:

$$a = \frac{H}{0.544} \tag{3-1}$$

On the other hand, corner compensation structures are not necessary for cavities in which (1 1 1) crystallographic planes are etched to form concave corners, as wet anisotropic etchants such as KOH, EDP and TMAH have a very slow etch rate for the (1 1 1) silicon planes. Thus, the limiting etched structure at the concave corner is bounded by the slowest etching planes [58].

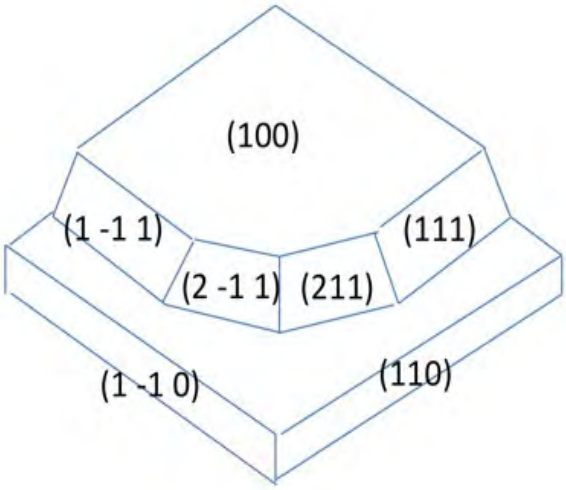

Figure 3-6: Appearance of other etching planes at the convex corner during anisotropic etching.

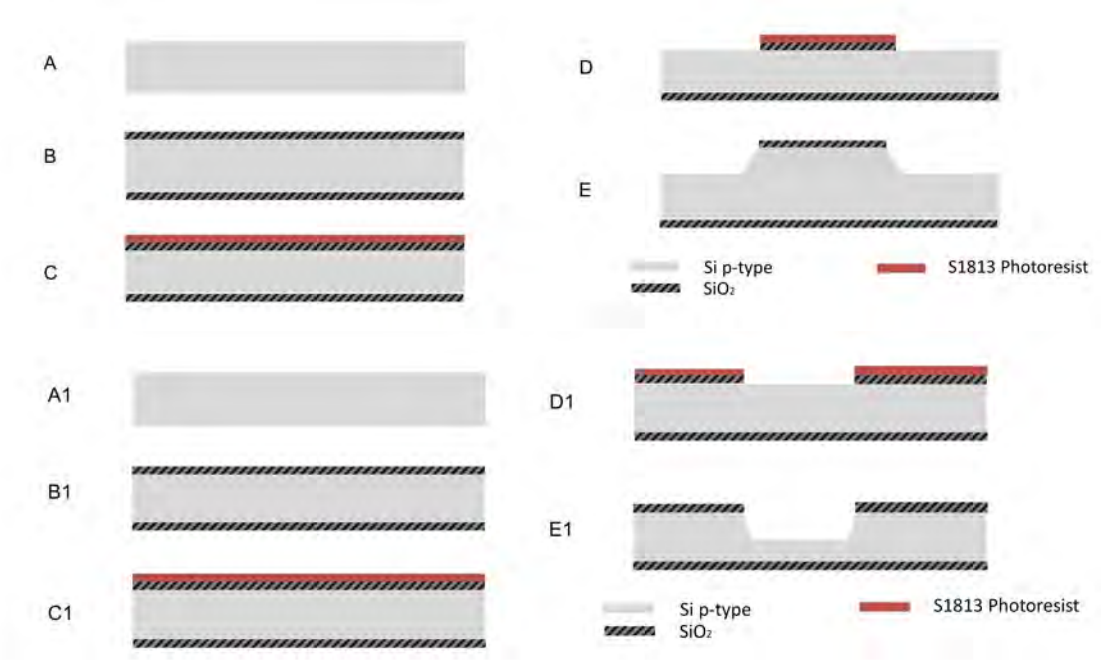

Figure 3-7: (A-E) Process flow of etching mesa pyramids in Si. (A1-E1) Process flow of etching inverse pyramids in Si. Masks are used in lithography steps.

P-type Si wafers are used as substrates. An RCA cleaning step of p-type Si wafers is used to clean the substrates from metal and organic contaminants that may hinder the growth of a uniformly oxide layer. Following the cleaning step, wet thermal oxidation is used to grow a layer of silicon dioxide. The wafers are placed in a furnace at a temperature of 1100°C for 55 minutes in order to grow ~550 nm layer of oxide on each side of the wafer. The oxide layer's thickness is chosen to be sufficient enough to withstand the KOH solution and act as a mask layer during the anisotropic etching step, as the 30% KOH solution has a theoretical etching rate of 7.7nm/min for etching thermally grown SiO2 at etching temperature of 80°C. The oxide layer should also withstand etching using a TMAH based solution [46].

The top oxide layer is patterned with the first photomask using photolithography, Figure 3-5. Shipley S1813 positive photoresist, an ultraviolet (UV) light-sensitive polymer,

is spin coated on the flat wafers at 3000 rpm for 35 seconds. The wafers are then soft baked at 110°C for 1 minute on a hotplate so that the photoresist layer hardens and does not stick to the photomask during the exposure step. Since the photoresist used is a positive one, the chemical structure of the photoresist changes so that UV light exposed regions become more soluble when placed in a developer solution, while unexposed regions polymerize and become difficult to remove in a developer solution. MF319 developer is used to wash away exposed photoresist regions while the wafer is agitated for 1 minute, and the remaining photoresist pattern acts as a resist layer protecting the underlying oxide layer from getting etched. Following the exposure step, using a mask aligner, the wafers are hard baked at 115°C for 2 minutes on a hotplate. Transene Buffered Oxide Etchant (BOE) is then used to etch away the oxide layer at the non-photoresist protected regions on the wafer. Following the oxide etch step, the photoresist layer is stripped away in acetone, followed by an IPA and DI water rinse. Thus, a copy of the photomask pattern is translated onto the oxide layer. The wafers now are then placed in an anisotropic etching solution in order to create mesa pyramid structures.

3.3.1. Results: Etching with KOH and KOH+IPA solutions

Initially, 30%wt KOH solution was used for anisotropic etching, where KOH pellets in DI water at a ratio of 30g for 1000mL DI water to prepare a 30%wt KOH solution. Using a hotplate, the solution is brought to a temperature of 80 ºC. The wafer is then placed inside the solution where the primary flat is aligned with the bottom of the container. The orientation in which the wafer is placed inside the etching solution is essential as discussed in the earlier section. Optical images, Figure 3-8 A-C, show extensive undercuts at the convex corners of features, as well as the rough surface obtained following the etching step. Profilometery analysis indicates that etched surface is very rough with an average

roughness of 5.58 µm when the etched depth is about 15 µm, and that the roughness distribution is very non-uniform in some regions, Figure 3-9. The etch rate was calculated to be 0.60 µm/min.

Then, 5% IPA + 5M KOH solution was then prepared and attempted. Optical images, Figure 3-8 D-F, show the surface roughness is still present, however, the structure is realized with minimal undercutting at the convex corners. Profilometery analysis indicates that the surface roughness decreased when IPA was added for etched surfaces, however, the surface is still very rough with an average roughness of 3.96 µm when the etched depth is about 15 µm, Figure 3-9. The etch rate was calculated to be 0.53 µm/min. The decrease in etch rate was expected, as discussed in the previous section.

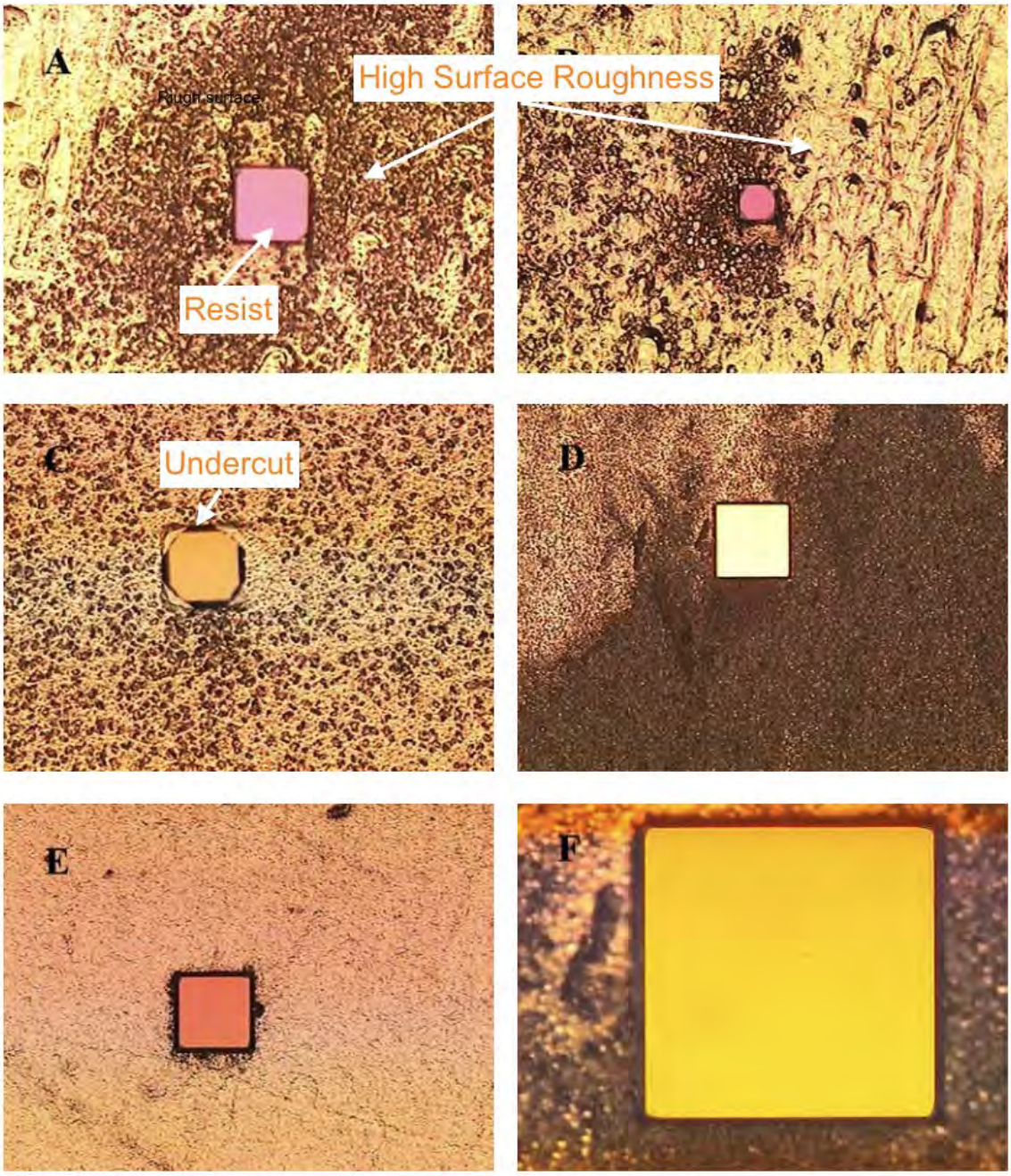

Figure 3-8: Optical images of samples etched with 30%wt KOH solution (A-C). Etching created very rough surfaces and over etching in features, especially around corners. 30%wt KOH + 5% IPA solution (D-F) reduces surface roughness and over etching. Pyramids dimensions in A-F are 50um x 50 um.

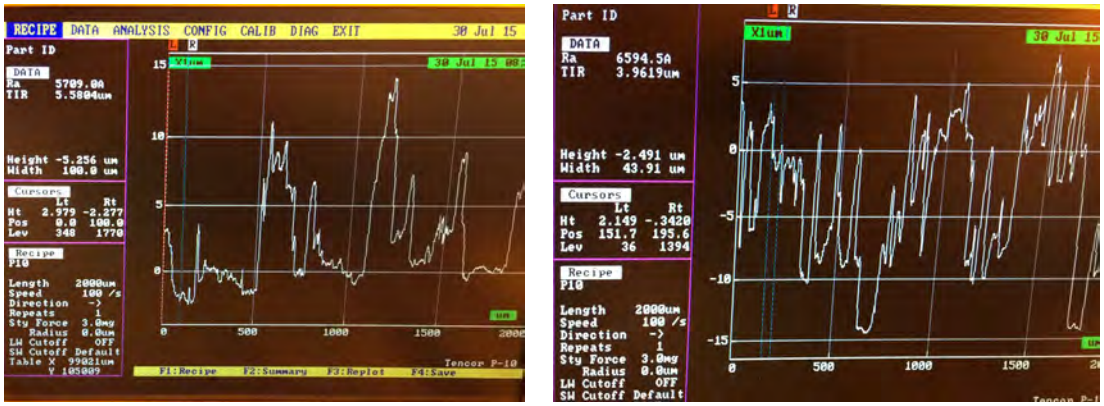

Figure 3-9: Profilometry measurements of samples etched with 30 wt% KOH solution with an average roughness of 5.6 µm (Left), and 30 wt% KOH + 5% IPA solution with an average roughness of 3.96 µm (Right).

3.3.2. Results: Etching with TMAH + IPA Solutions

As a result of the KOH based etching solutions, TMAH based etching solutions was used instead. 25% TMAH solution with 10% IPA added was used as an anisotropic etching solution. The samples were etched at 90 °C to realize structures of depths of 15 µm and 25 µm at the experimental etch rate of 0.588 µm/min, Figure 3-10. Profilometery analysis, using Bruker Dektak XT profilometer, indicates that the surface roughness decreased significantly to less than 0.7 µm, however, over etching at convex corner at 15 µm depth is evident, while over etching is a lot more significant at 25 µm depth, Figure 3-11. Thus, a new mask design with square corner compensation structures was used, Figure 3-5.

Mesa and inverted pyramids are realized after Si is etched using TMAH+IPA solution and the layer of oxide is stripped using BOE. The square corner compensation structures are used for the mesa structures, can be seen in Figure 3-12. No compensation is required for inverted pyramids.

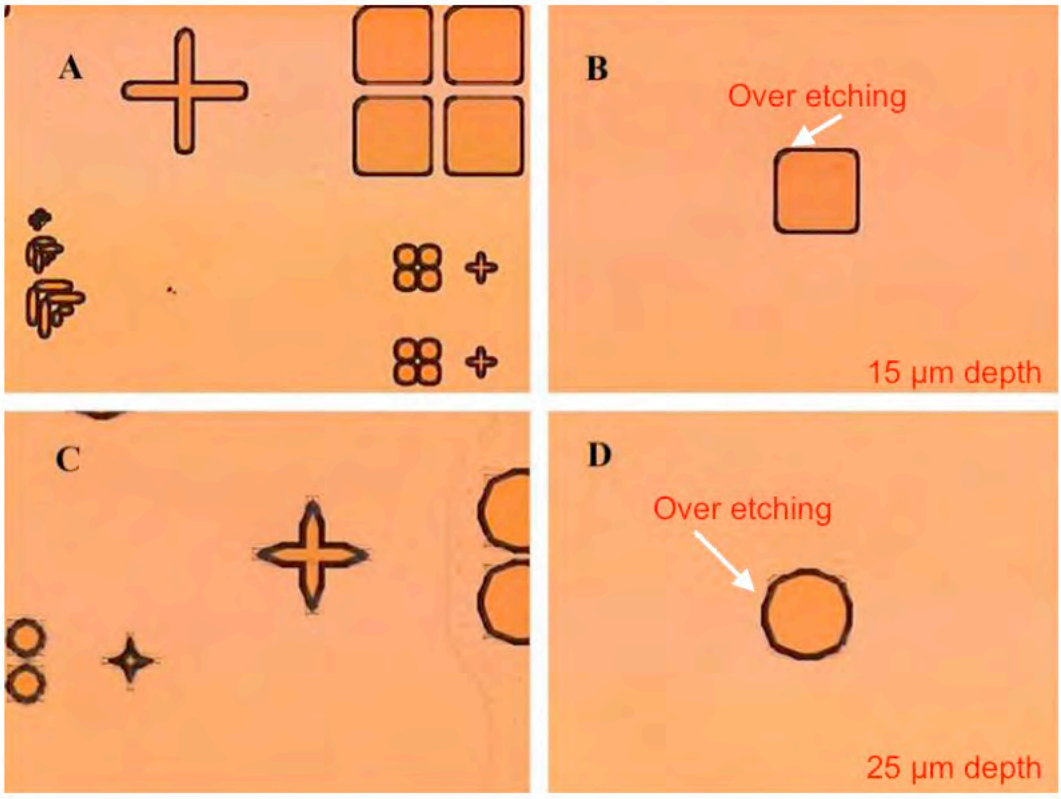

Figure 3-10: Optical images of samples etched with 25%wt TMAH+10%IPA solution at 90 °C to realize structures of depth of 15 µm (A-B) and 25 µm depth (C-D). Over etching at convex corner at 15 µm depth is starting to appear, over etching is more significant at 25 µm depth. Alignment features in A are 1um, 2um, and 5um widths for the L-shape features.

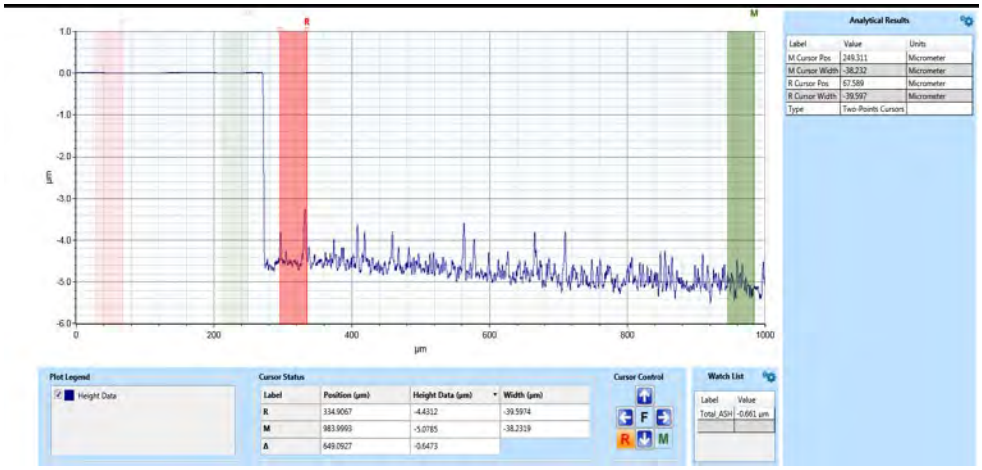

Figure 3-11: Profilometry measurements of samples etched with 25% TMAH+ 10% IPA solution with an average roughness of 0.661 µm.

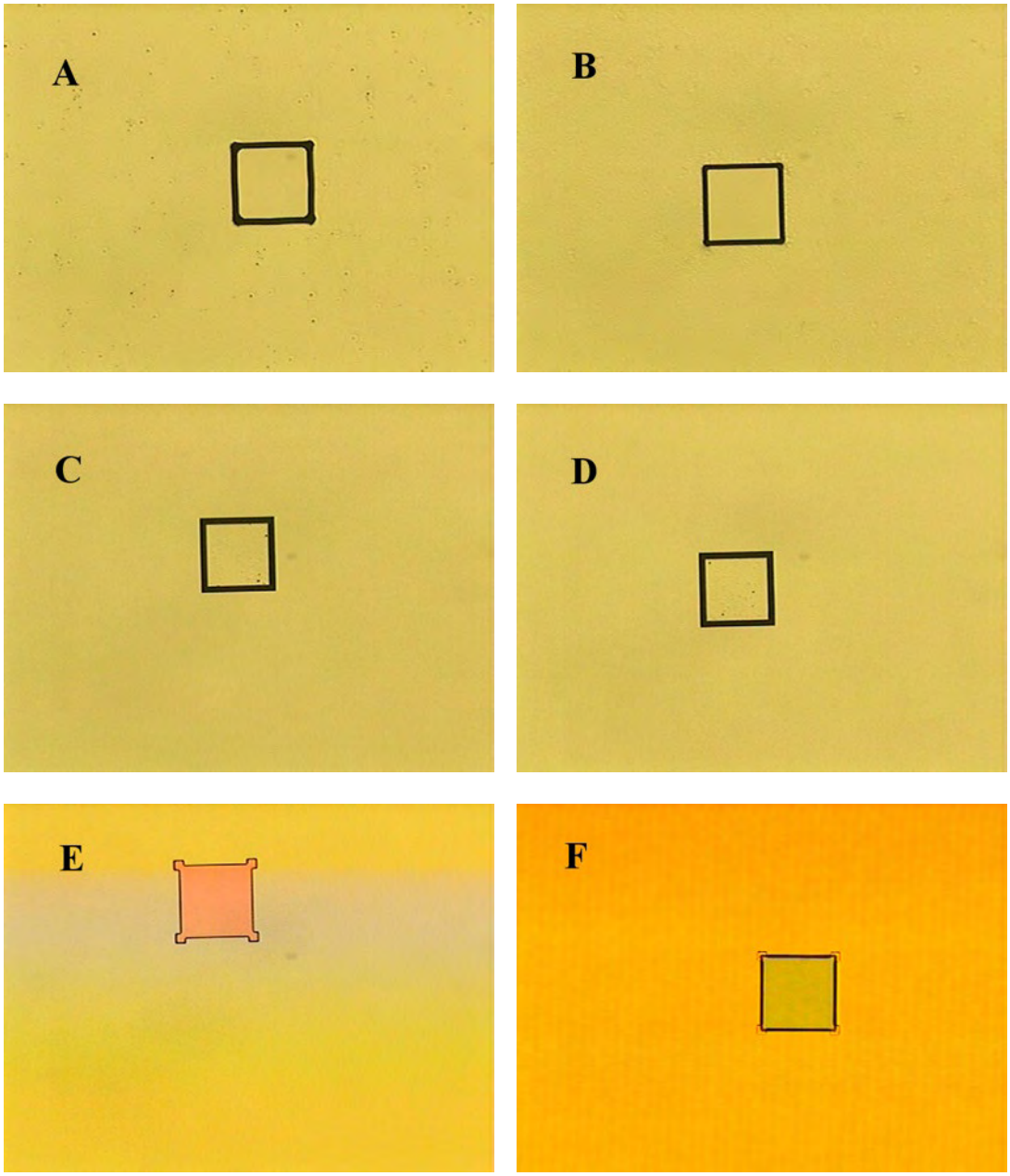

Figure 3-12: Optical images of structures etched with 25%wt TMAH+10%IPA solution at 90 °C to realize structures of depth of about 15 μm of mesa pyramids (A-B) and inverted pyramids (C-D). Pyramid dimensions are 50um x 50 um. In picture A, remnants of the corner compensation square structure are still present, indicating that the desired etch depth has not been reached yet. B. Corner compensation square structure is completely etched away, indicating that the desired etch depth has been reached. E. Corner compensation structures before the Si etching step. F. Corner compensation structures on the oxide layer are visible before the oxide layer is stripped.

3.4. 3D device Lithography:

After the pyramid structures are obtained, silicon dioxide is thermally grown at a temperature of 1100 °C for 55 minutes in order to grow ~550nm layer of oxide on each side of the RCA cleaned wafers. The oxide layer thickness is chosen to form an effective mask layer during the phosphorous thermal diffusion step.

In order to obtain 3D uniform photoresist layers, required to realize pn regions on pyramid facets as well as following metallization process, a deposition process was developed by combing spray and spin coating deposition processes.

3.4.1. Spray Coating vs Spin Coating to Achieve Uniform Layers of Photoresist

After oxide layers are thermally grown, a uniform layer of photoresist needs to be deposited in order to etch windows in the oxide layer for the selective diffusion step that follows. Spin coating and spray coating are two deposition processes attempted in order to achieve a uniform layer of photoresist, Figure 3-13.

Spin coating has been widely used as the primary method of resist deposition. Spin coating, in which resist is poured on the wafer surface and spun at high speeds, the fluid experiences a centrifugal force of rotation and a viscous shear force of the flowing annulus, causing the resist to spread across the wafer. The uniformity of the resist film and the smoothness of the surface are dependent on the viscosity of the resist solution, speed at which the resist is spun, surface topography and roughness of the wafer, and the adhesion between the wafer surface and the resist [59]–[61].

The thickness of the deposited layer can be can be calculated as follows [60]:

$$z = \frac{kP^2}{\sqrt{\omega}} \tag{3-2}$$

where z is the film thickness in µm, P is percentage of solids in the resist, ω is the angular velocity, and k is a constant in µm /sec$^{0.5}$, which is dependent on the type of photoresist used. Increasing the angular velocity at which the resist is deposited or decreasing the solids concentration in the resist solution results in thinner resist films.

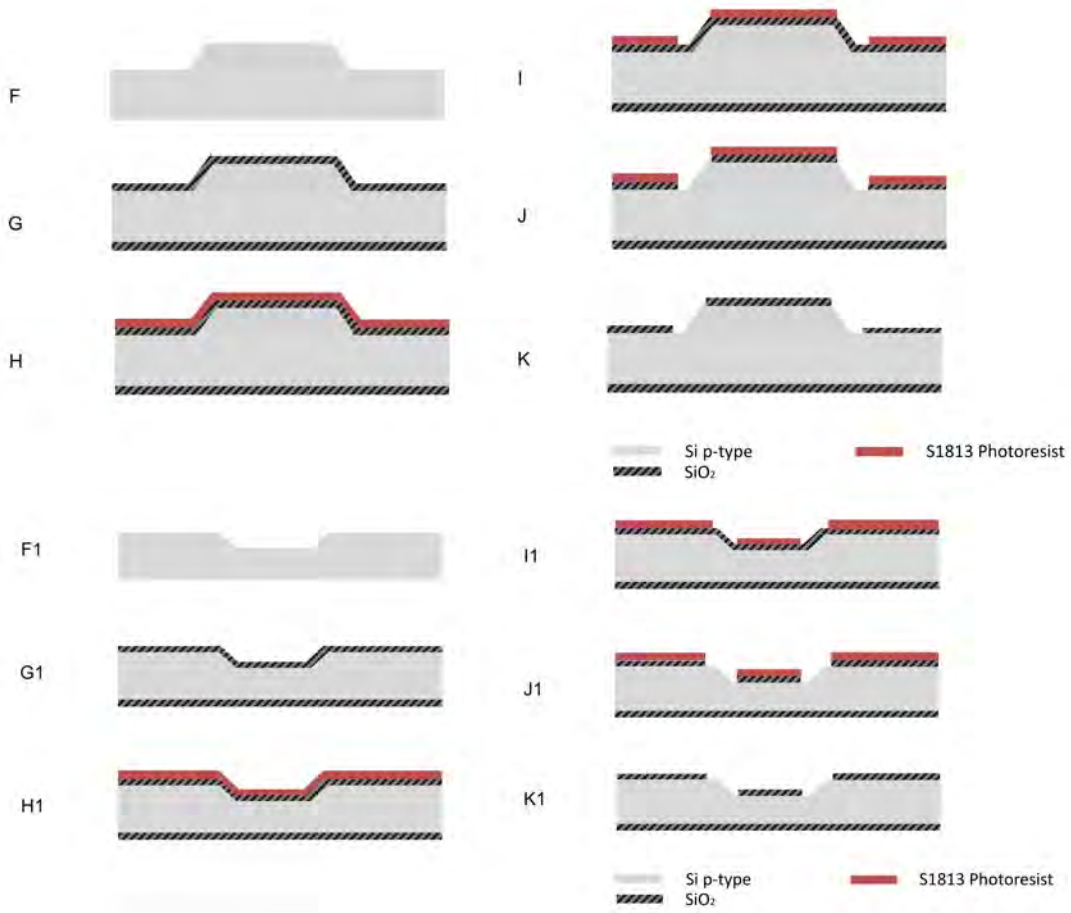

Figure 3-13: Process flow of deposition of photoresist on 3D mesa (F-K) and inverse (F1-K1) structures to create windows for the phosphorus diffusion step.

In the case of 3D structures, resist may start to slide off the edges and accumulate at the bottom of the structures. A non-uniform resist layer may cause difficulty in patterning the resist layer, thus, affecting post-patterning fabrication processes, like diffusion and metal deposition [60], [62].

Spray coating deposition is where the resist solution is stored in a reservoir and is deposited due to air pressure creating an aerosol directed towards the wafer. The spray distribution is dependent on the distance separating the nozzle from the substrate, pressure at which air inflows into the nozzle, solution viscosity, particle size, spraying velocity, and the temperature at which the deposition takes place [61]–[64], figure 3-14. It does not depend of surface roughness.

There have been several studies about achieving a uniform resist layer using both spraying and spinning coating methods [60], [62], [65]. While the spin coating method has been widely used [60], [61], [65], other methods like spray coating [62], [66], [67], electrodeposition [68], and dip coating have emerged as alternative deposition methods in order to deposit uniform resist layers on 3D structures. Spray coating may offer the most cost effective method of deposition and a wide selection of resists that are compatible with the process. Electrodeposition may offer very good step coverage and uniformity, but it requires that the resist is electrodeposited and may require the use of multiple resist baths. Spray coating offers a more controllable and reproducible method than the spin coating method, but requires the use of expensive equipment and low viscosity resist solutions [61], [65], [68]. Thus, a low viscosity solution may be unattractive for use with the mesa structures.

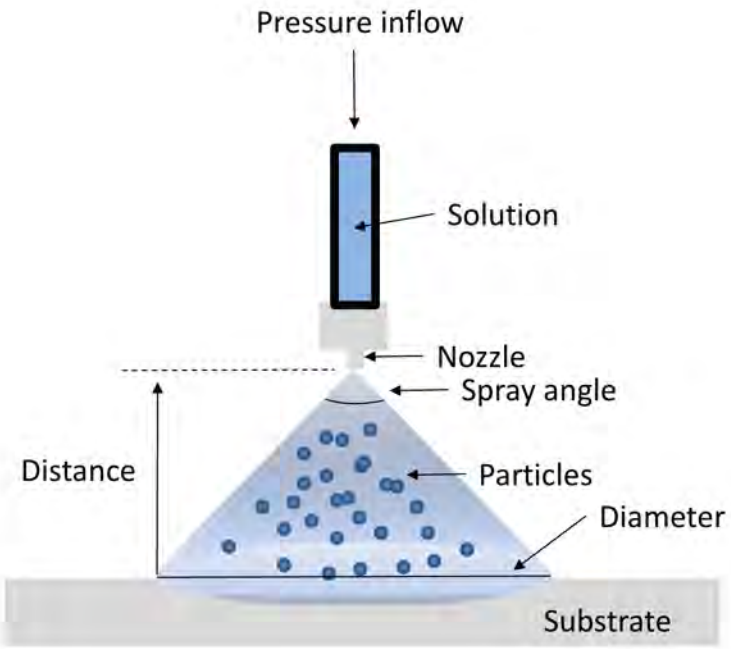

Figure 3-14: Deposition of solution onto a substrate using a spray deposition system.

Spin coating was attempted first at 4000 rpm and 2000 rpm using Shipley S1813 photoresist while using a spin coated layer of hexamethyldisilazane (HMDS), which acts as an adhesion layer, to help achieve a good adhesion between the silicon dioxide layer and the photoresist layer [69].

Since the mask design includes both inverted and mesa pyramid structures, achieving photoresist uniformity throughout is challenging. In inverted pyramids, depositing photoresist at a high spinning speed, 4000 rpm, produces a relatively thin layer of photoresist than when spinning at a lower spinning speed, 2000rpm. Spinning at 4000 rpm, the photoresist seems to accumulate in the grooves as well as spin off the top edges of the pyramids, shown in Figure 3-15. The spin off at the top of the edges is likely to be due to the centrifugal force due to spinning, noting that the pyramid is rotating around an offset axis. This causes the photoresist at the edges to spin out of the edges, for example

Fig. 3.15 A. However, spinning at 2000 rpm seemed to have a slightly better result as the resist surrounding the top edges of inverted features is relatively less sparse.

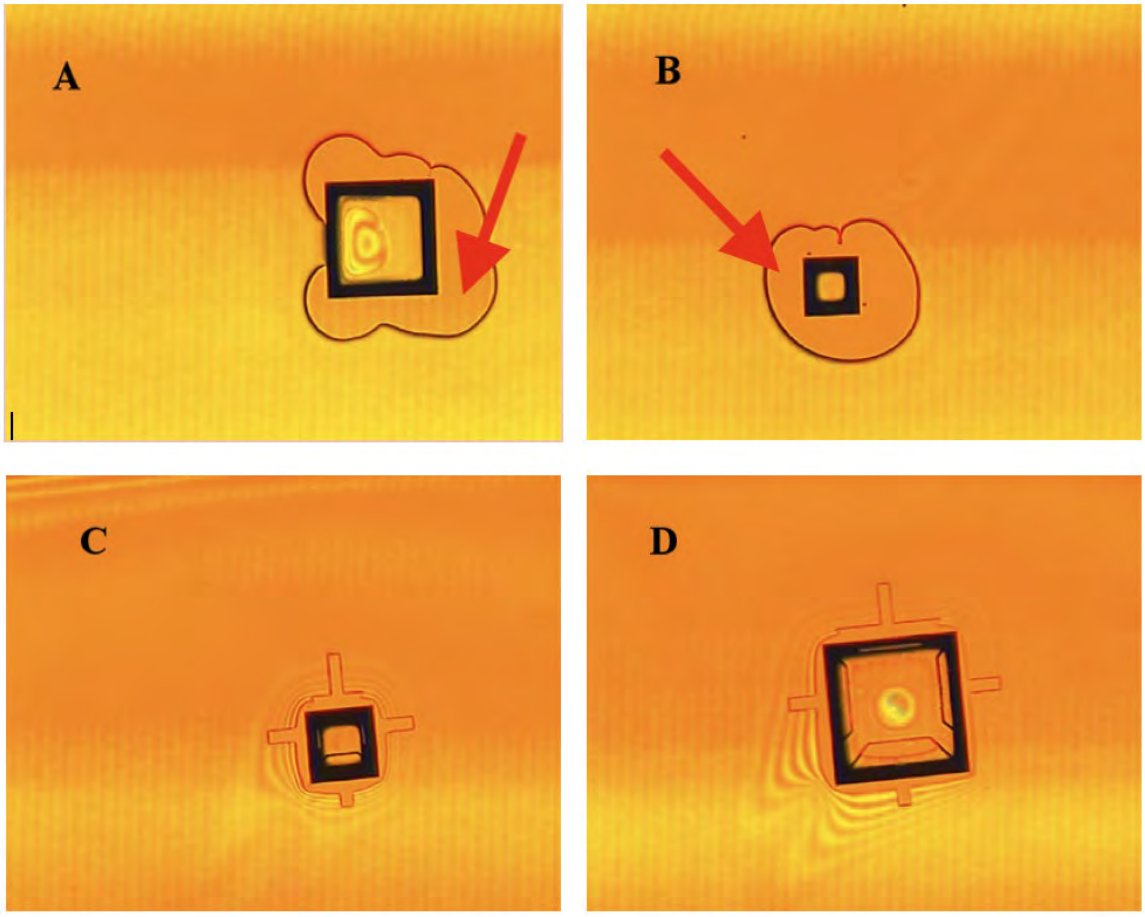

Figure 3-15: Optical images of spin coating of S1813 photoresist at 4000 rpm (A-B) and 2000 rpm (C-D) onto inverted pyramid structures of 50um x 50 um dimensions. Arrows indicate the lack of photoresist, as the photoresist seems to accumulate in the grooves as well as spin off the top edges of the pyramids.

Furthermore, in mesa pyramids, depositing photoresist at a high spinning speed, 4000 rpm resulted in photoresist accumulating non-uniformly on top of the pyramids in addition to resist sliding down the sides and accumulating at the base of the pyramids, as shown in Figure 3-16. However, spinning at 2000rpm seemed to have caused an increased accumulation of the resist at pyramid bases with resist still accumulating non uniformly at the top surface of the pyramids.

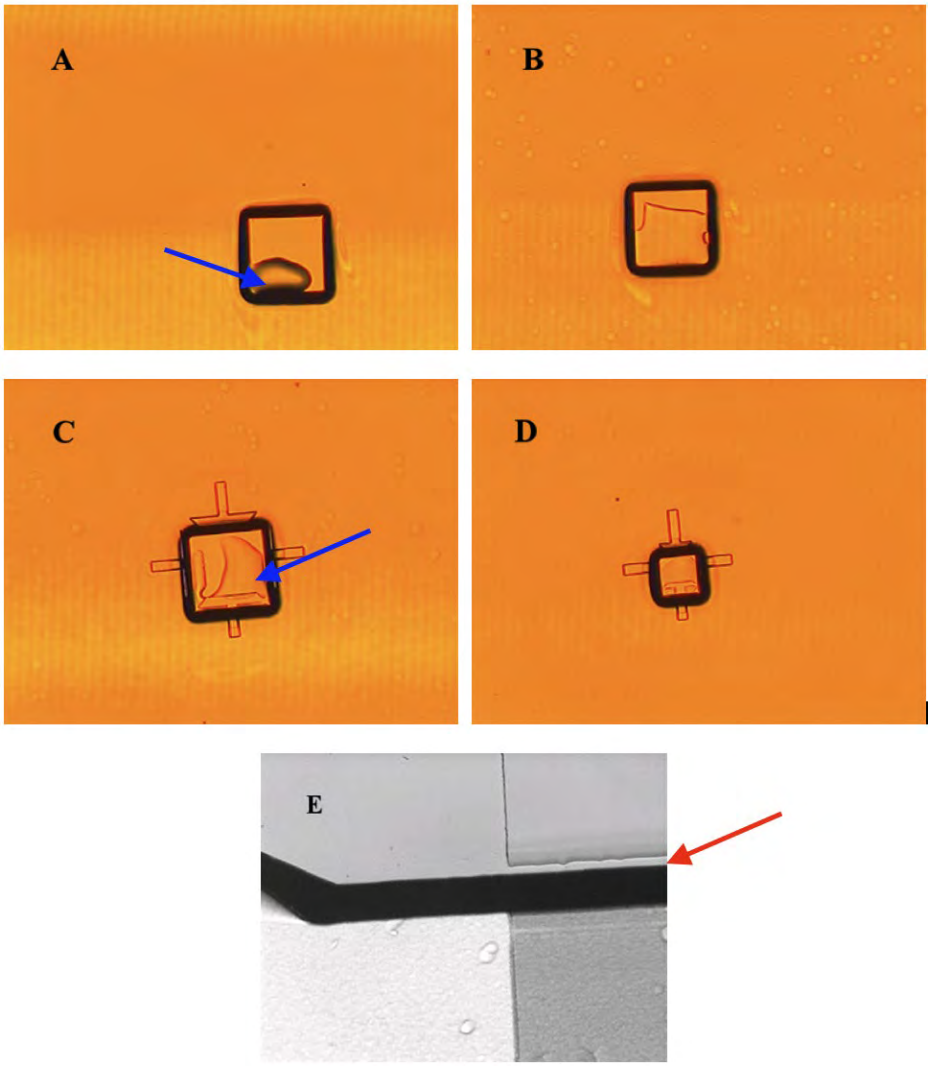

Figure 3-16: Optical images of spin coating of S1813 photoresist at 4000 rpm (A, B, E) and 2000rpm (C-D) onto mesa pyramid structures, 50um x 50um in dimension. Photoresist seems to slide and accumulate at the base of the pyramids as well accumulate non-uniformly at the top of the pyramids (blue arrows). E. Photoresist doesn't get deposited over the edge of the feature, 15um depth (red arrow).

The non-uniformity in photoresist thickness across the wafer becomes more of an issue during the exposure and development processes. Figure 3-17 shows SEM images of photoresist spin coated at 4000 rpm, where photoresist is selectively exposed and developed. Depending on the spacing between features, photoresist accumulate differently at pyramid bases. Thus, upon exposure and development, some base areas

would still have unexposed photoresist when other areas are fully exposed and developed. Even though several exposure times were tried to optimize a process that would work on all mesa and inverted features, the variation in thicknesses across the wafer as well as non-uniform distribution of resist around inverted features and atop mesa features proved to be problematic in having reproducible results. In an attempt to have a more uniform distribution of photoresist and cover more areas on the wafer, increasing the thickness of the photoresist layer by spin coating Shipley S1827 instead of S1813 was attempted, as S1827 produces a thicker layer of photoresist when spun at the same speed as S1813 [70], [71]. Spin coating S1827 caused more accumulation of resist at pyramid bases, and the non-uniform distribution atop the mesa pyramids was still present, Figure 3-17.

Spray coating was then attempted, first using a portable manually controlled spray. MicroSpray™ is a positive-acting aerosol resist, which is contained as an aerosol spray can [72]. While the method of using a portable system is convenient to deposit layers of photoresist from several angles and distances, the deposited resist layer is very thick compared to S1813, as shown in Figure 3-18. thicker lawyer poses additional challenges during exposure and development stages. The variable uniformity distribution across the wafer posed issues with a reproducible exposure and development processes is shown in Figure 3-19.

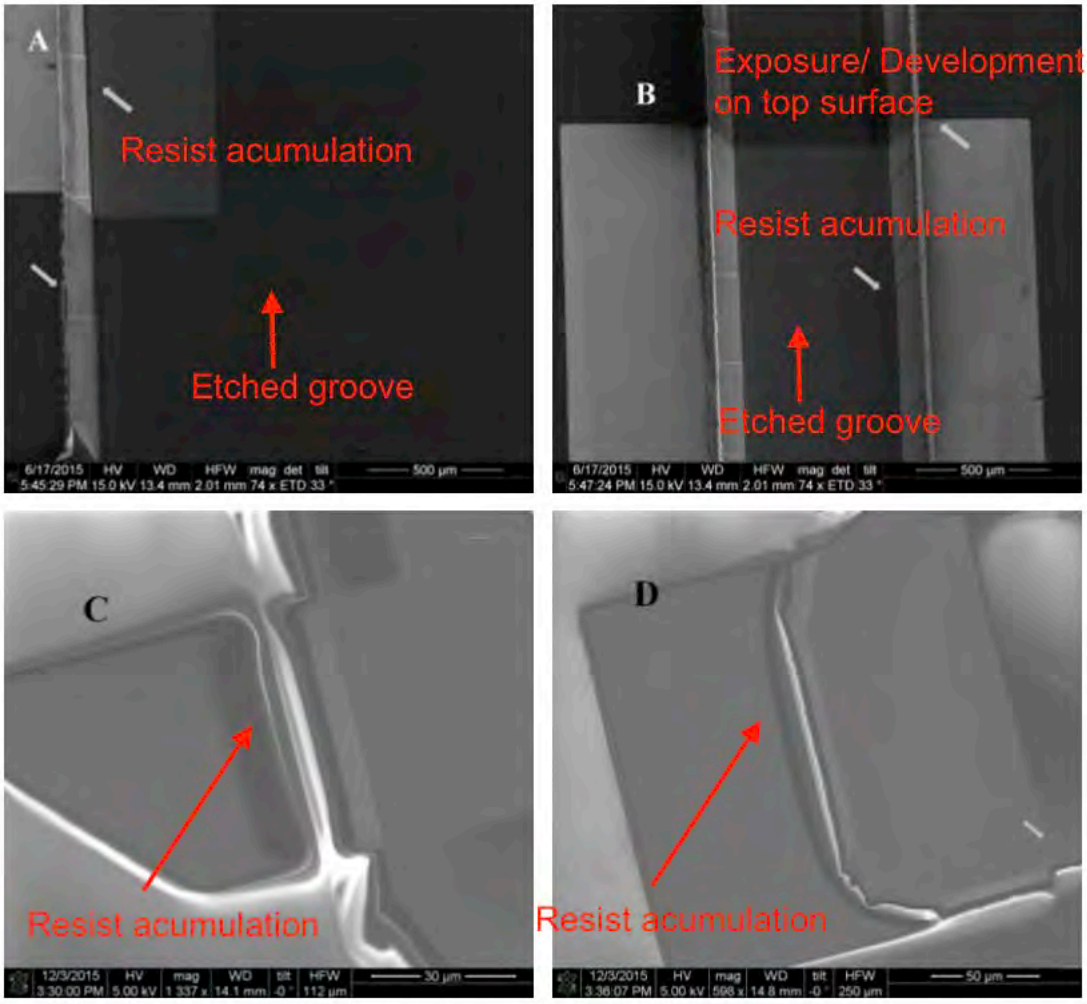

Figure 3-17: SEM images of spin coating of S1813 photoresist at 4000 rpm onto mesa pyramid structures (A, B), and images of spin coating of S1827 photoresist at 4000 rpm onto mesa pyramid structures (C, D). Accumulations of resist at pyramid bases causes variations in exposure and development times of resist across the substrate. Increasing the thickness of the resist causes more accumulations at the bases, as indicated by the arrow in C. In D, thinner resist causes less accumulations at the base of the pyramid.

Following the manual spray attempt, the SonoTek ExactaCoat Spray Coater automated spray coating system is used to deposit S1813 photoresist onto substrates. S1813 was used as the resist solution's viscosity was low enough to be deposited using the system without the need to add thinning solutions to further lower the solution's viscosity.

As the first user to use the spray system for photoresist deposition, the author conducted a study to try and optimize the SonoTek spray deposition process by varying

some of the system's features, such as flow rate, path speed, nozzle height, and nozzle power.

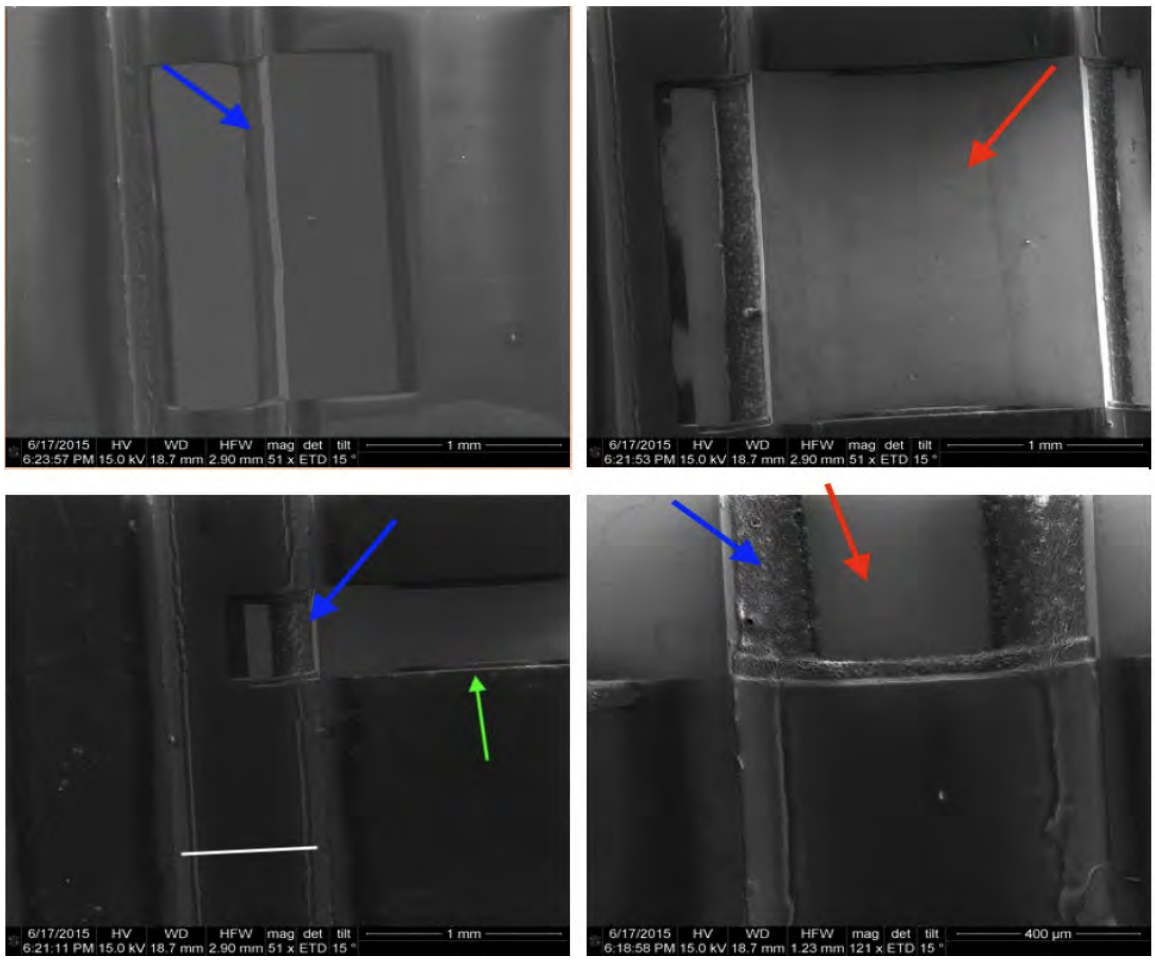

Figure 3-18: SEM images of spray coating using MicroSpray™ when the spray is held at an angle of 45°. Photoresist accumulations are present at the features bases (blue arrows). Exposure and development of resist have varying effects across the substrate. Red arrows indicate regions within pyramid tops where exposure and development were successful.

Photoresist is spray deposited using the pattern in Figure 3-20. Vertical paths (green arrow in Figure 3-20) are separated in such a way that the horizontal spacing (white line in Figure 3-20) is short enough that depositions along the vertical paths overlap. Several trials were conducted in order to determine the ideal parameters to reduce island formation in the deposited photoresist, as shown in Figure 3-13. The path speed was adjusted in order to prevent unwanted broken and segregated deposition of

resist. The nozzle height determines the diameter of deposited material as mentioned earlier.

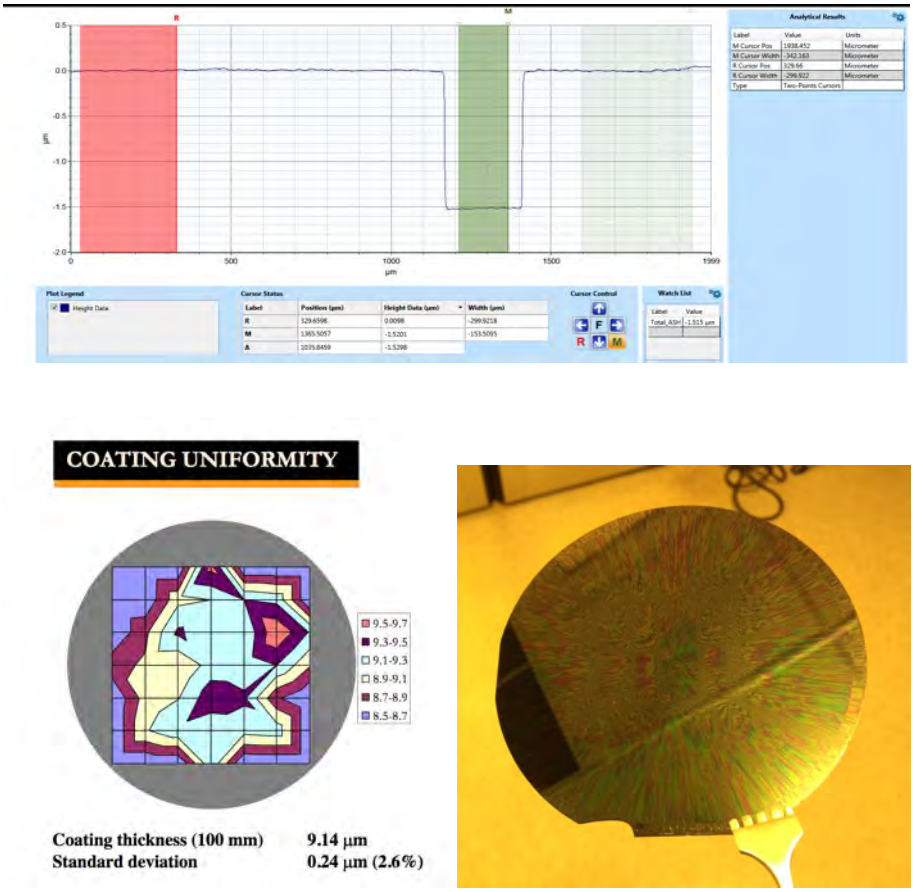

Figure 3-19: Coating uniformity of the MicroSpray™ with and average thickness of 9.14 µm a varying uniformity distribution (bottom left image) [72]. Bottom Right, non uniformity distribution in the deposited photoresist layer is visible. The difference in distribution is represented by the difference in colors of the resist layer (4 in wafer).

The deposited profile follows a distribution at which the highest percentage of material is deposited at the center of the diameter, as well as an increasing chance of island formation at the edges of the diameter where the percentage of deposited material is decreased. Thus, the nozzle height was coordinated with horizontal spacing so that the height was adjusted to have an overlapping diameter of deposition [66]. In addition, spray deposition

attempts at an idle nozzle power less than 1.5W yielded in photoresist leaking from the nozzle when the system is in idle mode. Decreasing the idle power to 1.25W decreased the leakage at idle nozzle significantly. On the other hand, running nozzle power was attempted at powers 3.5W and 5W. Profilometery analysis suggests that increasing the power to 5W had minimal effects on the uniformity of the deposition or thickness of the photoresist layer.

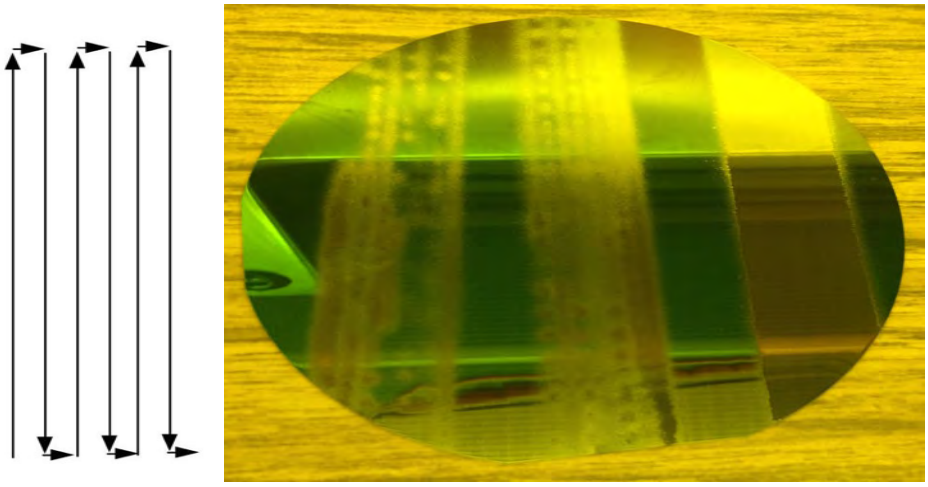

Figure 3-20: Photoresist spray pattern (Left). Photoresist pattern sprayed at a flat (4 in) wafer at pump flows 0.1, 0.3, and 0.5 mL/min at idle nozzle power of 1.25 Watts and run power of 3.5 Watts (left to right respectively).

Then, deposition while varying the pump flow rate was attempted while keeping the Idle power at 1.25 Watts and Run power at 3.5 Watts. Deposition at 0.1mL/min and 0.3mL/mins resulted in island formation, with decreased island number as the pump flow rate increased, Figure 3-21. Profilemtery results show that resist deposition at 0.1mL/min results in a photoresist thickness ranging between 2.1µm and 3.0µm. The deposition is an increase from the 1.5µm thickness using spin coating method discussed earlier. On the other hand, 0.3mL/min results in a photoresist thickness of around 5.8µm (a significant increase from 0.1mL/min pump flow rate) with a lot of non- uniformity in the deposition still

present. Resist deposition at 0.5mL/min results in a photoresist thickness of around 5.9µm, not a significant increase from 0.3mL/min pump flow rate, with a relative enhancement in the uniformity distribution.

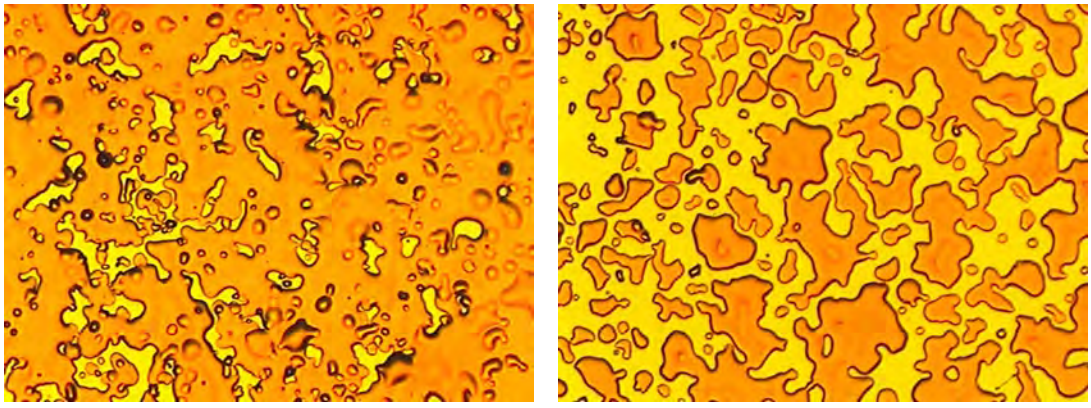

Figure 3-21: Microscope image of the photoresist showing island formation of the deposited resist. The island frequency and size increased significantly with decreasing the pump flow rate from 0.3mL/min (left) to 0.1mL/min (right).

The 0.5mL/min at idle power of 1.25 Watts and run power of 3.5 Watts were then used for photolithography steps where 3D features are present on the wafer. The spray deposition process using these parameters proved to be very efficient compared to the spinning process, as well as significantly more cost effective. The amount of resist used to deposit a thin layer of resist using spinning deposition can be used to precisely spray deposit resist onto 4 wafers. Figure 3-21 shows the optical images. The profilometery results of photoresist formation at 0.1mL/min and 0.3mL/min are shown in Figure 3-22.

Following photoresist deposition, the wafers are placed on a flat surface for a few minutes to allow the resist to settle. The wafers are then soft baked on a hotplate at 100ºC for 1 minute. The exposure step was about nine times longer at 76s compared to when the wafers are exposed at 8.5s for the spinning process, as the resist layer is significantly thicker using the spray deposition process. The combination of exposure and development

time of around 1 minute results in feature resolution of around 2μm, which is slightly worse than the resolution obtained by the spinning process on wafers with flat (2D) features, as shown in Figure 3-23.

Figure 3-22: Profilemtery results show that resist deposition at 0.3mL/min (top) results in a photoresist thickness of around 5.8μm (not a significant decrease from 0.5mL/min pump flow rate) with a lot of non-uniformity in the deposition. Resist deposition at 0.1mL/min (bottom) results in a photoresist thickness of around 2.1μm (a significant decrease from 0.3mL/min pump flow rate) with a lot of non-uniformity in the deposition with regions of an average thickness of around 3.0μm.

Following a hard bake process of the wafer using a hotplate at 115 ºC for 2minutes, BOE is then used to etch away the oxide layer at the non-photoresist protected regions on the wafer to create windows through the oxide layer in preparation for the selective thermal diffusion process. Following the oxide etch step, the photoresist

layer is stripped in acetone. This is followed by an IPA and DI water rinse.

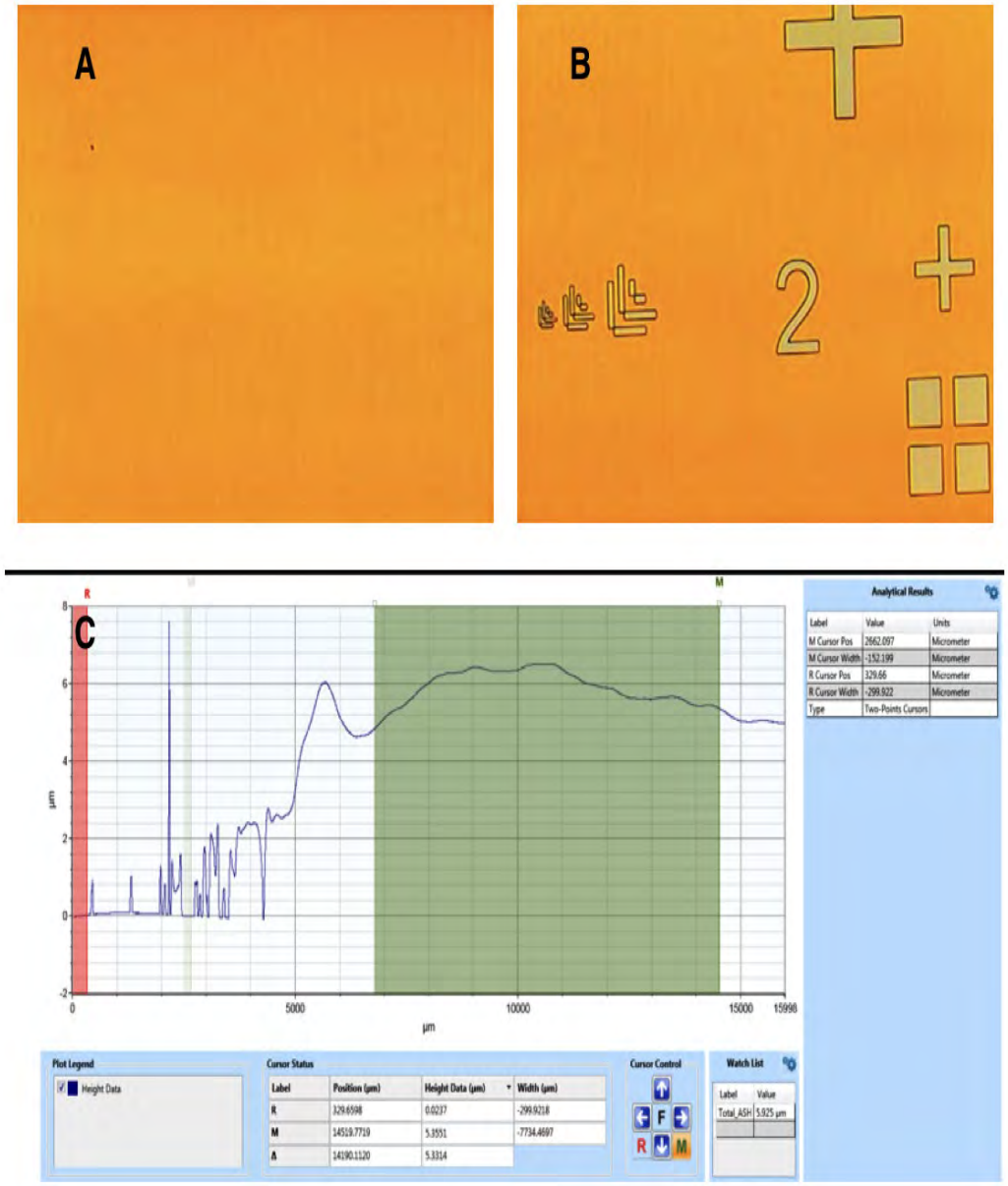

Figure 3-23: Microscope image of the photoresist showing uniform deposition and lithography at flow rate deposition of 0.5mL/min. Profilemtery results show that resist deposition is relatively uniform with thickness of around 5.9µm. L-shape alignment features in B are 1um, 2um, and 5um feature lengths.

3.5. Forming the p-n junction photodiodes

3.5.1. Diffusion of Phosphorus

In order to create n-type regions in the p-type substrate, the substrate needs to be doped with n-type dopants such as Arsenic or Phosphorus. Such impurities are introduced into the substrate, at low concentrations, to selectively modulate some of its electrical and optical properties. Impurities are mainly introduced through ion implanters or diffusion. Ion implantation takes place by directionally accelerating individual ionised dopant atoms (ions) at high voltage/high current, leading to the precise control of doping position and depth levels as well as less radial spread of dopants, laterally and into the substrate, making the process suitable for small structure (< 2μm) devices. However, accelerating dopants into individually-processed substrates may lead to lattice damage in Si. In addition, activating the dopants at high temperatures leads to the diffusion of dopants further into the substrate, thus, altering dopant positions and creating larger diffusion regions than desired. On the other hand, the thermal diffusion of dopants instead of implantation is typically easier to integrate with complex processes. In diffusion, where multiple wafers can be placed in close proximity to the doping source in a high temperature chamber, dopants naturally gradient flow from the source, a higher dopant concentration to a lower dopant concentration, without relying on further activation or thermal processes [73]–[77]. Thus, thermal diffusion is used for the initial proof of device concept. Upon further investigations and device optimization, ion implantation was to replace the diffusion process for more controlled, accurate doping profiles. However, the ion implantation

machine was not accessible during the fabrication process, and diffusion was sufficient for device fabrication and performance testing.

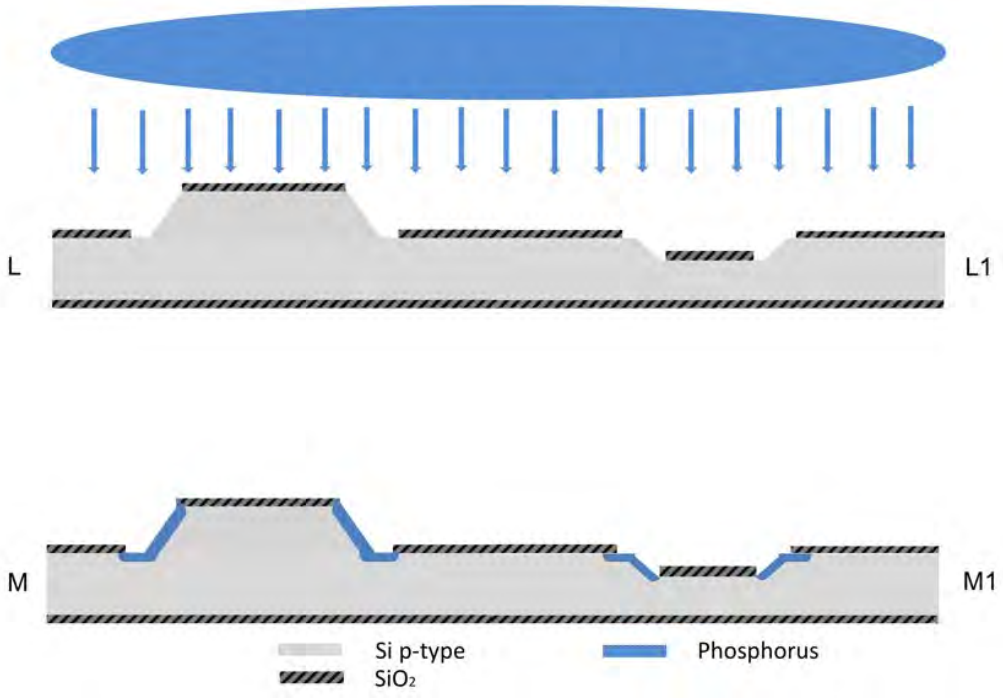

Figure 3-24: Process flow and schematic of the phosphorus diffusion step in order to create p-n junctions mesa (L-M) and inverse (L1-M1) structures.

Thermal diffusion of phosphorus is carried out in a furnace at 975 °C for 25 minutes. The oxide layer serves as masking layer against unwanted diffusion of phosphorus. Thus, openings in the oxide layer are used to create a selective diffusion process in which p-n junctions are created on the slanted sides of pyramids. The openings are designed in such a way to account for the dopants that are expected to diffuse laterally as well, thus, they are separated enough to avoid any type of overlapping among diffused regions, in Figure 3-24.

Solid PH-1000N phosphorous sources, from PDS® Products, are used as a constant diffusion source, in which a constant level of surface concentration of phosphorus

in maintained. The wafers are placed with features facing the white phosphorus sources discs.

The diffusion coefficient, D, of phosphorus can be calculated using [74], [78], [79]

$$D = D_0 \, exp(-\frac{E_A}{k_B T}) \tag{3-3}$$

where E_A is the activation energy of phosphorus, k_B is the Boltzmann' s constant, T is the temperature, and D_0 is the pre-exponential diffusion coefficient of phosphorus. However, during ramp up and ramp down, the temperature is changing at a constant rate of 10 ºC per minute. Thus, the temperature change, from the initial temperature of 800 ºC, can be represented by the function

$$T(t) = 800 + 10t \tag{3-4}$$

The solid solubility limit at the temperature change from 800 ºC to 975 ºC is not significant enough to affect the junction depth estimations [80], [81]. The changing diffusivity during ramp up can be calculated using:

$$D = \int_0^{17.5} (D_0 \, exp\left(-\frac{E_A}{k_B T(t)}\right) \tag{3-5}$$

where the initial and final times are based on the constant ramp up rate of the furnace. Similarly, expressions for temperature change and diffusivity change due to temperature change are used for the ramp down at the rate of 10 ºC per minute.

The total diffusivity is the summation of the diffusivities during ramp, ramp down, and the diffusion at 975 ºC, can be calculated, [74], [79]

$$(Dt)_{total} = \sum_i (D_i t_i) \tag{3-6}$$

Using the surface concentration equation of phosphorus where the diffusion depth, x, is at the junction depth [74], [79],

$$\mathrm{N_S\,(x,t) = N_B\ erfc}\left(\frac{\mathrm{x_j}}{2\sqrt{\mathrm{Dt}}}\right) \tag{3-7}$$

where N_B is the background doping concentration of the substrate discussed in an earlier section.

Thus, the junction depth can be estimated, using a complementary error function equivalence table, as summarized in Table 2, [82]. The surface concentration of phosphorus is the solid-solubility limit at 975°C [80], [81].

Table 2: Simulated resonance frequencies of five different devices with different coupling ratios.

N_s [cm^{-3}]	N_B [cm^{-3}]	D_0 [cm^2/s]	E_A [eV]	k_B [eV/K]	Junction depth [µm]
≈$8.5x10^{20}$	$1x10^{16}$	4.70	3.68	8.62×10^{-5}	1.34

3.6. Low Temperature Oxidation and Metallization

Following the phosphorus diffusion step, the oxide layer, previously acting as a diffusion mask, is stripped away in order to grow a new thin layer of oxide. The oxide mask layer needed to be removed, as potential trapped charges in the oxide layers would interfere with the device operations. In MOSFETs for example, trapped charge in the

dielectric oxide layer creates part of the gate threshold voltage, where the mismatch could degrade device functionality, especially in ultra-low-power systems. The type of charge is dependent on the process parameters, where fixed oxide and interface charge, at Si-SiO2 interface, are caused by structural Si defects from oxidation or bond breaking at interfaces and temperature and cooling rates, respectively. Other charges include charges due to highly mobile ions of impurities or due to static charges. Stripping the oxide layer avoids dealing with trapped charges, and a new thin layer of oxide is grown to ensure the device electrical insulation [74], [76]. This is followed by lithography steps to create metallization contacts through the LTO layer and metallization are similar to the previous steps, where a uniform thin layer of resist was deposited throughout the wafer.

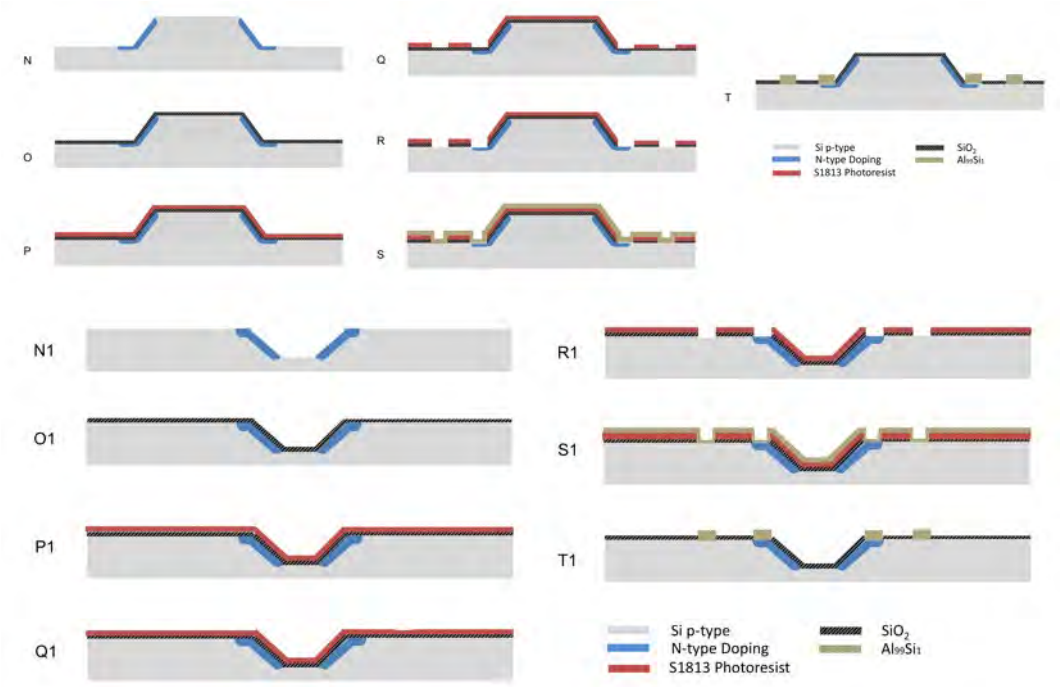

Figure 3-25: Process flow and schematic of the LTO and metal lift off steps in order to create metal connections to p- and n- regions in mesa (N-T) and inverse (N1-T1) structures.

The thin layer of silicon dioxide is thermally grown using wet oxidation at a relatively low temperature, 800 °C for 3 hours to obtain an 80 nm – 100 nm thin layer of oxide.

Relatively low temperatures are used to grow the layer since higher temperatures cause the drive-in of phosphorus into the substrate. The thin oxide layer acts as an electrical insulating layer. Contact windows are etched through the oxide layer, as the contacts can then be made with the metallization step later on. Spray coating with the parameters discussed in a previous section is used to deposit a uniform layer of photoresist, as the oxide layer is etched as before. Then the photoresist layer is stripped in an acetone bath followed by IPA and DI water washes, as shown in Figure 3-25.

Following RCA cleaning of the wafers, a lift-off process then follows. A layer of resist is deposited on the wafers using spray coating (similar parameters as earlier steps), the resist is patterned, Figure 3-27, and a layer of silicon doped aluminum is deposited onto the wafers. The metal on non-patterned regions is then removed as the resist is stripped. The ~340nm metal layer is %1 Si doped aluminum alloy ($Al_{99}Si_1$) which is deposited using DC sputter deposition in order to create a low resistance interconnection and provide bonding pads. While thermal evaporation offers poor step coverage. This makes it better for a lift-off process, obtaining consistent metal deposition results was not attainable. The Si-doped Aluminum is used to ensure that Al does not diffuse into the substrate, as Al can also act as an impurity, rather than creating a low resistance contact metal layer [74], [76].

Finally, wafers are annealed at a temperature of 450 °C for 25 minutes in order improve the metal to silicon contact. The quality of the contact was significantly enhanced post annealing, Figure 3-26. I-V characteristics of a diode were measured using Tekronix Curve Tracer Type-576, as shown in Figure 3-26. Figure 3-27 shows the optical images of spray deposited photoresist that is patterned before the metal deposition and lift off steps for the inverse and mesa pyramids. Figure 3-28 shows SEM images of the

microfabricated mesa and inverse pixel designs. Figure 3-29 shows an optical image of the microfabricated mesa pixel design.

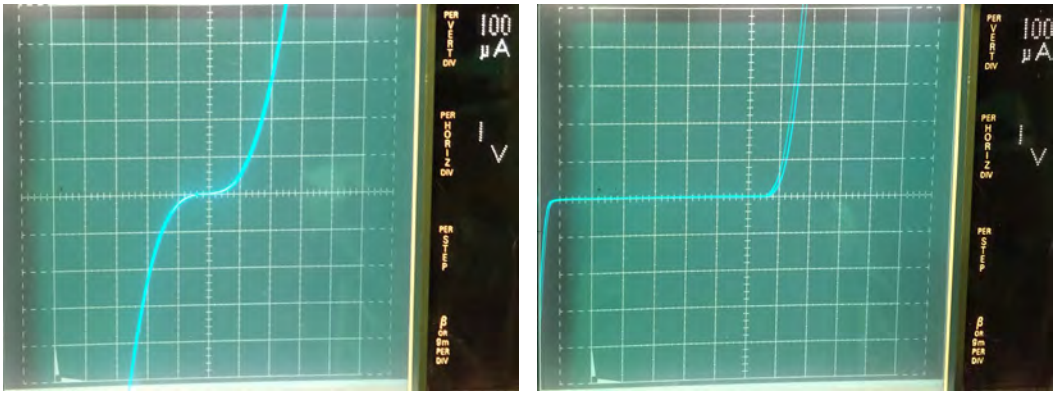

Figure 3-26: I-V characteristics of the microfabricate photodiode measured using Tekronix Curve Tracer Type-576. Left, image shows an I-V curve of a diode with a non-ohmic contact. Right, image shows an I-V curve of a diode with post annealing.

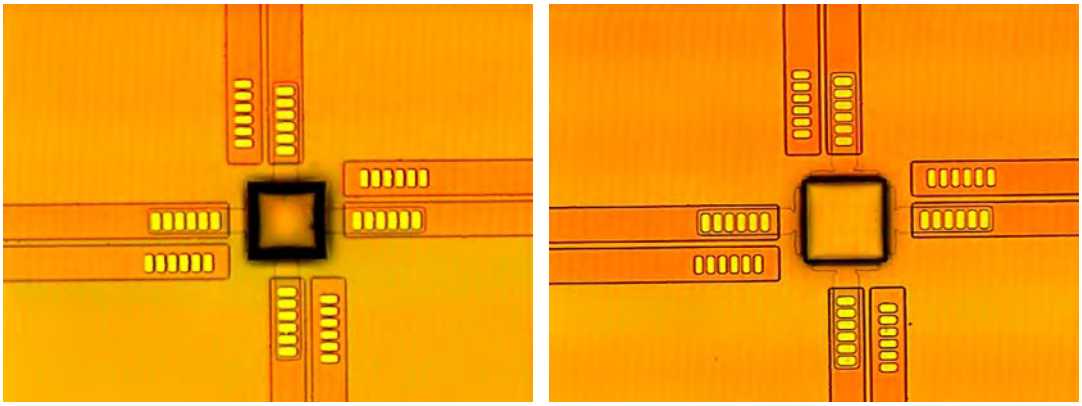

Figure 3-27: Optical images showing spray deposited photoresist which is patterned (windows) before the metal deposition and lift off steps, (Left) inverse pyramid, (Right) mesa pyramid. Metal windows are 15 um wide.

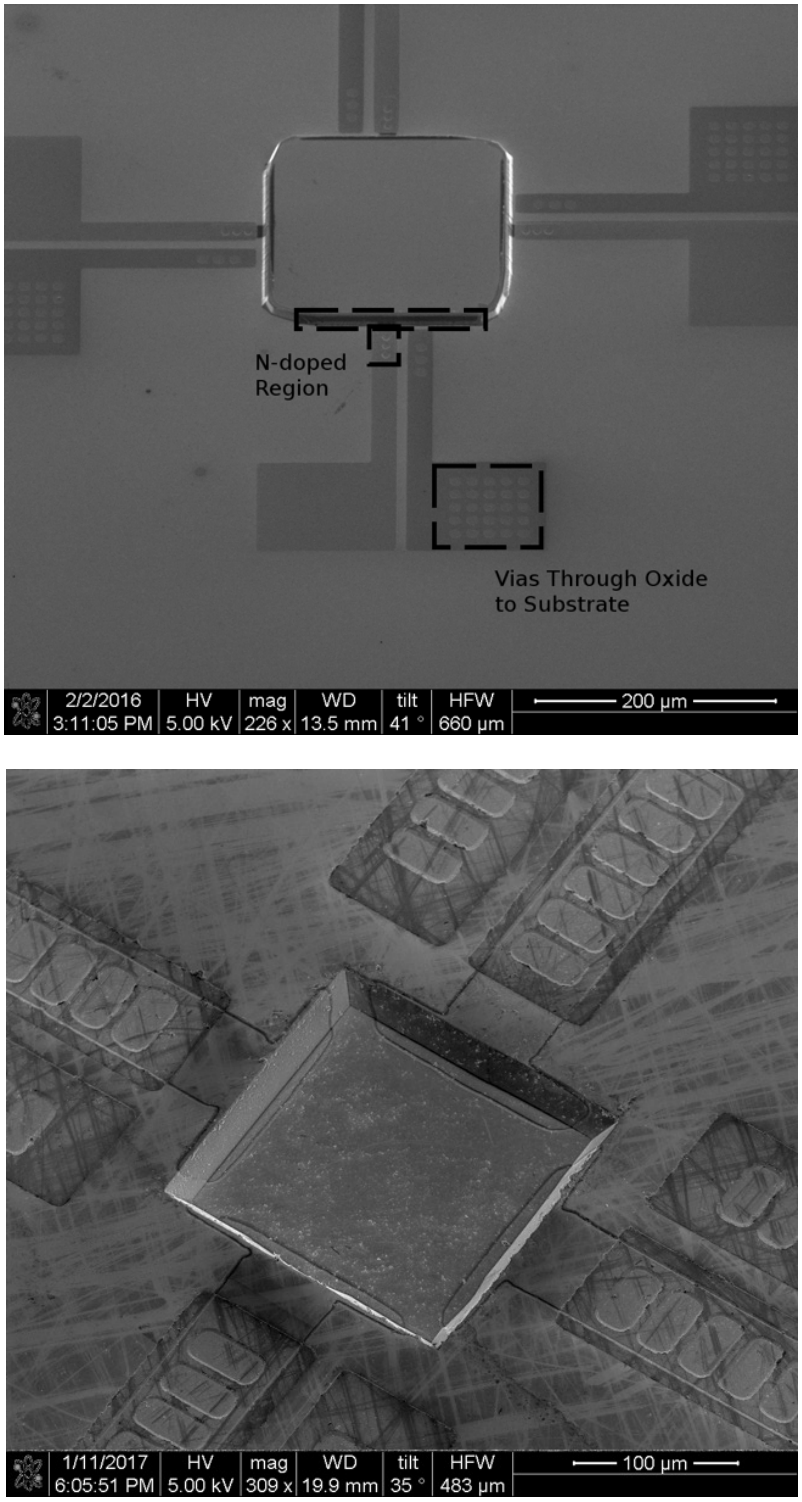

Figure 3-28: SEM images of the microfabricated mesa pixel design (Top) and the inverse pixel design (Bottom). Pyramids showing N-doped regions, while p-regions on the substrate are connected through the metalized vias. [37] ©2017 IEEE.

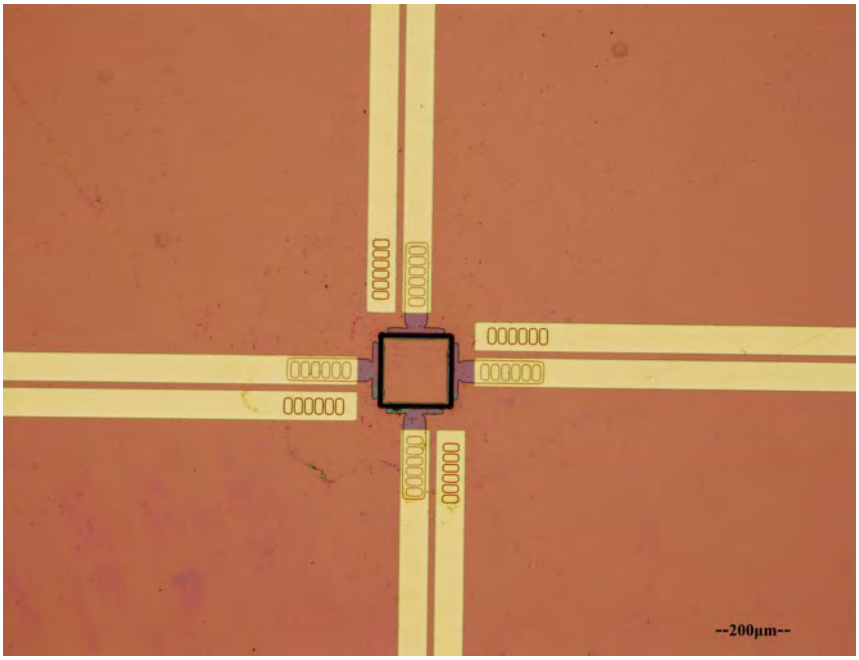

Figure 3-29: Optical image of the microfabricated mesa pixel design. Contact pads connect the doped N-regions on the pyramid with the substrate (p-region) through vias. Contact pads are designed to be far away from the pyramids to prevent light interference or reflections.

3.7. Packaging for tests

There were two sets of fabricated designs in total. In the first design, the metal pads were close to the pyramid, which would be problematic if loops of bonded wires during wire bonding and packaging step were large enough to cause reflections from light sources, potentially affecting generated photocurrent readings. An SEM image of the first design of the microfabricated device is shown in Figure 3-28 (Top). The second design included a potential solution by moving the contact pads much further away from the pyramid in order to minimize reflections from wires. An optical image of the second design of the microfabricated device is shown in Figure 3-29. The difference in size of the two designs is more visible in Figure 3-30, as the package cavity size for design one has

dimensions of 0.9mm x 0.4mm with samples dimension of 0.25mm x 0.25mm while the package cavity size for design two has the dimensions of 0.8mm x 0.8mm with sample dimension of 0.75 mm x 0.75mm. Samples are mounted inside a Dual-In-Line (DIP) ceramic package and attached with a conductive tape.

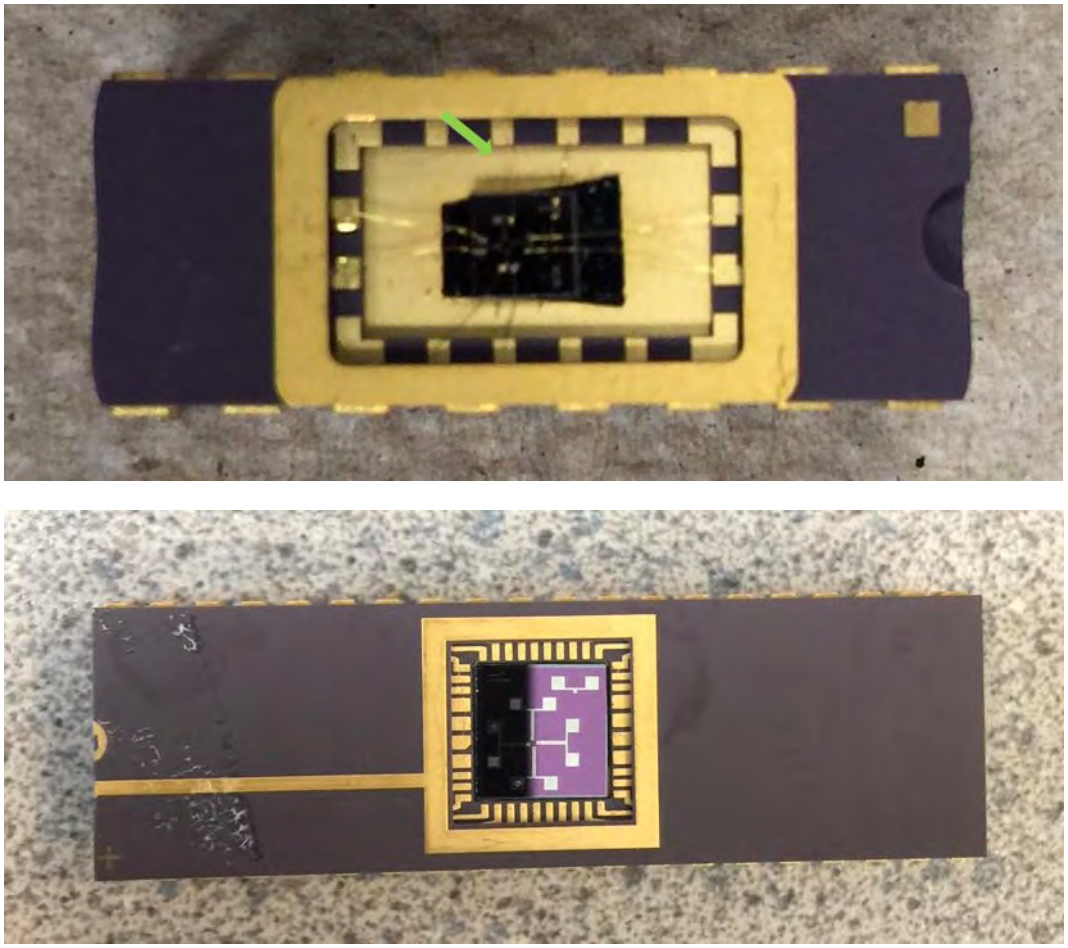

Figure 3-30: Images of the two sets of fabricated designs, (Top) first design, (Bottom) second design mounted on DIP ceramic packages of different sizes. The green arrow in the top image points at a wire connecting the fabricated device with the package. Wires connect the sensors to the pads on the package, allowing the sensors to be connected to bread boards for easier testing in circuits.

4. Results for the Microfabricated Vector Optical Sensor

In this chapter, characterization of the microfabricated mesa vector optical sensor design is presented and discussed. The validation of performance of the device uses the experimental testing setup discussed previously for the prototype is demonstrated. Parts of this chapter are adapted from [37].

Microfabricated Mesa VOS - One Pixel System is shown in Figure 4-2. Figure 4-1 shows an SEM image of the fabricated pixel in p-type Si substrate. The phosphorus diffusion regions on each side of the pyramid have an average area of 1.50×10^{-3} mm^2. The pyramid-top surface area is 200 µmx200 µm and has an average depth of 15 µm.

4.1. Test setup considerations

When using the microscope to take optical images, it was interesting to see how the pixel responds to natural light from the lab window compared to the flat design. The shining surfaces of the pyramid indicate the direction at which light is coming from, light from the nearby window in the lab area is projected from the east (with slight deviation to the north) side of the pixel. On the other hand, it is not easy to determine the direction of incident light in the flat design. Figure 4-2 shows the schematic of the circuit used. The photodiodes are connected in parallel with one another and in parallel with a power source Vee at 4V. A transimpedance amplifier is used to convert the photocurrents generated from each photodiode to measurable voltage outputs. Capacitor C1 is used to

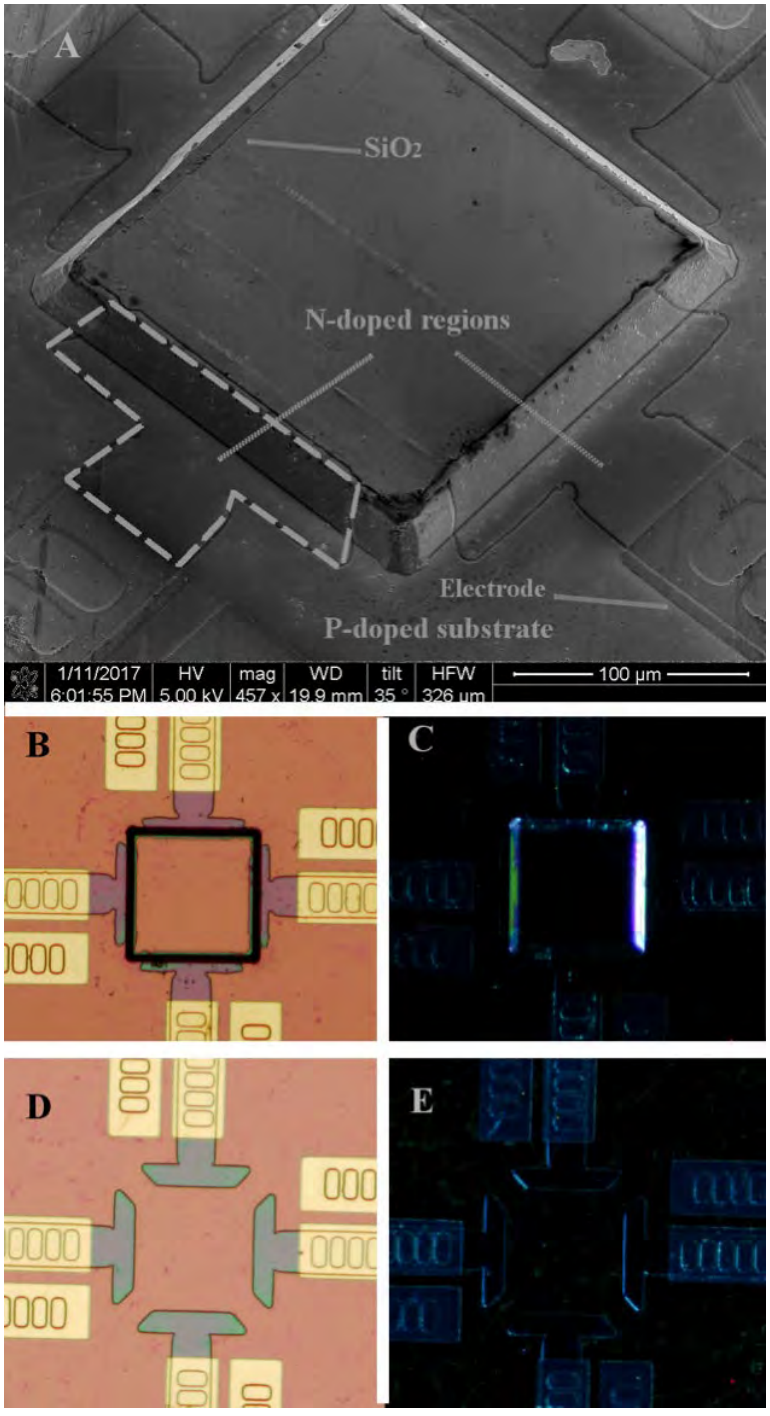

Figure 4-1: (A) SEM image of a mesa microfabricated design showing the electrodes connecting doped and substrate regions. Optical microscope image of a mesa pyramid design with microscope lights turned on (B) and off (C). (C) demonstrates light detection through directionality, as incident light from a nearby source can be seen across all pyramid facets. Optical images of the flat design with microscope lights on (D) and off (E). The direction of incident light in (E) can not be identified.

decrease the output noise, hence, facilitate the control of input current. As a control, a flat design was also fabricated at the same time and mounted in similar packaging to the mesa pyramid design. An Arduino Mega256 microcontroller is used to read the voltage outputs from the photodiodes as well as to provide a D/A input for a photodiode on a flat surface, which is used to filter out background light. MATLAB® is used to analyze the acquired data and display the outputs in real-time.

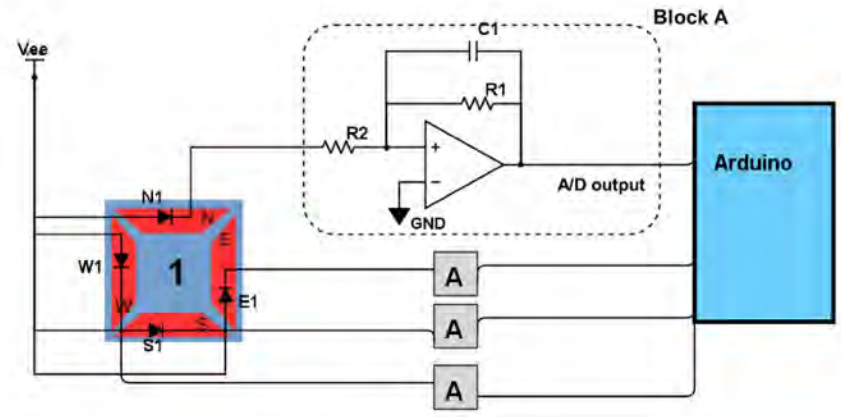

Figure 4-2: A schematic of the circuit used with a TIA circuit and an Arduino Mega256 microcontroller. Generated photocurrent from the connected and packaged photodiodes due to light detection are converted into voltage readouts on the microcontroller for further signal processing. [37] ©2017 IEEE.

An optical enclosure (Thorlabs XE25C7) was used to minimize the device exposure to unwanted background environment illumination. A microcontroller with a stepper motor module is used to position and rotate an optical source (incandescent light bulb, 1.4W) in 3D, as shown in figure 4-4.

4.2. Functional tests and diode calibration

DC current-voltage (I-V) characteristics of the diode was obtained using a National Instruments PXIe-1085 with multifunction DAQ modules system, which was used as a

power source and to acquire voltage and current readings from the photodiodes. figure 4-3 shows the measured IV characteristics of the photodiodes on one pixel in a dark state, when there is no illumination, and when illumination is introduced. The I-V characteristics follow the ideal diode model, and the photodiodes are operated in the reverse current mode at bias voltage of -5.0V [37].

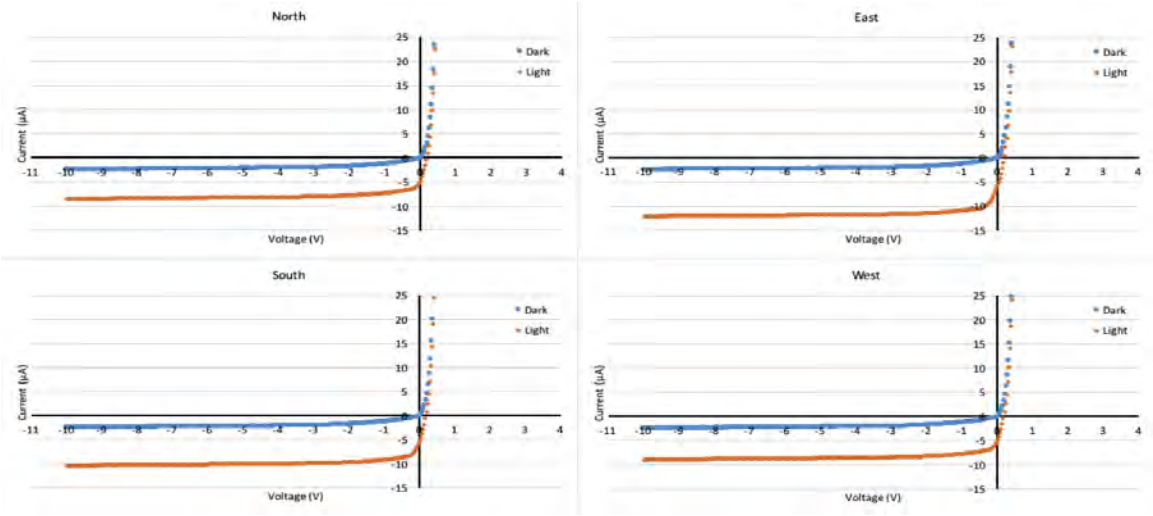

Figure 4-3: Current voltage characteristics of the four photodiodes of the pyramid pixel when the pixel is placed in a dark setting, and when the pyramid is exposed to light (optical microscope, under constant illumination conditions) directly above the sample. Photodiode characteristics are observed as expected. Generated photocurrent is detected due to light exposure. Generated photocurrent in all facets is of approximate value, which is also expected for microfabricated photodiodes in very similar settings. The slight variations in the photodiode characteristics are expected, since each photodiode on the same wafer will have similar characteristics, but not identical.

An incandescence light bulb (1.4W) is used as an optical source to expose the detector from several locations, and generated photocurrents at the facets of a single VLS pixel are measured. Since variations in the photodiodes' characteristics, raised by the fabrication process or otherwise, will affect the pixel measurements, it is important to consider the range of characteristics. These are tested for each facet by taking each facet's I_P measurement at an angle of 90°, relative to the pixel rather than the facet, by

placing the incident light source directly above the pixel at a position right on top of the center of the pyramid.

4.3. Pixel Tests

The generated IP ratio of two opposite facets of the pyramid is calculated, and the ratio is then used to find the inclination angle, as described earlier, after the facet diodes are calibrated. Thus, a photocurrent ratio equal to one indicates that the optical source is at a position equidistant from all four facets, that is, at a location above the center of the pyramid. However, conditional statements need to be included during signal processing steps, such that the pixel distinguishes relevant facets ratios for angle calculations.

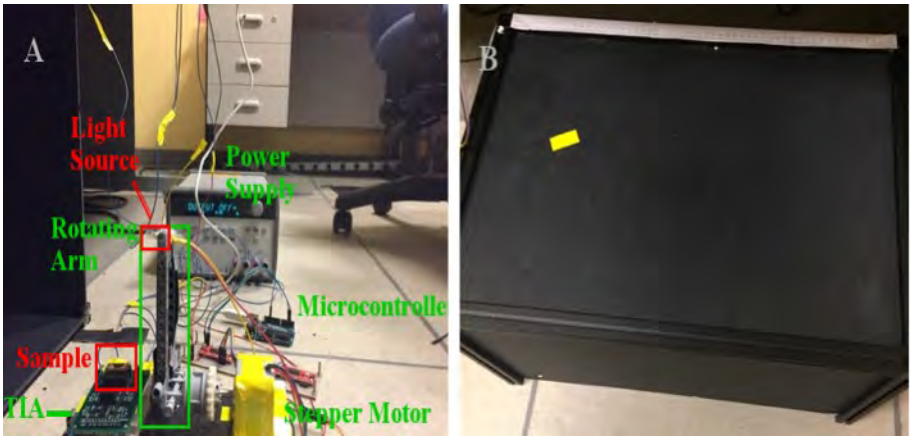

Figure 4-4: Images of the experimental setup. A. The packaged sample is connected via a TIA circuit to the microcontroller (Arduino). The stepper motor is used to rotate the arm holding the light source to several angular positions. The stepper motor is controlled by a microcontroller. B. The system is placed under a black box (Thorlabs) to reduce background lighting [37] ©2017 IEEE.

However, it may arise during inclination and rotational angle calculations, that one of the ratios is reading a value close to one while the other ratio is distinctly reading values which

are erroneous, such as a very high ratio, due to one of the facets not receiving enough illumination for example.

Furthermore, on design trade-offs, incident light projections have to be angled at an inclination angle between 54.7º, the pyramid base angle, and 125.3º, the complementary angle of the opposite facet. Projections outside this range yield an increasing error in estimation, as photocurrent readings become more unreliable as the facet opposing light projections becomes in the shadow of the pyramid. Figure 4-5 shows real and experimental values of the inclination and rotational angles, i.e. the angular resolution for the one pixel system, as the optical source position was varied.

Results indicate that the experimental values are accurate to within 2 degrees when the optical source is projected at an angle equal to α, that is when one of the facets is at planar optical projection. However, errors arise when the projection angle deviates from angle α, as projection intensity becomes proportional to the cosine of the inclination angle [83]. Errors become more significant when projections occur at an angle smaller than α from either side of the facets, since minimal light gets exposed onto the opposite facet of the pyramid, and the photocurrent response on the photodiode is close to zero, thus, obtaining an accurate response becomes more challenging.

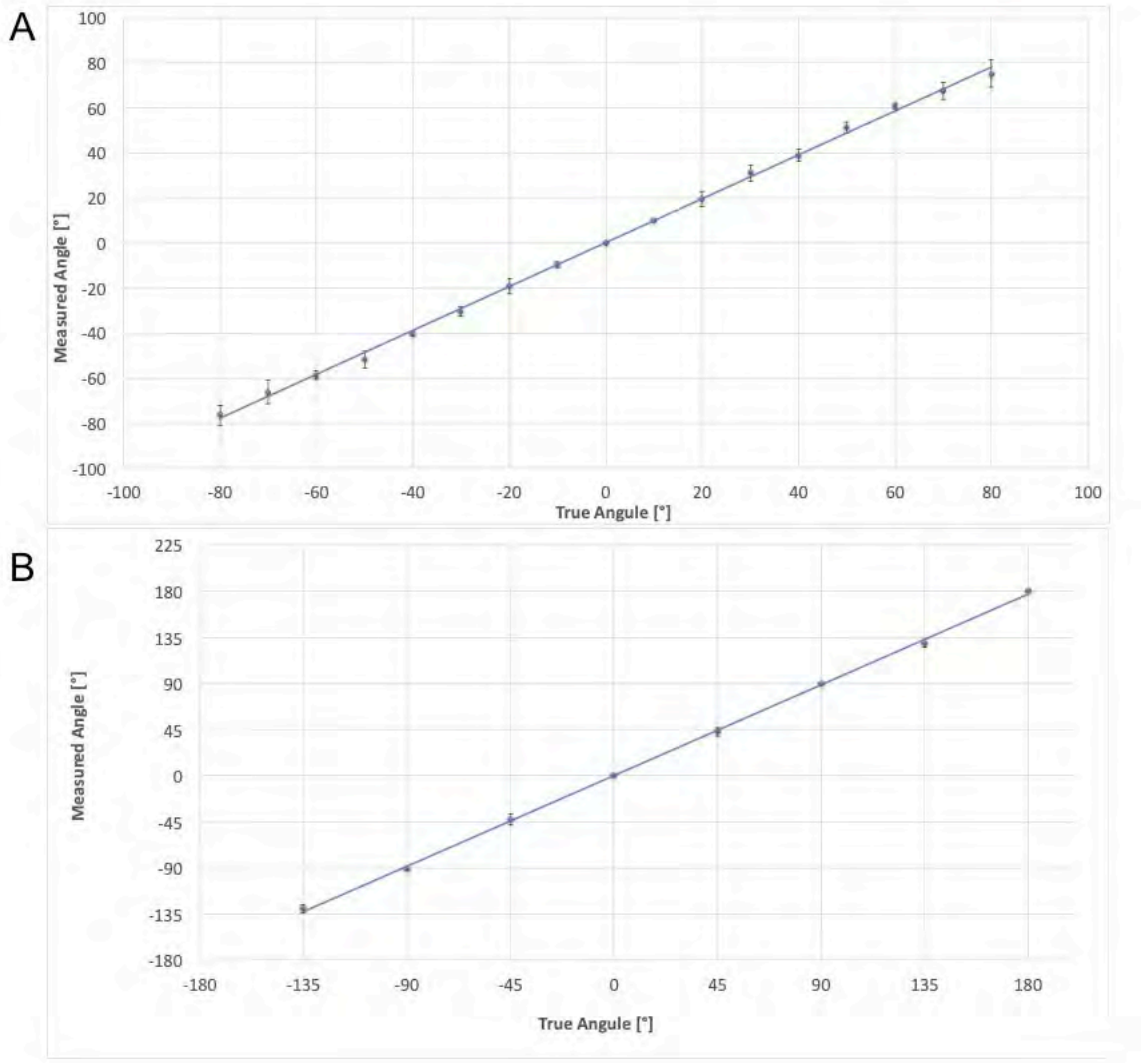

Figure 4-3: Actual and measured values of inclination and rotational angles, A and B respectively. Incident ambient light is projected and varied from between - 80° and 80° onto all the facets of the pyramids. As expected, detection at incident angles closer to 90°/-90° yield more errors and deviations from true angles, as facets opposing incident light start failing to detect the light. Measured angle and the angle of rotation in 360 ° respectively. The error bars represent the results from repeated measurements [37] ©2017 IEEE.

4.4. Photodiode noise estimation and tests

The experimental results indicated that the noise in the photodiodes and their current measurement systems could be overcome by repeated sampling of the diode photocurrent as is typically used in sensor systems (although not in digital transmission photo diode systems, where error control is used). A brief review of photodiode characteristics and a noise analysis was conducted [39]–[41], [76].

The responsivity, refers to the measure of the photodiode's sensitivity to light, of the north photodiode is 0.53 A/W at 650nm using

$$R_\lambda = \frac{I_P}{P} \tag{4-1}$$

where P is the incident light power at a given wavelength.

The total noise current generated in a photodetector is determined by

$$I_{tn} = \sqrt{I_{sn}^2 + I_{jn}^2} \quad , \tag{4-2}$$

where I_{sn} is the shot noise, which is related to the statistical fluctuation in both the photocurrent and the dark current, and it is given by:

$$I_{sn} = \sqrt{2q(I_P + I_D)\Delta f} \quad , \tag{4-3}$$

where q is the electron charge, I_P is the generated photocurrent, I_D is the photodetector dark current, and Δf is the noise measurement bandwidth.

While the thermal or Johnson noise I_{jn} is due to the shunt resistance in the photodetector due to the thermal generation of carriers:

$$I_{jn} = \sqrt{\frac{4k_B\, T\, \Delta f}{R_{SH}}}\,, \tag{4-4}$$

where k_B is the Boltzmann Constant, T is the absolute temperature at 273 K, and R_{SH} is the shunt resistance of the photodiode. Shunt resistance is the slope of the I-V characteristics curve of a photodiode at zero bias, experimentally, the value is obtained when voltage is introduced at V=0±10mV value. An ideal photodiode should have an infinite shunt resistance; however, actual values vary greatly. The higher shunt resistance values are more desirable, as the overall Johnson noise gets reduced [39]–[41], [76].

Table 3: Dark current, saturation current, and shunt resistance of the North, East, South, and West photodiodes on one pixel.

Device	North	East	South	West
Dark Current [μA]	-2.17	-2.19	-2.20	-2.18
Saturation Current [μA]	-8.14	-8.14	-11.79	10.04
Shunt resistance [Ω]	2804.64	2255.21	2468.24	2664.98

Dark current, saturation current, and shunt resistance of the North, East, South, and West photodiodes on one pixel were calculated from the experimental measured characteristics, when the pixel is placed in a dark setting and when light from an optical microscope (under constant illumination conditions) is introduced. Table 3 is a summary of the photodiode characteristics in one pixel, i.e. dark current, saturation current, and shunt resistance of the North, East, South, and West photodiodes.

The Noise Equivalent Power (NEP) is the amount of incident light power on a photodetector, which generates a photocurrent equal to the noise current, and it is defined as:

$$NEP = \frac{I_{tn}}{R_\lambda} \tag{4-5}$$

The noise equivalent power is found to be 3.65 μW/Hz$^{1/2}$. NEP values can vary greatly depending on the photodetector size and active region, values from 10^{-11} W/Hz$^{1/2}$ for large active area photodiodes down to 10^{-15} W/Hz$^{1/2}$ for small active area photodiodes are typical [40], [41]. Characterization for the inverse design including the brief error analysis were found to be close to the mesa design for similar average active areas and illumination.

Figure 4-5 shows the actual and measured values of the rotational and inclination angles are presented as the inclination angle as incident ambient light is projected and varied from between -80° and 80°, and the angle of rotation in 360°, respectively. The average for measured angles for true inclination angle -80° are -75.49° with standard deviation of 0.71°, The average for measured angles for true rotational angle 45° are 43.05° with standard deviation of 0.63°. Thus, the experimentally estimation of angular proximity in 2D is demonstrated [37].

4.5. Laser Beam Induced Current Tests

4.5.1. Method applied to each pixel

A focused laser beam (HeNe, 633nm wavelength, <1 mW) is scanned across the p-n junction on a planar surface of the device in order to estimate the dimensions of the n-doped region profile on a planar surface. By reverse biasing the substrate as the laser scans across the p-n junction, laser beam induced current is measured at each point across the scanning path. The induced current can provide an approximation of the region dimensions. A laser scan through the flat (100) region starting at the p-region across the n-region and ending the scan at the p-regions gives an approximate width of the n-doped region in the flat region. A laser scan starting at the top of the n-doped slanted (111) region and ending at somewhere in the n-doped region at (100) would indicate any discontinuities in n-doped region as well as a better profile of whether the doped region is uniformly doped. Discontinuities in the non-doped regions, or areas where n-diffusion did not occur at all, could be the result of photoresist non-uniform distribution (for example accumulations of photoresist at the bottom of the pyramid. figures 3-16 to 3-19) leading to areas of the photoresist not properly developed, and subsequently the oxide not being etched, thus, the remaining oxide layer would act as a mask during the n-diffusion step, where masked regions would not get exposed to n-diffusion. As laser illumination approaches a p-n junction edge, a portion of the junction actively separates photo-generated carriers, thus, providing local diffusion flow of majority electrons into the n-type region and majority holes into the p-type region. This causes a forward-bias like behavior and an increased potential in the active area, represented in Figure 4- by a peak negative induced current value with respect to the laser position at the edge of the n-region. As the

laser is approaching the opposite edge, an opposite effect of carriers diffusion occurs at the n-p junction, represented by a peak positive current value, indicating the end of the n-region. On the other hand, the laser is scanned across an n-doped region starting from the top of the <100> planar surface of a facet down towards the <100> planar surface in order to as ensure the angled <111> facet and the planar <100> region are connected and continuously doped, A relatively uniform doping profile across the two surfaces is expected, as intrinsic diffusion coefficient of dopants is independent of wafer orientation, and crystal defects, which may promote diffusion, are negligible in silicon although the wet etch process may create surface irregularities promoting diffusion [75], [84], [85] .

Light penetration into the surface is characterized by the mean-free path of generated minority carriers, which is given by their diffusion length, and the overall current in the segment is proportional to the inverse minority carriers diffusion length. As the laser scan starts from the top of the facet, the approximation of a two-dimensional carrier transport on the slanted surface is valid, and the overall variation in carrier concentration occurs at a continuously increasing minority-carrier diffusion lengths in, at least, one dimension in that region, thus decreasing the overall current as the laser scans the slanted area towards the base of the pyramid, equation 4-6,

As the laser approaches the wide base of the pyramid and the rest of the <100> substrate surface, light penetration into the surface is only dependent on one-dimensional carrier transport, thus, generating an overall lower induced current relative to the angled regions, [39], [86]–[91]. The laser induced current is proportional to the characteristic diffusion length [90], [91] by :

$$|I_{LBIC}(x,y,z)| = k\ exp\left(-\frac{\sqrt{x^2+y^2+z^2}}{L_P}\right) \quad (4\text{-}6)$$

Where k is the proportional coefficient, and x,y, and z represent the location from

laser spot location to the boundary of p-n junction.

Laser scans did not detect any discontinuities within the doped region, which is a good indication that there were possibly no photoresist or oxide accumulations at sides of the pyramid during the diffusion process.

In equation 4.6, the penetration depth location at position (x,y,z) can be used to indicae of the inclination angle of Si. The laser is scanned within the n-doped region in the (100) surface when the device is not tilted and when the device is tilted at 10, and 30. The (z) variable is constant, since the laser is incident within the flat (100) region. The penetration depth in Si should be constant, regardless of the tilt angle, so (y) should stay constant, and the only variable is (x), which denotes the distance separating the light projection and the regions containing high concentration of minority carriers. Thus, x changes significantly and affects the overall induced laser current due to the angle at which Si is tilted. The changes in induced current to the defocusing laser as it scans across an elevation of 15um, the height of the pyramid is around 15um, are insignificant relative to the changes sure to tilt angle. Changes in induced current due to focusing the laser then defocusing it on the same flat 100 region are measured to be around 20nA. In addition, focusing/defocusing the laser in the (111) region also induces a change at around 20nA. However, induced current changes are in the microamp range.

4.5.2. Laser beam experimental setup and results

An image of the experimental setup for the laser beam induced current measurements is shown in Figure 4-6. A laser is scanned across the sample in several directions, where current-voltage measurements are recorded to detect response variations due to incident light.

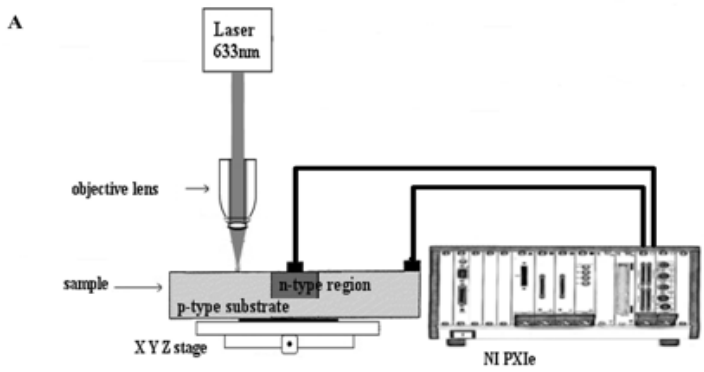

Figure 4-4: Experimental setup for the laser beam induced current measurements. A laser is scanned across the sample in several directions. IV measurements are recorded (National Instruments PXIe) to detect response variations due to incident light.

Since the previous results confirm that the (111) facets are n-doped and that there are no discontinuities in the n-doped region in the area connecting the (111) facet and the (100) flat region, the width of the n-doped region on the flat surface can be approximated using the laser scan. When laser is scanned across p-region - n region - p-region, the current changes at the edges of the doped regions. Figure 4-8 shows the induced current measured and normalized as the laser is scanned laterally across the pn-junction on the flat surface (path (d) in figure 4-7). The width of the n-doped region on the flat surface can be estimated to be 63.86 +/- 4.12 μm. The estimation can be compared with the diffusion area visible in the SEM image in Figure 4-1 (A), which is estimated to be 70 μm.

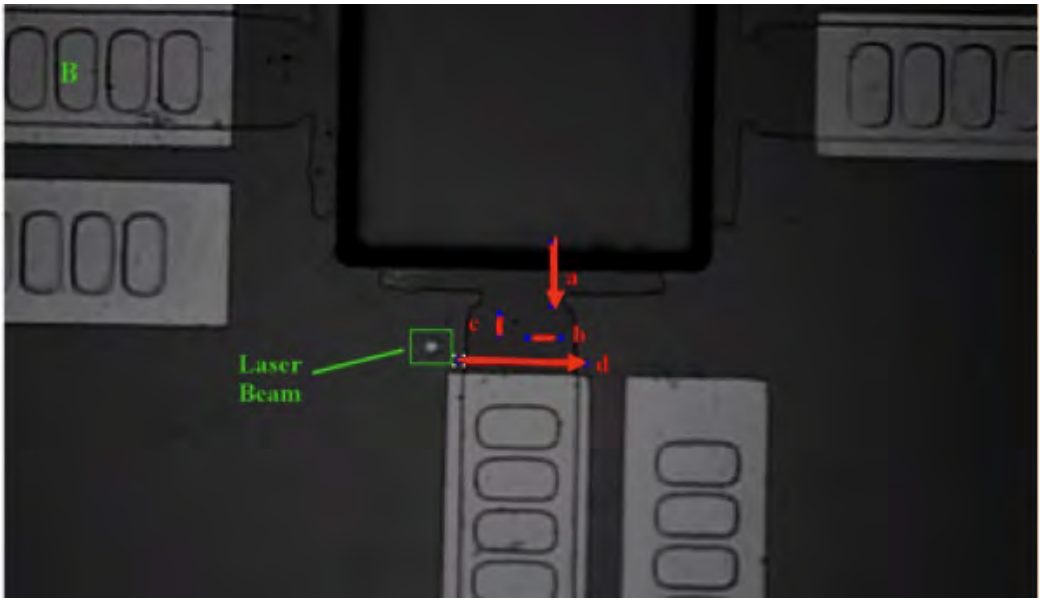

Figure 4-5: Induced current measurements following laser beam paths and variations across the pyramid structure and along doped regions. The laser beam is used to approximate doped region depths, as well as an indicator of doped region continuity.

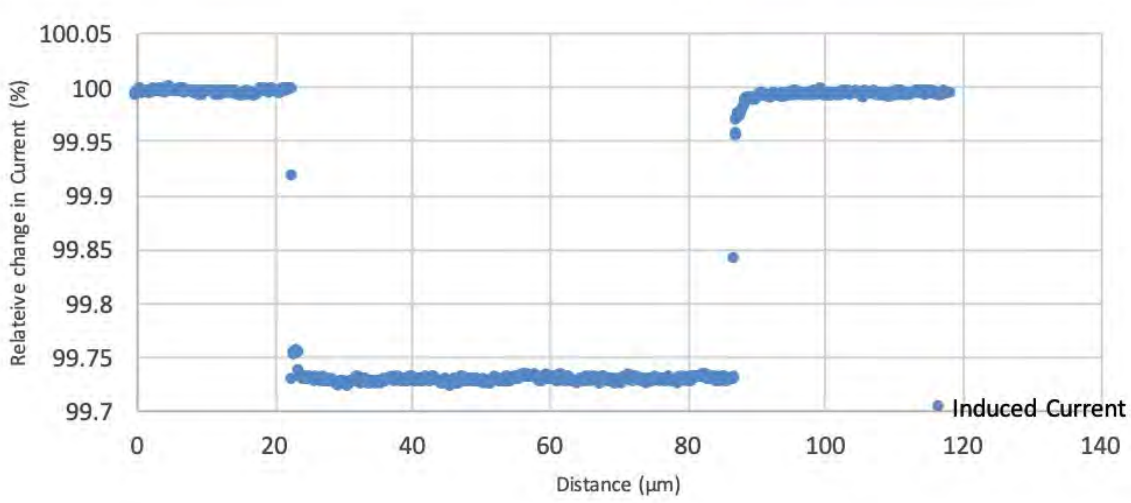

Figure 4-8: The laser is scanned across an npn doped region at a 90° angle (direction d in Figure 4-7). Schematic of laser beam at tilted angels. The scan profile indicates the depth width at an approximate width of 70um,.

The laser beam is then scanned from the top side of the facet towards the flat portion of the diode (Figure 4-7 path(a), when the sample is horizontal and when the sample is tilted. Figure 4-9(A) shows the induced current measured and normalized at tilt angles 0°, 10° and 30°. The laser is also scanned laterally across the facet with base angle 54.7° and compared to the scan in Figure 4-9(A).

The laser was scanned within the flat region of the n-doped region (Figure 4.7 paths (b), (c)), when the sample is horizontal and when the sample is tilted. Figure 4-9(B) shows the induced current measured and normalized at tilt angles 0°, 10°, and 30° when the laser is scanned laterally (Figure 4-7 path (b)). The relative change in induced current is insignificant, as shown in Figure 4-9(B). Minimal to no change in induced current, is expected, since the laser is scanned horizontally, along the z-axis direction, while x and y components remain unchanged (path (b) in Figure 4-7).

Since the n-doped region is relatively uniform, the change in induced current as the laser is scanned along path (a) is mostly due to laser being scanned at an angle, the inclination angle of Si. Thus, based on induced current measurements, an unknown inclination angle can be extrapolated. The profile indicates the pyramid height at 15um, as measured by a profilometer.

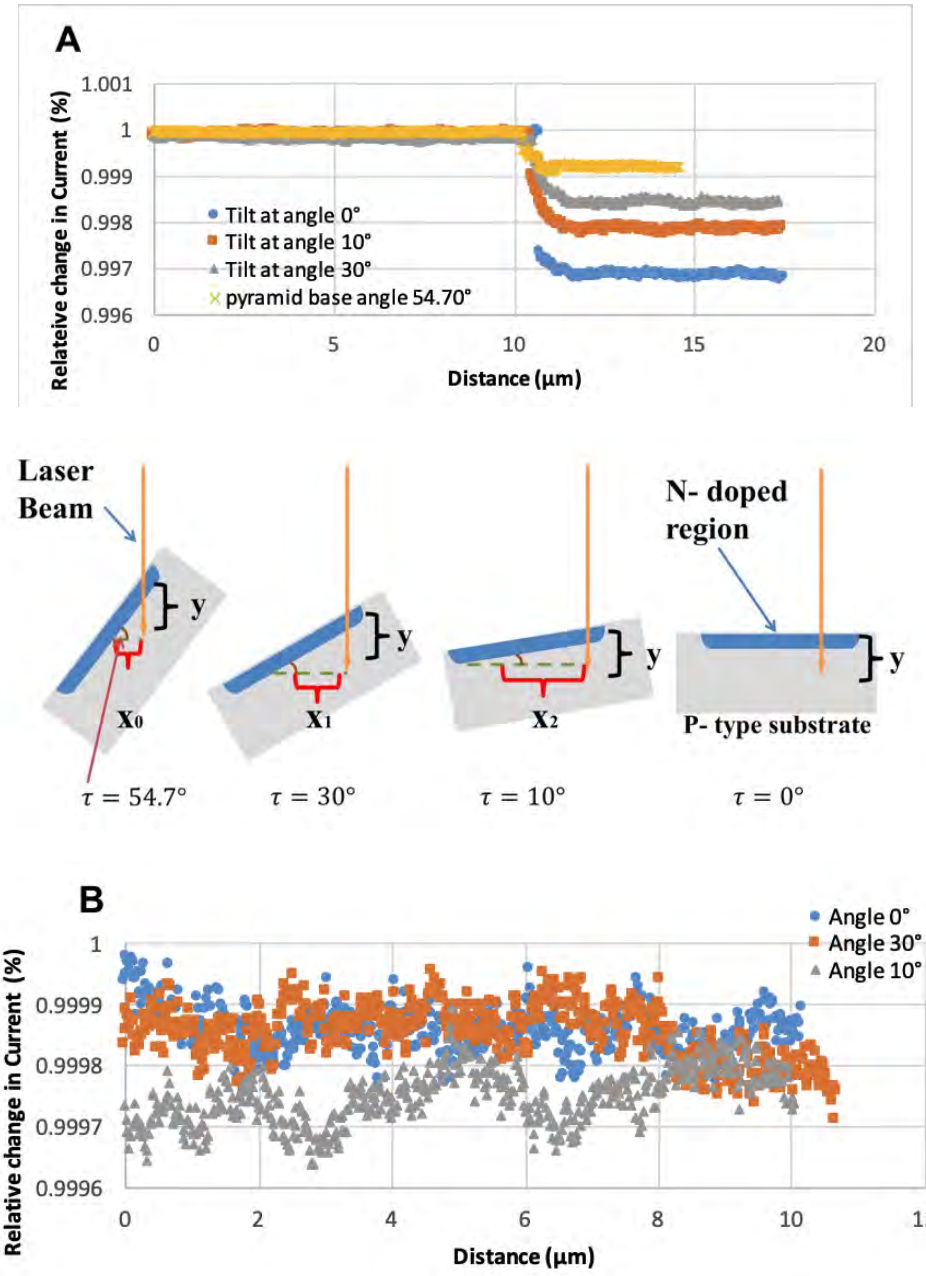

Figure 4-9: Laser beam induced current measurements and induced current measurement as the laser beam is scanned across different directions of a facet in doped regions on the pyramid. In A, the current is measured across the pyramid (direction a in Figure 4-7), as the pyramid is titled at angles 10°, 30°, and 54.7°, as shown in the schematic. The relative change is measured against at pyramid at 0° (no tilt). In B, the laser is scanned within the flat region (direction b in Figure 4-7), while holding z constant.

4.6. Summary of Results

A single mesa pyramid in itself is demonstrated to detect the inclination and rotational angles of an incident light source, thus, providing a spatial proximity in 2D. A laser beam is used as a preliminary method of estimating the dimensions of the n-doped region profile on planar and tilted surfaces scanned. Scanning the laser across a p-n junction can help detect disconnections or un-uniformities in doped regions, indicating issues during the microfabrication process. The method can be used as a quick indication of the effectiveness of the microfabrication steps on angled as well as etched surfaces.

5. Carbon-Based Composite Alternatives

5.1. Fabrication of Micro-Bolometers for long wave IR sensing.

One of the applications of the Si-based optical sensors is their integration within sensor systems for wide detection range applications, well beyond Si's 700 and 900 nm range. Since one of the applications also included long wave IR detection, suitable materials for such integrations were investigated, to be used as potential thermal layer add-ons to the Si sensor.

Multi-walled carbon nanotubes and graphene based films have been demonstrated to have moderate temperature coefficient of resistance (TCR) and wideband IR absorption efficiency [124]. It has been demonstrated that by incorporating these nanoparticles into a thermally and electrically insulating polymer, polystyrene, the temperature sensitivity increases in Multi-walled carbon nanotubes and graphene based films. The layers were deposited using a spraying setup without further chemical or thermal treatment. The low cost, simple, and versatile deposition process, in addition to the experimental TCR values demonstrated for these films make them a suitable for infra-red image sensors. They can also potentially be integrated with hybrid solar cells (HSCs), where the thin film or composite layer can act as a window layer to reduce reflections as well as a front electrode for the Si-based optical sensors.

5.1.1. Carbon-Based Composite

Carbon based nanomaterials, particularly graphene and carbon nanotubes (CNTs), have attracted increasing interest in thermal sensing applications due to their remarkable electronic and thermal properties, as well as their photo-response in the infrared (IR) range.[92]–[95] However, the properties of multi-wall CNT (MWCNT) and graphene films vary greatly depending on the deposition process.

Despite being the main method of growing carbon based thin films on various substrates, chemical vapor deposition (CVD) of carbon is not considered compatible with many fabrication processes for microsystems, mainly due to the high deposition temperatures, typically ranging between 500 and 900°C. Other complications in the integration of the deposition process arise from the required pre-processing steps (e.g., generation of nucleation sites). In the case of CNTs, the deposition technique can be tuned to produce multiwalled or single- walled nanotubes on a variety of substrates.[96]–[98] Films of graphene can also be produced by high temperature annealing or chemical reduction from graphene oxide [99]–[102]. Most of the deposition processes are used to obtain isolated individual and multilayered sheets or ultrathin films.

Various thermal, conducting, electrochemical, and optoelectronic device designs and properties have been demonstrated for such films [95], [100], [103]–[105], especially with the advantages of reduced fabrication costs and complexity. Drop casting, spraying, dip coating, inkjet printing, and vacuum filtration were demonstrated as alternate deposition methods [101], [102], [105]–[107]. In many of these techniques, the carbon nanoparticles are transferred onto a substrate in the form of a solution or suspension within a solvent, where the nanoparticles are integrated within polymer based composites deposited onto substrates, followed by a low temperature process to evaporate the solvent

or cure the composite. Polymers with varying properties, polycarbonate, [106] polystyrene (PS), [101], [102] SU-8,[108], poly(ethylene oxide) and poly (methyl methacrylate)[6], [98], [109], have been used to prepare carbon based nanoparticle composites. In the case where the nanocomposite material needs to be electrically conductive, the concentration of nanoparticles within the solution needs to be above the percolation threshold, [98], [101], [102], [110], [111]. For example, in order to deposit graphene films, one approach is to deposit non conductive graphene oxide (GO) films, then chemically or thermally reduced, in order for the films to become conductive. In addition, reducing uniformly deposited GO thin films with a controllable number of layers was demonstrated to have a fraction of the optimal electrical, chemical, and structural properties of that of monolayer graphene. The reduction of GO films usually involves annealing at high temperatures, and/or the use of wet chemicals in several chemical reactions in order to try and reduce the functional groups bound to graphene [88], [97], [100]–[102], [106]. On the other hand, CNT deposition may be based on whether the material is multi-walled or single-walled, though uniform SWCNT networks of varying densities have been mostly deposited using the vacuum filtration method. While vacuum filtration offers advantages like optical transparency and film thinness and uniformity, the samples may have to be transferred after being vacuumed to a substrate, in addition to being washed and etched to achieve the desired uniformity [92], [103], [104], [107]. Most of the deposition processes are used to obtain isolated individual and multilayered sheets or thin films deposited over large areas.

Adding an electrical and thermal insulating polymer, such as polystyrene, reduces the thermal cross-linking between CNT/ graphene particles, thus, increasing the conductivity within the films. In addition, the nanoparticle composites provide an enhanced

mechanical durability to the films, without completely sacrificing graphene's or CNTs' electrical, chemical, and structural properties [94], [97], [98], [109], [110], [112], thus, allowing them to be used in a wider range of applications.

Uncooled thermal IR detectors such as microbolometers offer a number of advantages over cooled detectors, including simple manufacturing processes, compact design, as well as their relatively lower power consumption, making them desirable in a subset of commercial and military applications as low cost detectors. In addition the thermal and electrical properties of the composites and thin film materials allow for cost effective integration of the modules within solar applications, such as hybrid solar cells [112]–[114].

Materials with higher temperature coefficient of resistance (TCR) values are preferred as higher variations in the resistance of materials due to changes in temperature provide a stronger signal response. Vanadium oxide in its different oxidation states (such as VO_2, V_2O_3, and V_2O_5) is commonly used as a micro- bolometer sensing material, with TCR values at around 2%/K at room temperature for sputter deposition samples [115], [116].

In this chapter, a cost effective controlled spray deposition technique is used to deposit multilayered graphene and MWCNT thin films and composites. The resistance variations of the films due to changes in temperature were measured, and a TCR for the films has been calculated for each film. Experimental results demonstrate the TCR values as high as -0.7%/K for five layers spray deposited graphene/PS films.

Figure 5-1. Low deposition processes allow for the deposition of carbon-based nanocomposites and VOx thin layers on 3D structures in Si, polymer, or other materials where layers can be used as single layers or parts of multilayer devices, including a layer of air, vacuum, polymers, or other materials.

5.1.2. Experimental Setup

Figure 5-2 shows a diagram of the air pressure spray system used, where solutions outflow through an airspray nozzle. Simulations suggest that air spray pressure follows a distribution curve where most of the deposition occurs at the center of the circle in a theoretical circular conical distribution. The probability of deposition of particles along the edges of the cone decreases as the distance from the center of the circle increases. The center of the cone has the highest concentration of deposited particles. The variables that control the spraying deposition process include the nozzle-substrate separation distance, pressure at which air inflows into the nozzle, solution viscosity, particle size, spraying velocity, and the temperature at which the deposition takes place [63], [64].

MWCNT and graphene films and composites using polystyrene (PS) as the base polymer were prepared. The nanoparticles were uniformly dispersed in a solvent or polymer solution and deposited onto a glass slide using spray deposition. Glass slides with metal electrodes were used as substrates, and a 3D printed shadow mask was used to obtain resistors of different dimensions.

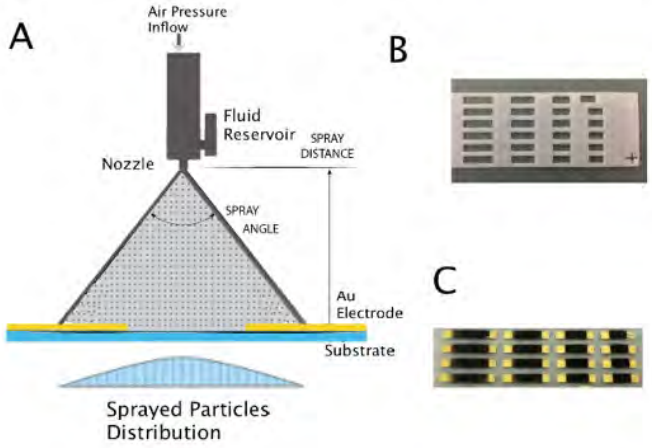

Figure 5-2. (A) schematic of the spray deposition process; (B) Stencil mask for resistors of different length and width; and (C) Deposited resistors on a glass substrate with gold electrodes.

The nanoparticle suspensions were deposited at controlled pressure, temperature, and spraying speeds to achieve controlled thin film depositions. COOH functionalized multi- walled carbon nanotubes powder (MWNT 95% 20–30 nm in diameter obtained from Cheap Tubes, Inc.) was dispersed in toluene using high-energy sonication with an ultrasonic horn (Fisher Scientific 550) at 150 W for 15 min.16 This resulted in a MWCNT suspension with 2.7% w/v concentration. Graphene (flakes 6–8 nm sized platelets nanopowder, >99.5% purity from SkySpring Nanomaterials) suspensions with concentrations of 1.5% w/v and 2.7% w/v were prepared in a similar manner to the MWCNT solution. The films were deposited on glass substrates according to the following procedure. The PS solution was prepared by dissolving PS beads (190,000 Mw from Scientific Polymer Products) in toluene and stirring at 60 C to have a concentration of 10% w/v solution. MWCNT-PS and graphene–PS solutions were prepared by adding MWCNT

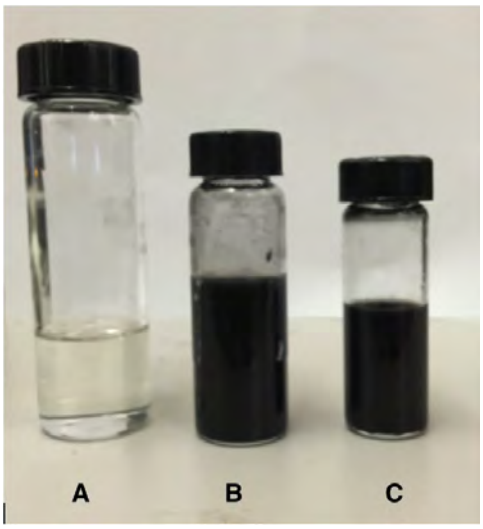

Figure 5-3. A. The polymer solution consists of polystyrene beads dissolved in Toluene. B. Graphene (monolayers flakes) are dissolved in Toluene to prepare the graphene solution. C. Multi-walled carbon nanotubes (powder) are dissolved in Toluene to prepare the MWCNT solution.

and graphene suspensions to PS solutions at ratios 0.77:1 for PS:graphene and 0.69:1 for PS:MWCNT. The resulting solutions were mixed using an ultrasonic probe for 10 min. Adding PS at a higher concentrations and ratios causes the film to lose its uniformity and become brittle, causing the films to flake off the substrate during subsequent steps. In addition, high PS concentrations cause cracks in the film, thus causing the composite to lose its conductivity. The samples were deposited on a glass substrate with gold electrodes. The few nanometers thick electrodes were deposited by thermally evaporating gold on top of a chromium layer on glass substrates. Samples were prepared at several dimensions, Fig. 5.1C. The thickness of the deposited films were measured using a profilometer.

After the deposition of films between the metal electrodes, the temperature coefficient of resistance was calculated from:

$$\alpha = \frac{1}{R_0}\frac{\Delta R}{\Delta T}$$

where R_0 is the initial resistance at the reference temperature, ΔR is the change in resistance, and ΔT is the change in temperature.

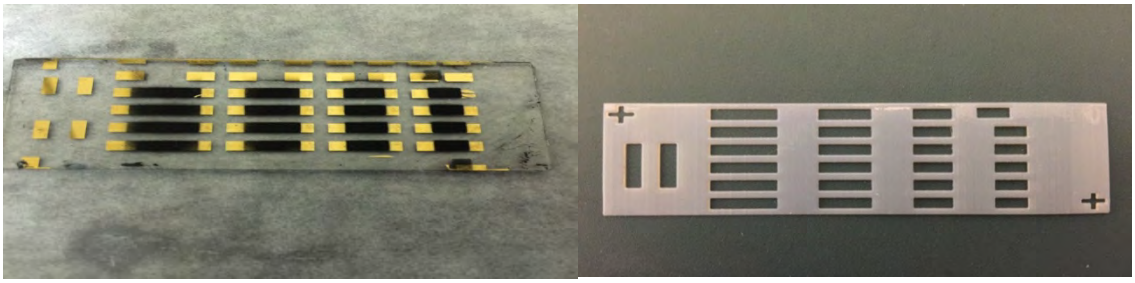

Figure 5-4. Left: Sample: graphene layers are spray deposited onto a glass slide with pre-deposited electrodes with varying gap ranges between 1 cm and 5cm. A stencil mask (right) is used to deposit graphene within the electrodes to create thermoresistive films.

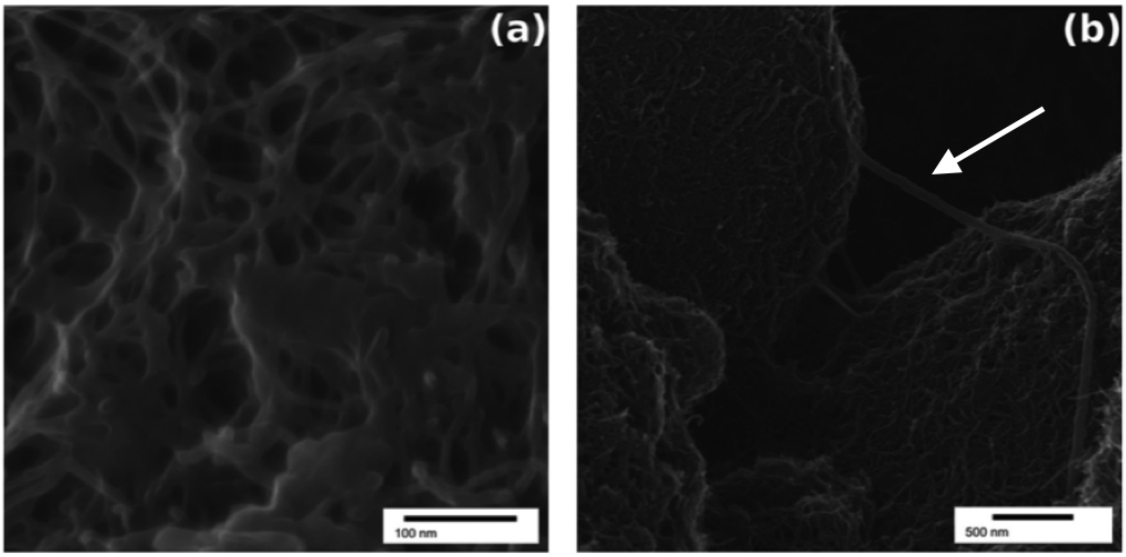

Figure 5-5. SEM images of MWCNT PS nanocomposites. (a) PS addition provides added interconnected layers of MWCNT-embedded polymer layers. (b) The clusters of nanotubes are interconnected by layers of MWCNT, ensuring conductive paths between clusters.

5.2. Results: Carbon-Based Films and Composites

5.2.1. Multiwalled Carbon Nanotubes films and composites

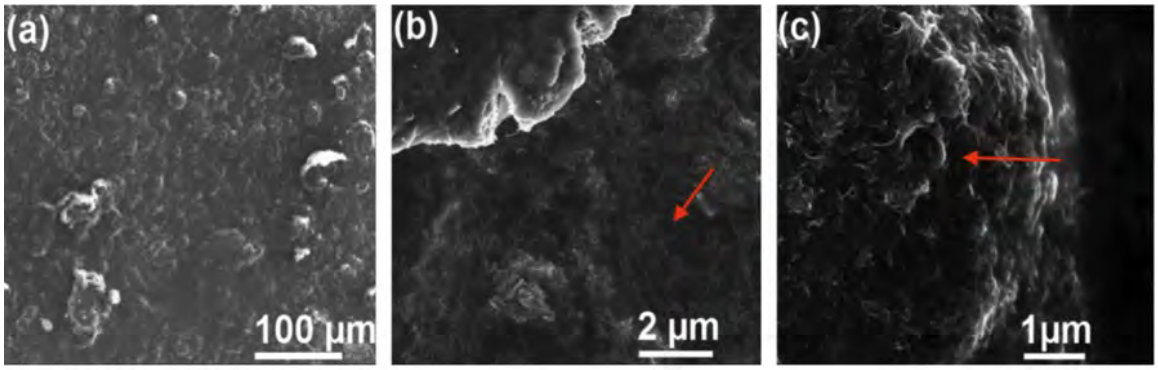

Figure 5-6 (a) SEM images of MWCNT embedded and randomly distributed in polystyrene at different resolutions of (a) 100 um, (b) 2 um, and (c) 1 um. Adding PS tends to cause the nanotubes to cluster together.

Experimental results indicate that in all cases, the films mixed with polystyrene exhibited significantly lower sheet resistances compared to films of nanoparticles. The addition of thermally and electrically insulating polystyrene results in lower sheet resistances for the deposited MWCNT and graphene films. The nanotubes are randomly oriented in PS, as most of the nanotubes appear to be in clusters and are embedded within the polymer. The significant decrease in the MWCNT/PS films' resistance can be attributed to percolation of nanoparticles where a conductive path for the current between the two electrodes is established through the networks of connected nanoparticles and increased thermal conductivity of the polymer–nanoparticles matrix. Due to the random nature of the distribution of nanoparticles, a minimum concentration of nanoparticles is required to warrant conduction. When mixed with a polymer, the viscous forces between the polymer and nanoparticle contribute to two effects [112]. The first effect is the increase in the potential pathways between the two ends of a nanocomposite as the nanoparticles

are brought together during solvent evaporation and curing, as shown in Fig. 5.5. On the other hand, the same forces typically lead to the formation of clusters of nanoparticles which, due to the high concentration of nanoparticles within them, will have high conductivity. These clusters can then be connected to each other through few nanoparticles, as shown in Fig. 5.6, lowering the overall resistance of the film significantly [112]. Graphene also appear to be randomly oriented in the films containing PS.

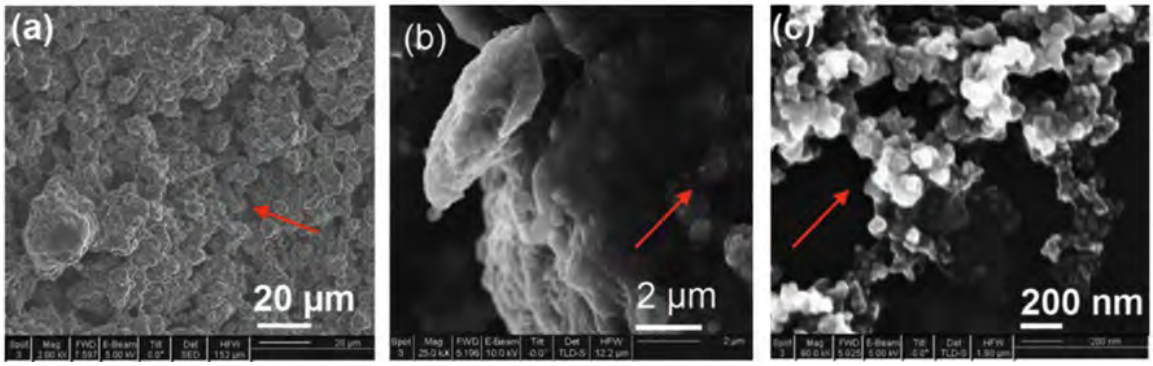

Figure 5-7. (a) SEM image (20 µm resolution) of graphene–PS multilayer film. The gap between graphene flakes increases when polystyrene is introduced. (b) SEM image (2 µm resolution) showing graphene flakes integration with the polymer at higher magnification. The nanoparticles appear as flakes embedded in polystyrene. (c) SEM image (200 nm resolution) of a multilayer graphene film. Accumulation of flakes is visible on top the film's layer of smaller flakes.

While PS acts as a thermal and electrical insulator, due to the large concentration of PS in solution, the hydrophobicity of PS pushes away the conducting nanotubes, due to hydrophobic forces, causing the nanotubes to stack and cluster. In addition, MWCNT allocate in films due to the Van der Waals and electrostatic interactions as well as esterification. Esterification is the formation of ester bonds between MWCNTs due to carboxylic acid function groups at the walls of the nanotubes reacting with each other in the presence of toluene, thus forming larger clusters. The random orientation of MWCNT as well as their allocation in films allows the application of the percolation theory of a

random distribution of conducting tubes. The insulating polymer becomes conductive with the formation of conductive nanotube networks within the polymer; CNT concentration surpasses the percolation threshold, the critical concentration required for the insulating polystyrene solution to become conductive [108], [117]–[121].

Figure 5-6 shows SEM images of MWCNT and MWCNT/ PS films. The nanotubes are randomly oriented in PS. Most of the nanotubes appear to be in clusters and are embedded within the polymer. Figure 5-8 shows the relationship between the films' thicknesses and the deposited number of layers. By controlling the deposition parameters discussed earlier, thicknesses of films consistently increase with the number of deposited layers. Measured sheet resistance of deposited layers of MWCNT (for both 1.5% w/v and 2.7% w/v densities) decreased significantly when PS was added. Figure 5-8 shows the thickness of spray deposited MWCNT (2.7% w/v) and MWCNT-PS (2.7% w/v) measured against deposited number of layers in films. As temperature increases, the sheet resistance of both MWCNT films and MWCNT/PS films decreases as long as the temperature of the films is below the glass transition temperature of polystyrene (at T_g = 65.0 °C [122]). An increase in the temperature causes an increase in the thermal generation of carriers, resulting in an increase in the conductivity of the nanoparticles, thus a decrease in the sheet resistance of the films [106], [112]. When the nanoparticles are embedded within the polymer film, the restructuring of conduction network due to thermal response of the polymer should also be considered. However, as the temperature of the film approaches the glass transition of PS at 340 K, the polymer softens, contributing another factor to the electrothermal response of the films [122].

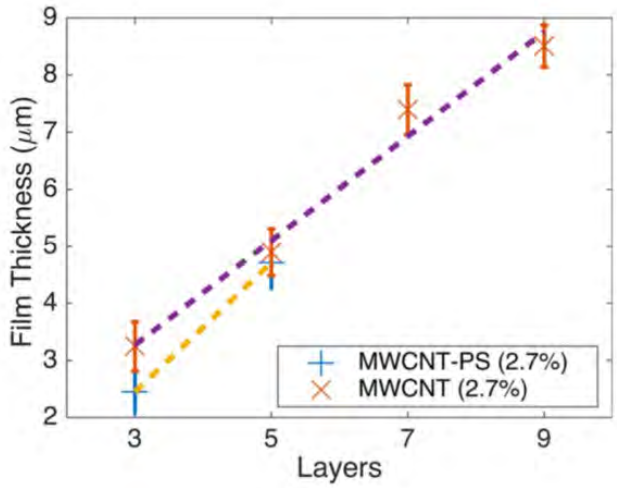

Figure 5-8. The thickness of spray deposited MWCNT (2.7% w/v) and MWCNT-PS (2.7% w/v) are measured against deposited number of layers in films. The average thickness of the films increases consistently when more layers are deposited.

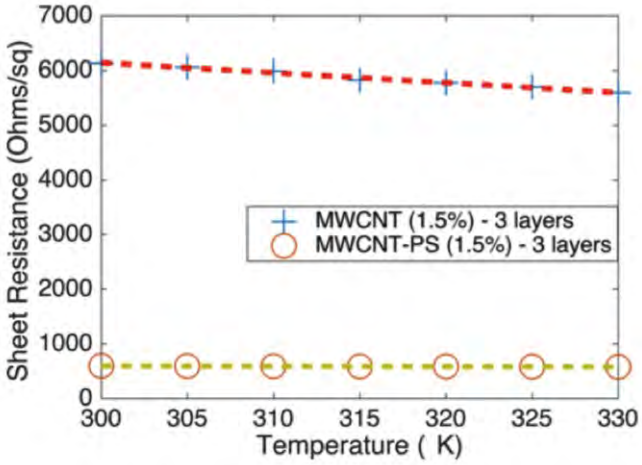

Figure 5-9. Sheet resistance variations of three layered spray deposited MWCNT (1.5% w/v) films are measured along temperature variations when PS is added to the solution. The overall resistance of the films decreases significantly with the addition of PS. Both films have a negative TCR.

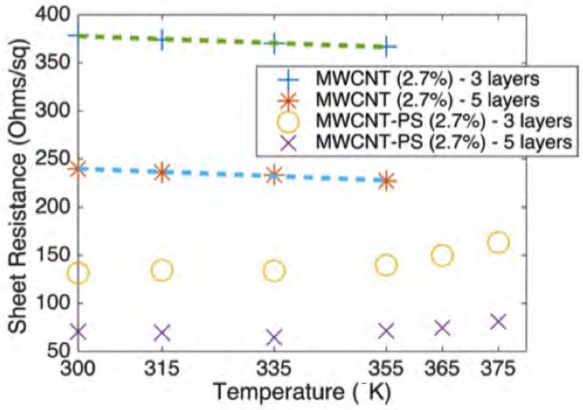

Figure 5-10. Sheet resistance variations of three and five layered spray deposited MWCNT (2.7% w/v) films are measured when PS is added to the solution across several temperatures. The overall sheet resistance of the films decreases with the addition of PS. Films have a negative TCR value, up until the glass transition temperature of polystyrene (340K), where the TCR becomes positive.

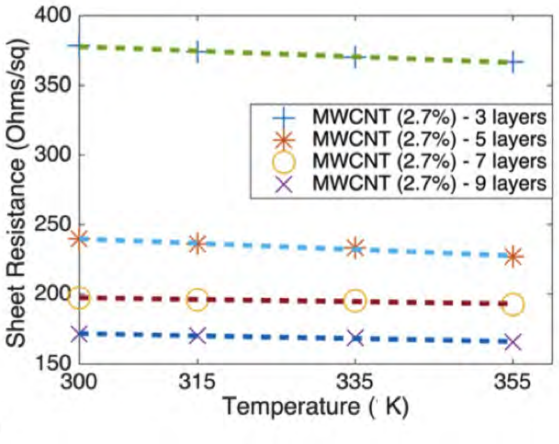

Figure 5-11. (Color online) Sheet resistance variations of 3, 5, 7, and 9 layered spray deposited MWCNT (2.7% w/v) films are measured against temperature variations. The overall sheet resistance of the films decreases with the addition of more layers.

Figure 5.11 is a plot of the sheet resistance variations MWCNT-based when PS is added to the solution. When the temperature of the composites exceeds the glass transition temperature of the polymer matrix, their resistivity increases [123]. This causes the films to have an overall positive TCR values at high temperatures. However, when the

temperature of the films is well below Tg of PS, MWCNT and MWCNT/PS films have a negative TCR. The effect of increasing the number of layers on the thermal response of the films was also studied. Increasing the number of layers increases the overall concentration of the conductive nanotubes within the films, thus, decreasing the overall resistance in the films, as expected.

Number of layers	MWCNT (1.5% w/v)	MWCNT (1.5% w/v) + PS	MWCNT (2.7% w/v)	MWCNT (2.7% w/v) + PS
3	−0.10	−0.30	−0.055	−0.096
5	−0.095	−0.30	−0.092	−0.049
7	—	—	−0.041	—
9	—	—	−0.060	—

TABLE 5-I. Experimental TCR values as well as the average film thickness for MWCNT-based films (%/K) for temperatures below Tg of polystyrene.

The concentration effect of the conductive particles in the films is more clearly shown when the sheet resistance of three layers of MWNCT film of 1.5% w/v density (Fig. 5.5) is considerably lower than that of the three layers of MWCNT films of 2.7% w/v density (Fig. 5.7). Table I summarizes the data from MWCNT-based films.

Number of layers	Graphene (1.5% w/v)	Graphene (1.5% w/v) + PS	Graphene (2.7% w/v)	Graphene (2.7% w/v) + PS
3	−0.37	−0.16	−0.45	−0.62
5	−0.37	−0.16	−0.66	−0.69
7	−0.31	—	−0.35	−0.58
9	−0.31	—	−0.36	−0.35

TABLE 5-II. Experimental TCR values as well as the average film thickness for graphene-based films (%/K) for temperatures below Tg of polystyrene.

Table 5.II compares the TCR values obtained for various combinations of graphene-based films. Both graphene and graphene/PS films exhibited higher TCR values when compared to MWCNT or MWCNT/PS films. On the other hand, in contrast to MWCNT-based films, the magnitude of TCR values of graphene and graphene/PS films decreases when more layers are deposited. The highest measured TCR is that of the five-layer film of graphene/PS with a TCR of -0.7%/K.

5.2.2. Graphene films and composites

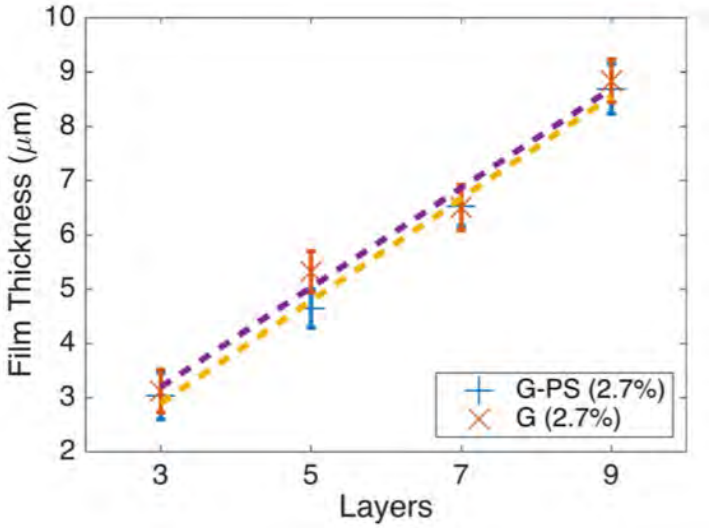

Figure 5-12. Thickness of spray deposited graphene (2.7% w/v) and G–PS (2.7% w/v) films. The average thickness of films increases consistently when more layers are deposited.

On the other hand, Figure 5-8 shows SEM images of graphene as well as graphene/PS films. Figure 5-9 shows the increase in the films' thicknesses as more layers are deposited. Depositing graphene at lower (1.5% w/v) concentrations results in a better distribution of graphene flakes across the sample, causing the film to become more uniform than at higher concentration (2.7% w/v). As a result, films made with lower graphene concentration exhibited a lower sheet resistance as expected, Fig. 5.10.

Increasing the number of layers decreases the resistance in films at both concentrations, with the low graphene concentration films having the lower resistance as seen in Fig. 5.11. As more layers are deposited, graphene based films start exhibiting the electrical thermal properties of that of graphite based films [124].

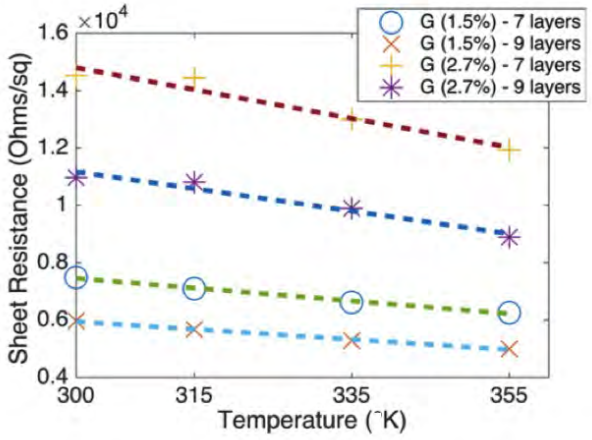

Figure 5-13. Sheet resistance variations of seven and nine layered spray deposited graphene at two different densities (1.5% w/v 2.7% w/v) are measured against temperature variations. The overall sheet resistance in films with lower density is lower than the overall sheet resistance of higher densities. All films have a negative TCR value.

When polystyrene is added, graphene flakes become embedded within the polymer. This causes the resistance of the films to decrease significantly, as shown in Fig. 5.12. The decrease in resistance in graphene/PS films can also be attributed to percolation between the nanoparticles and the interconnection between accumulated graphene flakes due the viscous polymer [100]–[102], [108], [110], [112], [125]. Figure 5-12 compares the thermal responses of nine-layer graphene-based films and MWCNT/PS composite. Adding PS to these films causes the films to have higher resistance, since the concentration of the insulating polymer is high enough to decrease the contact between individual graphene flakes. Higher PS concentrations becomes less of an issue when more layers, containing

more graphene flakes, are deposited causing graphene flakes to stack, thus decreasing the overall resistance in the films.

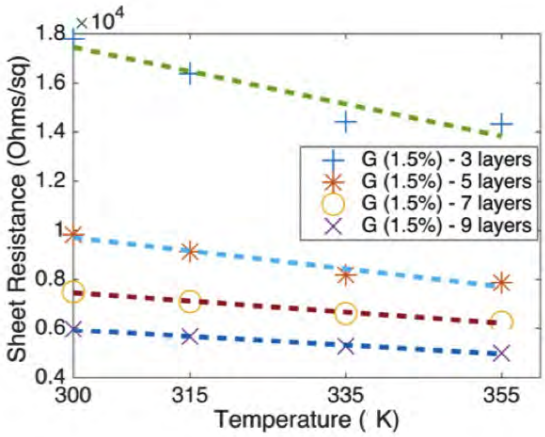

Figure 5-14. Sheet resistance variations of 3, 5, 7, and 9 layered spray deposited graphene (1.5% w/v) films are measured against temperature variations. The overall sheet resistance of the films decreases with the addition of more layers. All films have a negative TCR value.

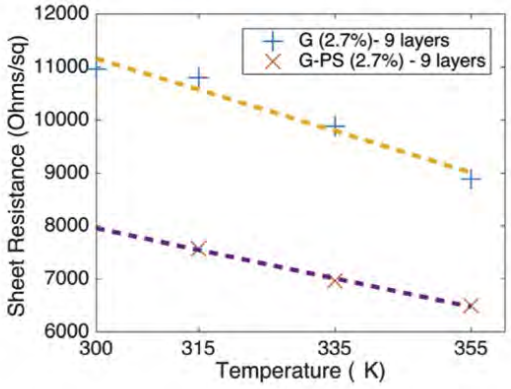

Figure 5-15. Sheet resistance variations of nine layered spray deposited graphene (2.7% w/v) films are measured against temperature variations, as PS is added to the solution. The overall resistance of the films decreases significantly with the addition of PS. Both films have a negative TCR.

5.3. Vanadium Oxide Thin Films

Concurrent to the carbon-based thin films, Vanadium Oxide thin films and a cost effective deposition process onto 3D designs were being studied by another student. Deposited Vanadium Oxide thin films have a much higher TCR value than their carbon-based counterparts. Using dip coating, high temperature coefficient of resistance values for these films at -2.8%/°K was achieved, making them very suitable for infrared thermal application.

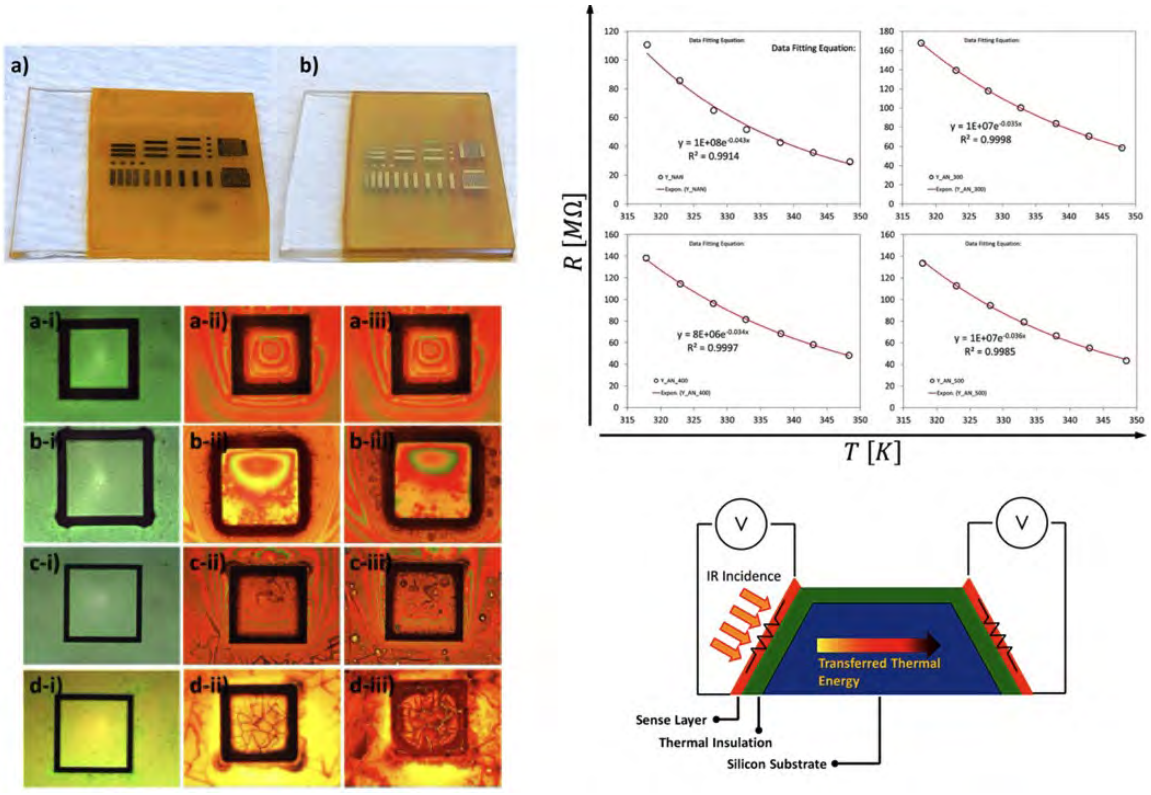

Figure 5-16. VOx thin film deposition, characterization, and deposition 2D and 3D substrates to create thermoresistive sensors [126]. VOx was first deposited on glass substrates, where performance validations indicate higher TCR values than carbon-based depositions. Bottom left: VOx thin films are deposited onto the facets of mesa pyramids microfabricated in silicon. A layer of oxide acts as an insulator separating the Si substrate from the deposited thermoresistive layer.

In his thesis [126], Dr. Vosoogh-Grayli provides a thorough review of the materials and deposition processes as well as further research into the deposition, suitability, and integration of the developed VOx thin films onto 3D structures. Due to its substantially higher TCR response, VOx was eventually chosen as the resistive materials to be deposited onto 3D structure, where the integration, deposition, and characterization was investigated and demonstrated in [126].

In conclusion, a low-cost spray deposition process was used to deposit MWCNT and graphene based thin films. The changes in resistance of graphene and MWCNT based films were noted as a thermal and electrical insulator polymer, polystyrene, was added. The changes in resistance of the films as the temperature is varied and when more layers are deposited were also noted. Experimental results show that the TCR values for some the films are comparable to those of some of the thermoresistive material used in thermal detection or hybrid solar applications. However, due to VOx's higher TCR response, the student deposited VOx thin films onto 3D structures to create 3D thermoresistive sensors.

6. Optimization and Reliability in The Integration of Silicon Photovoltaic Cell Interconnection Technologies

The Internet of Things (IoT) is an ecosystem that interconnects networks of physical devices through the Internet. Typically, the physical devices include sensing components, allowing devices to acquire physical inputs or changes in their environment, and relay the information within networks. Embedding more sensing devices within a network allows for a better understanding of the parameters, and correlations, within the environment. The intriguing aspect of IoT solutions is the ability for network nodes from one sector, i.e. sensors, devices, and systems, to monitor and control aspects of the sector as well as communicate and relay information to other systems, which could have been historically correlated but not actively connected. Depending on the interconnectivity of nodes and networks as well as the application, wireless sensor networks (WSN), containing a number of deployed nodes communicating wirelessly, reduce connectivity complexities as well as provide applications with the integration versatility needed for internetwork communications. An example of WSN would be the direct communication between sensors monitoring environmental quality within a city, such as sensors quantifying air quality, noise level, and traffic flow sensors providing traffic patterns for example. From such collected data, researchers at IMEC were able to simulate the redistribution of traffic within the City of Antwerp, Belgium, to potentially maintain noise levels and air quality within a specified range during certain periods of the day within parts of the city [127].

The backbone of IoT infrastructures in smart buildings, smart parking, and smart cities is the integration of a significant number of sensors, nodes, that are required for

monitor and control-associated systems actively collecting and communicating data. However, significant constraints arise from the deployment of standalone devices, i.e sensors, in excessive numbers, since a significant number of equally deployable power sources, such as batteries are required. Periodic maintenance requirements and limited power supply such as batteries are not effective for long term solutions due to operations' duty cycles and depreciating sensing reliability. In that regard, emerging technologies are based on rechargeable power sources in combination with energy harvesters and appropriate circuits to efficiently transfer the harvested energy and protect batteries from overcharging. In the case of solar power circuits, harvesters that rely on energy sources with known intermittencies and non-optimal weather conditions, also include low-power maximum power point trackers (MPPT) to efficiently transfer the harvested solar energy to rechargeable batteries, in addition to embedded DC-DC converters. On the other hand, indoor WSN applications, where sensors that are constantly deployed within a close proximity to ambient lighting elements may require less circuit sophistications. More recently, there has been more favourable transition approaches towards battery-less systems [128]–[134].

Concurrent with the continued demand for design optimization on solar systems to be even more easily integrated and compatible with sensors and communications technologies, there's a global increase in demand for a transition from non-renewable fossil energy sources towards clean and renewable energy sources. Photovoltaic (PV) solar panels provide an interesting technology with significant contributions to alternate methods of power generation as well as compatibility with emerging technologies. The low-cost and ever-increasing efficiency of c-Si PV modules play an important role in promoting and developing the technology for customizable and general commercial use.

In addition, emerging new technologies related to individual cells as well as associated cell interconnections within solar cell modules and encapsulation technology provide several optimizations to current designs and performances, thus, allowing for easier integration of the technology with battery-less systems and WSN applications.

Potential applications for the optical sensors mentioned, as well as the thin films and composites, include its ability for an easier integration into silicon PV solar or hybrid solar applications, particularly as stand-alone solar tracker devices for energy generation systems, embedded within a solar panel, or micro-fabricated as a part of the design within individual cells or outliner cells, on the sides or edges of the modules. The seamless integration of the optical sensor, as well as other sensing devices, into cells or panels, requires design and process optimization, on the pre-fabrication cell design level as well as cell, module, and panel patterning, layout, and fabrication levels that precede the integration of such sensors in several standalone, sensor-fusion, and IoT applications. Seamless integration of sensors implies that multiple connected sensors within systems operate without the sensors interfering with each other or negatively affecting the performance of the system they are connected to.

In order to overcome some of the challenges posed by current PV modules as well as to accommodate for the integration of newer embedded sensing technologies, IMEC has developed a novel interconnection technology to improve performance and reliability of solar cell modules while focusing on lowering materials and production costs. The multi-wire interconnection technology is based on a woven fabric, designed for the interconnection of bifacial cells, comprising of encapsulant ribbons and electrically conductive solder-coated wires. The weave enables reliable electrical connection without the need for precise alignment as well as implements sufficient encapsulation for the layup

phase of the PV module, thus, further facilitating processing and integration into other technologies.

The appeal in the technology is mainly due to the potential it holds for a significantly improved trade-off between optical (finger shading) and electrical (resistive transport) losses [135]–[144]. In addition to the performance enhancements on the cell and module levels, the technology allows for an improved trade-off between electrical and financial implications as the process considerably simplifies module layup and production, independent of optical considerations. Following proof-of-concepts made to demonstrate the technology, further optimization including the introduction of low temperature solders in order to reduce stress in the cells within modules [141]–[143], [145]. However, the lack of features to compensate for thermal expansion coefficient differences might create long-term reliability problems, therefore, further process development, performance, reliability, and cost optimization are ongoing.

In this chapter, the discussion deviates from sensor performance validations into design and process optimization that precede sensor integration, more specifically, the use of the novel multi-wire interconnections in bifacial silicon PV solar applications, which also provides the building block into the integration of solar power with sensing technologies and derived solutions. Following previous validations of the technology based on traditional stitching, or using transparent contact foils with integrated wires, process optimization was developed to start transitioning the process from the research level stage into an industrial process scaled for the commercial development of bifacial silicon PV solar modules and panels. Some of the optimization of novel multi-wire interconnections in bifacial silicon solar cell modules are discussed. Further building on previous work of group members, where they worked on several optimization including

material types and optimization in the module setup as well as interconnection stitching pattern analysis. My optimization are to study the overall impact on the modules with sufficient reliability to maintain cell performance and efficiency within the modules' lifespan. By integrating sensors and real-time monitoring within modules, different layout set-ups are evaluated and optimized. Electroluminescence imaging and current-voltage measurements at different stages of thermal cycling of the modules are used to validate the optimization. The characterization techniques provide an overview of modules' performance and response to illumination with respect to the modules' degradation over thermal cycles.

In addition, transient thermal measurements, inspired by the microelectronics industry, is used to study the thermal properties of polyolefin elastomer when aligned glass fibers are embedded, used as an encapsulant material in PV applications as well as substrate and packaging layer materials in flexible electronics applications. Studying the thermal properties allows for a better overview of Si cells and sensing expected behaviour within a module.

6.1. Interconnections

On a typical cell with busbars, the connection, generated current is transferred onto an adjacent cell through fingers connected to busbars, which are made of material containing silver (Ag). Recently, the busbar number in cells has increased from three to five, since adding more busbars reduces the effective finger length in which current travel distance to the nearest junction is decreased along with the series resistance (Rs) within the module [140], [146], [147].

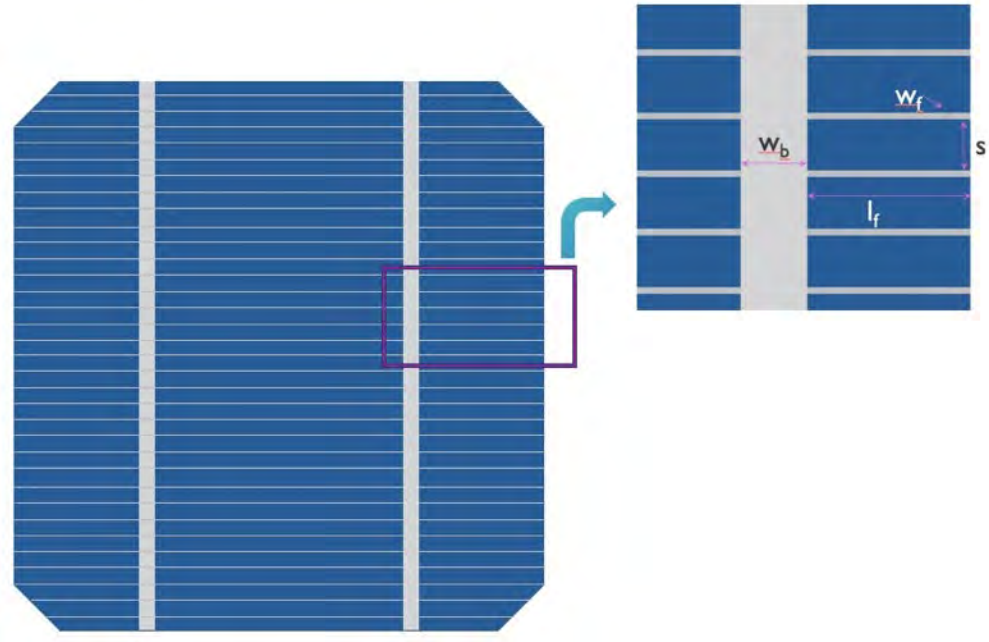

Figure 6-1. A standard two-busbar solar cell of width W_b, showing the spacing parameters S (spacing between fingers) and l_f (finger length to edge of cell) between connection of width W_f within a solar cell.

Braun et al. discuss the increased efficiency achieved compared to conventional three-busbar cells as well as reduced fabrication costs. Reduced power losses are mainly due to significant reduction in the distance current travels to the nearest interconnect junction in a multi-wire setup, compared to cells containing 3 busbars [140].

$$\text{power loss} = I^2 R = \frac{(x J_{mp} S_f)^2 \rho_f}{A_f} \qquad (6.1)$$

where x is the distance travelled by current to the nearest junction, J_{mp} is the current density at the maximum power point, S_f is the spacing between the fingers, ρ_f is the specific electrical resistance of the finger material, and A_f is the finger's cross-section area.

Busbar-less PV solar cells have been gaining interest, mainly due to reduced fabrication costs since less Ag is used and replaced with less expensive metals, such as nickel, as well as increased illumination exposure area due to reduced shading losses [140], [146]. The coverage fraction of typical (3-busbars) Si solar cells is in the range of 7% to 10%. Figure 6-2 shows a typical 15.6 cm mono-crystalline silicon PV solar cell with 3 bus bars. The busbars cover a significant portion of the cell.

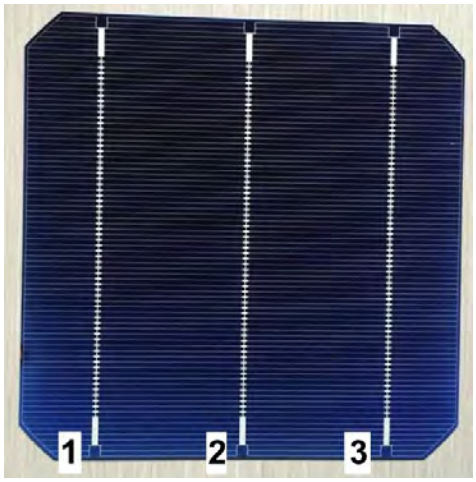

Figure 6-2. Image of a typical 15.6 cm mono-crystalline silicon solar cell with 3 bus bars. The busbars cover a significant portion of the cell.

The estimates do not take into account the internal reflection of incident light within the module, as close to 55%-60% light reflected from contacts, depending on the geometry of the contacts, gets reflected back from the glass-air interface onto the active cell area. The shading fractions due to the busbars are much more significant than the shading fractions of fingers in the cell. The shading fractions due to busbars and fingers in a unit cell, shown in figure 6-1, are S_{bus} and S_f respectively [148], [149] where

$$S_{\mathrm{bus}} = \frac{(1-t_b)w_b}{2\left(l_f+\frac{w_b}{2}\right)} \ , S_f = \frac{\left((1-t_f)w_f\left(l_f+\frac{w_b\, t_b}{2}\right)\right)}{(2 \ \cdot s \cdot \ (l_f+\frac{w_b}{2}))} \qquad (6.2)$$

and t_b and t_f represent the effective contact transparency factor in the busbar and finger respectively, w_b and w_f are the widths of the busbar and finger respectively, and l_f is the distance between the busbar and the edge of the cell in a unit cell.

On the other hand, in a multi-wire interconnection setup, traditional busbars are replaced by multiple thin round wires, 20 wires in our setup, where each wire has an approximate diameter of 190-200 µm. The solder coated (4-12µm) copper wires, used as interconnecting material to cells' fingers, are stitched through a polymer. Figure 6-3 shows an image of the busbarless cells used, where the added connections in the front side design of the cell takes into account lowering the possibilities of increased series resistance as the front side of cell interconnects with the backside of the adjacent cell. The back side is designed to reduce the series resistance on the edges of the cell due to interconnections with adjacent cells as well as eliminate alignment requirements with the foil embedded wires in the muti-wire setup. The interconnection setup provides an added benefit due to the wires' cylindrical geometry, where a significant portion of light reflected back from the wire gets reflected back again from the glass into the cell. Figure 6-4 shows a cross-sectional view of the combined multi-wire interconnection technology. Flat busbars have a maximum direct reflectance back against incident light sources due to its rectangular shape. In a wire, the cylindrical geometry allows for back reflectance into the cell. The reduced shading losses due the wires' geometry is an advantage of replacing busbars with wires. In addition, the wires' small surface area, relative to busbars, use up lower overall cell surface area [141], [148].

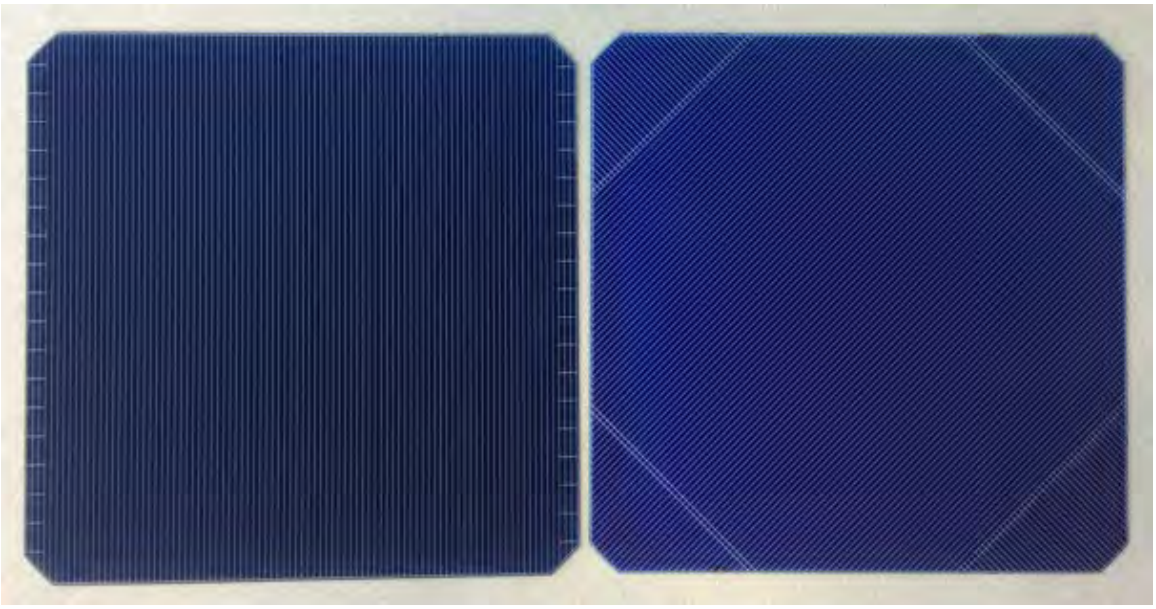

Figure 6-3. Bifacial busbarless c-Si solar cells used in our setup. The front side of the cell (left) shows no busbars covering any portion of the cell. The backside of the cell (Right) shows a finger pattern for optimized interconnection between cells of a module.

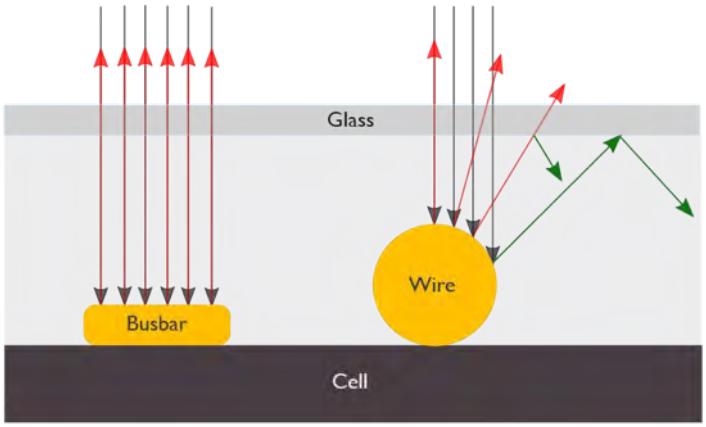

Figure 6-4 Cross-sectional view of the combined multi-wire interconnection technology. In busbars, the flat rectangular shape causes maximum direct reflectance back against incident light sources. In a wire, the cylindrical geometry allows for back reflectance into the cell. [Internal report, figure by Tom Borgers]

6.1.1. Multiwire Technology: Transition From Busbars to Wires

In multi-busbar designs, shading losses still account of a significant performance reduction, which can be unavoidable. The width of busbars decreased to somewhere between 1mm and 2mm in average commercial cells, in addition, there are added difficulties of having thinner interconnection ribbons. The aim to replace interconnection ribbons and busbars on cells with copper wires became more appealing, especially since Cu wire diameters can be significantly reduced, compared to ribbons and busbars. In addition, the geometry of the wire can increase the reflection percentage of incident light back into the cell, thus, further reducing shading loss.

The commercial development of implementing multi-wire an interconnect technology on busbar-less cells is based on three approaches. The first approach is introduced by SCHMID where wires are soldered directly onto the fingers. The step is followed by lamination, where a layer of polymer material conforms into encapsulant, as the high temperature and applied pressure onto the polymer encapsulate the cells and soldered wires. As in other standard processes, the lamination step of thermally and electrically insulating material is usually used to provide mechanical sturdiness for the module and protect the integrity of the cells in-field as well as prolonging the overall life of the module [150]. The second approach from Meyer Burger is referred to as Smart Wire Connection Technology (SWCT). In this approach, the wires are aligned and pressed onto a composite film during pre-laminations steps. In addition, the foils are pressed onto the cells to make ohmic contacts with the fingers as they're soldered directly onto the cell during a pre-lamination step. A lamination step then follows [139], [151]. There were several attempts at optimization including using thin wires (0.3 mm diameter), changing finger designs to dotted lines and plating Sn on fingers' surface to achieve better contacts

with wires, as well as other fingers designs and using other encapsulant foils to facilitate connections with back electrodes.

However, the added costs associated with the multiple steps, required during the pre-lamination and lamination steps, considerably add to the overall production cost and contribute to the setbacks of commercializing the associated technology. Other contributing issues include soldering reliability at the finger contacts as well as out-gassing of metal oxides during soldering which may lead to reactions with some polymers used for encapsulation, namely EVA, as well as other associated side reactions increasing the probabilities of fast encapsulant degradation and delamination.

Other challenges include having a composite layer made of material that will not react with the encapsulation layer during the lamination process, yet have a similar refractive index as the encapsulation layer. In addition, the overall thickness of the encapsulation layer should not change much in order to not affect light transmittance in the layer or compromise the mechanical robustness of the module [147], [152]–[155].

In an attempt to address the major challenges with the other approaches, a third approach is developed by IMEC. The multi-wire interconnection setup consists of approximately 20 solder coated wires where stitched into the thermally and electrically insulating polymer foil, thermoplastic polyolefin (TPO). The wires, 0.195-0.200mm thick copper wires coated with 57Bi-42Sn-1Ag, corresponding to alloy concentrations of 57% bismuth, 42% tin, and 1% silver, specialized for low temperature soldering, with a melting point at 139°, are stitched into the foil. In addition, the wires, which do not require to be aligned and pressed onto an additional layer of composite material or other pre-lamination steps, are soldered onto to the fingers to act as a multi-busbar setup during the lamination

process. Low melting temperature soldering decreases the chances of cells breaking during the soldering process due to decreased thermo-mechanical stresses on contacts and the cells as well as enhance solder contact reliability. Cost effective low temperature soldering also allows for the use of thinner solar cells. [145], [156], [157]. In addition, as discussed in a later section, the usage of TPO is ideal since the polymer foil does not react with metal oxides. On the other hand, the lamination step itself serves as both the soldering step, where the solder material around the wires melts to form solder joints with the cells' metallization fingers, and polymer conformation into encapsulant, as the high temperature and applied pressure as the polymer encapsulate the cells and soldered wires [158]. The one-step process also eliminates the need for precise alignment of the weave onto the cell, an added advantage over the other processes which require multiple alignment steps within their layup setups. In addition, the process does not require the additional pre-lamination steps as the other mentioned processes nor the usage of additional materials [139], [150], [151], [158].

In further attempts to decrease costs on the already cost-effective process, optimization of the lamination parameters during the lamination step as discussed in later sections. Furthermore, the performance of the modules is evaluated before and after thermal cycling to confirm the reliability of the process. The process is currently being developed for commercial production of modules using the technology.

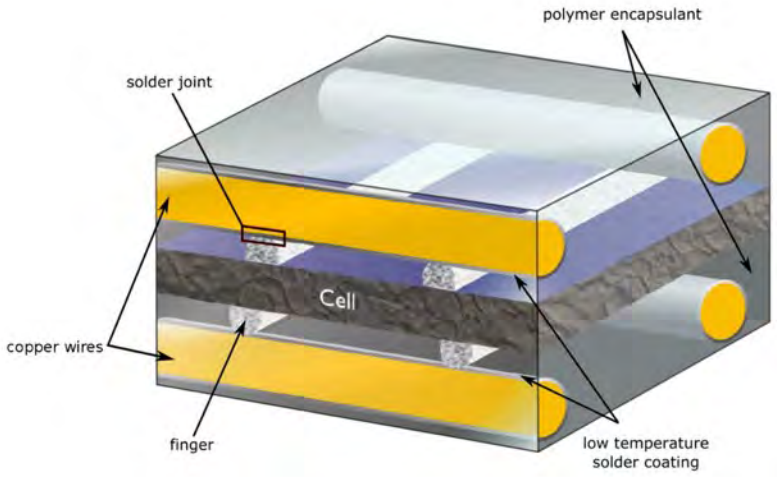

Figure 6-5. Cross-sectional view of the multi-wire interconnection technology integrated within a module containing a bifacial cell. The wired interconnections [containing a layer of solder] are embedded within an encapsulant. During lamination, the layer of solder melts to interconnect with the fingers of the cell, as the encapsulant layer engulfs the module component to ensure an added direct electrical contact between the cells. [Internal report, figure by Tom Borgers]

6.1.2. From Lamination Process of Bifacial Si Solar Cells

There are typically two module structures for PV solar cells. Most current mono- or polycrystalline mono-facial Si based PV module layouts are glass-backsheet (GBS), where a thin layer of glass, typically 3.2–4mm thick, is placed at the front of the module and a polymer-based insulating backsheet. On the other hand, glass-glass modules, where glass is used on both sides on the module, are less popular for mono-facial cells.

Bifacial crystalline silicon (c-Si) PV solar cells have received considerable attention in recent years as they are able to absorb irradiance from both sides of the cell. Thus, their potential to increase the overall efficiency and energy yield within modules has been economically and commercially appealing.

There are two module structures for bifacial solar cells, the glass/glass and glass/backsheet modules. Each of the module structures offer advantages and

disadvantages, wherein a glass/glass module, absorption due to the ground-reflections diffuse irradiance onto the rear side of the glass/glass module, thus increasing the energy yield, compared to monofacial cells. In addition, there were reports of reduction in electrical losses due to parasitic light absorption in the metal layer and high surface recombination at the metal–silicon interface of an Al back surface field [159]–[162].

On the other hand, backscattering and the scattering in the cell-gap region due to the backsheet's spectral reflectiveness as well as the reflection at the glass–air interface in glass/backsheet module structures can provide an increase in the current and power of the module as compared with the glass/glass structure [163]–[165]. However, in outdoor use, the additional energy yield provided by glass/glass modules provide a more cost-effective module structure for bifacial cells modules than the glass/backsheet module, despite the glass/backsheet providing a 2–3% higher power compared with a glass/glass module, where EVA is used as an encapsulant [160], [161], [166], [167].

6.1.3. Polymers and Encapsulation Material

In the module layout, the solar cells are typically sandwiched in between two layers of thermally and electrically insulating polymer foil. During the lamination process, the module is compressed under high temperature to melt the polymer and encapsulate the cells within the module. The encapsulation of cells provides the module with mechanical sturdiness and prolongs the overall module's life as well as protects the integrity of the cells in-field. The most popular encapsulant for a PV module design is the copolymer ethylene vinyl acetate (EVA). The popularity of the material is due to its low cost and processing requirements while providing good optical transmittance and electric insulation as well as its low water absorption [168]–[170].

However, EVA has its share of disadvantages. Despite its low cost, EVA requires UV–blocking agents or additional chemistry where UV-sensitive backsheets are used, thus increasing processing costs. Moreover, over time, the viscoelasticity creeping-based degradation of the copolymer material leads to delamination at the encapsulant- cell interface as well as the edges of the module. Moisture penetration into the module, primarily in hot and humid climates, as well as water dissipation into the module in rainy and snowy weather, create areas of corrosion in the module. In addition, degradation related to prolonged exposure to UV radiation causes EVA to decompose and produce acetic acid, thus, further accelerating the setup with corrosion. Corrosion affects the resistance in solder joints, cell metallization, and interconnects, due to deterioration in the metal layers and connections. Corrosion and acetic acid formations reduce the mechanical performance of the polymer as well as further coloration changes in EVA. Changes in encapsulation layer coloration also affect the intensity of incoming light. Thus, delamination and discoloration within the module reduce the overall power generation and output of the module due to the considerable power loss [138], [171]–[177]. Furthermore, modules with EVA encapsulation suffer potential induced degradation caused by active cells' negative potential. At high voltages, positively charged ions from glass, namely sodium ions, dissipate to the cell through the encapsulant, thus, reducing the power output of the cells [177]–[179].

In order to address the disadvantages of EVA, Polyolefin (TPO), a thermally and electrically insulating polymer, is used in the setup. The translucent TPO copolymer, consisting of a main thermoplastic polymer crosslinked with an elastomer, acts as an encapsulating material for cells within a solar module and offers some advantages over EVA.

TPO's transparency allows for it to be used without additional modifications or UV-blocking agents. TPO has thermo-mechanical and oxidation resistance, which tend to make its processability much less complex, since no free radicals or reaction by-products are produced during the lamination process, thus, reducing the possibility of corrosion in cell metallization and at solder joints. These features also make the polymer more resilient to potential induced degradation, compared to EVA. Its very low moisture vapour transmission rate reduces material storing costs before lamination, as well as contributes to the overall module integrity [170], [178], [180]–[184]. The viscoelasticity of the encapsulant material, referring to the combination of elastic and viscous properties of the polymer, plays an important role in determining which encapsulant is used in modules as well as associated lamination parameters used to prepare the module. The TPO-A (TPO of type A, from an undisclosed supplier) that we are mainly using in our setup is a TPO thermoplastic elastomer of relatively low viscosity, and its transition between solid and rubber-like, above its melting point, is rapid and reversible. In some reliability testing, TPO-A is compared with EVA, a thermoset cross-linking encapsulant which irreversibly exhibits elastic-like material behavior once its melting point has been reached [184]–[186]. In addition, TPO-A is compared with TPO-B, which is a thermoset, cross-linking, encapsulant with high viscosity, relative to TPO-A, in order to note reliability and module behavior patterns with different TPO materials.

Group members at IMEC are to perform quantitative viscoelastic analyses for several parameters for EVA, TPO-A, and TPO-B including shear and elastic moduli as well as viscosity variations as a function of temperature, applied pressure, and rotational frequency using dynamic mechanical analysis (DMA). Such parameters provide a better

insight into encapsulant behavior during the lamination process as well as post-lamination, thus, facilitating suiting encapsulants for module preparations and applications.

For example, in a GG module, encapsulant flow in between cells is strongly related to its viscous properties during the lamination process. Encapsulants with a high viscosity require more time to flow, thus, process lamination time is drastically increased to allow the encapsulant to fill in the gaps to avoid delamination issues. On the other hand, encapsulants with low viscosity and low elastic behaviour may cause excessive compression of the edges of the glasses, compared to the center of the modules, which may lead to breakages during thermal cycling [185], [186].

6.1.4. Electrical Performance

The assessment of thermal functionality within solar PV systems, as well as systems that depend on variations in operation and ambient temperatures such as in microelectronics, photonics, and solar systems industries, is essential in determining the systems' optimal design as well as expected performance and degradation patterns. The performance of solar cells decreases with increasing temperature of the cell, as thermally excited electrons begin to dominate electrical properties of the semiconductor [135]. The ideal solar cell behaves through the following equation:

$$\mathrm{I} = \mathrm{I_L} - \mathrm{I_0}\,[\mathrm{e}^{\left(\left(\frac{\mathrm{qV}}{\mathrm{nkT}}\right)\right)-1}], \qquad (6.3)$$

where, I, is the output current, I_L, is the current generated due to light, q, is the elementary charge of 1.6 x 10^{-19} Coulombs, V, is the measured cell voltage, n, is the diode factor, ideally equal to 1, k, is the Boltzmann constant of 1.38 x 10^{-23} J/K. T, is the cell temperature measured in Kelvin. I_0, is the saturation current of the diode and is denoted by [187]

$$I_0 = \mathrm{I}_{0,\mathrm{ref}} \left[\frac{\mathrm{T}}{\mathrm{T}_{\mathrm{ref}}}\right]^3 \exp\left(\frac{\mathrm{E}_{\mathrm{g,ref}}}{\mathrm{kT}_{\mathrm{ref}}} - \frac{\mathrm{E}_{\mathrm{g}}}{\mathrm{kT}}\right) \qquad (6.4)$$

where, Tref and Eg,ref refer to the temperature and bandgap energy of the semiconductor material at Standard Test Conditions, respectively.

Isc is the current through the solar cell when the voltage across the cell is zero. *Voc* is found by setting the net current equal to zero in the solar cell equation.

$$V_{\mathrm{oc}} = \frac{\mathrm{nkT}}{\mathrm{q}} \ln\left(\frac{\mathrm{I}_{\mathrm{L}}}{\mathrm{I}_0} + 1\right) \qquad (6.5)$$

where *Voc*, is the solar cell's open circuit voltage, Isc, and *FF* (fill factor) determine the maximum power from a solar cell. *FF* is defined as the ratio of the maximum power from the solar cell, denoted by the product of the maximum possible voltage and current outputs, VMP and IMP respectively,

$$\mathrm{FF} = \frac{\mathrm{V}_{\mathrm{MP}}\mathrm{I}_{\mathrm{MP}}}{\mathrm{V}_{\mathrm{oc}}\mathrm{I}_{\mathrm{sc}}} \qquad (6.6)$$

The solar cell's open circuit voltage (Voc) and fill factor (FF) decrease substantially with temperature, while short circuit current (Isc) increases slightly, thus reducing the overall performance of the cell [135].

6.2. Lamination process and optimization: Multiwire interconnections with bifacial cells

PV modules are typically laminated using a vacuum- membrane laminator with a single heating plate at the bottom of the laminator. The process mainly involves a vacuum step, where air and gases formed during the heat-up process, get released. The pressing step then follows, where the flexible membrane is pressed onto the module, under high temperature, to ensure that the layers in the layout adhere to each other. The step is then followed by the module cooling down as the liquefied polymer starts to solidify so as the integrity of the module stays intact [188].

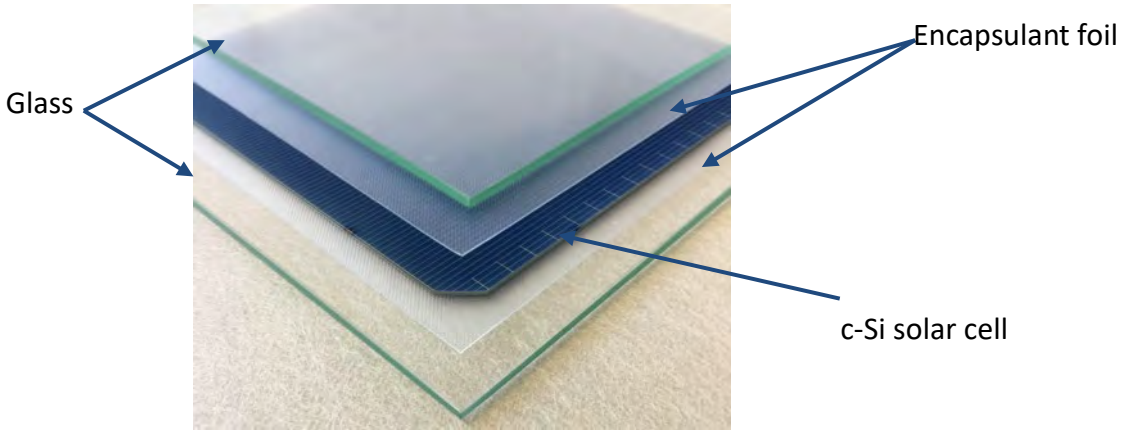

Figure 6-6. Module layout for the setup before lamination. PV solar cells are sandwiched in between two encapsulation foils and two layers of glass.

In SWCT setups and when bifacial cells are used, it is more ideal to provide pressure from both ends of the module, as well as more uniform heat transfer within the module, for the interconnects to maintain a good contact with the cells as the encapsulant layers liquefies. Thus, newer types of laminators evolved by emphasizing the features of older types of laminators, where both upper and lower plates of laminators are also used

as heating plates as well as a double-sided vacuum membrane where temperature and pressure can be applied from either side of the laminator, uniform heating and concurrent symmetrical pressure from both sides of the laminator, or with varying temperatures and pressures from either plate of the laminator for customized modules. Furthermore, in older laminators, where the sample is usually heated using the bottom plate and the upper plate is used to apply pressure on the module, the applied pressure distribution is not as uniform across the sample, where most of the pressure would be applied to the center of the sample, but minimal pressure applied at the edges. Thus, the compression at the edges of modules is not as effective as when pressure is applied from both sides of the module, thus, providing a better pressure distribution across the sample, as in the newer type of laminators. In addition, encapsulants with additives that cause out-gassings of volatile organic compounds (VOCs) during lamination are not typically suited for PV modules as they lead to bubble formations in the module. While, typically, the vacuum step during the lamination process is set up to remove air and VOCs, additives in encapsulants also usually include impurities that cause unwanted side-reactions leading to further formations of VOCs. In SWCT setups, out-gassing of metal oxides may also contribute to bubble formations or other defects in the module, as discussed earlier. However, more uniform heating, under pressure, enhances chemical reactions and associated side-reactions in encapsulant layers with additives, thus causing formations and entrapment of VOCs within the module and increasing the probability of bubble formation within the module [185], [188]–[192].

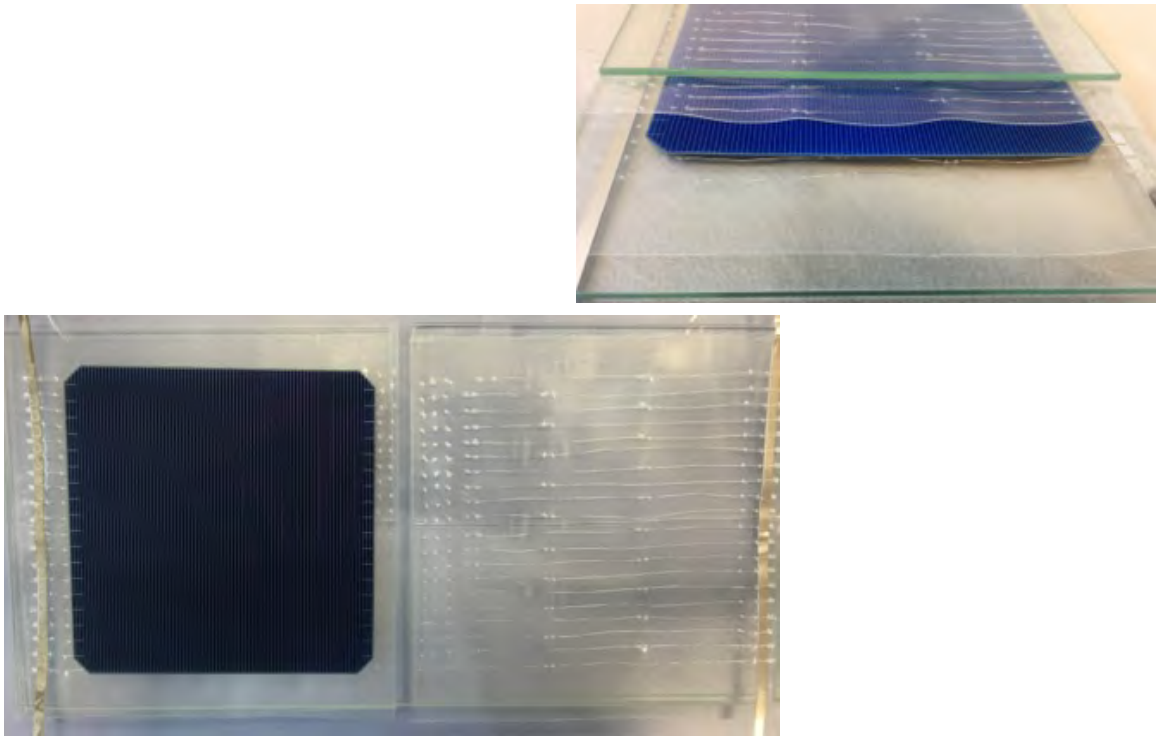

Figure 6-7. A one-cell module layout shows the interconnection wires stitched pattern into the encapsulant foil layers. When the module is laminated, the interconnections on both side sides of the bifacial cell are soldered onto the cell, according to the stitch pattern.

In our SWCT setup, TPO-A is used, as it is better suited to be used for the glass-glass setup, mainly due to the lack of additives required as well as other advantages, over EVA for example, as previously mentioned. In order to avoid some of the issued mentioned, a laminator with symmetrical two heating plates was used for the lamination of PV modules with a 2mm-GG lay-up and SWCT, Figure 6-7.

6.2.1. Temperature

The TPO-A foil used in our setup is a research industrial-level encapsulant foil, provided to us by industrial partners. However, due to non-disclosure agreements among participating research institutions, the content details and properties of which were not

provided, including chemical structure or backbone of the TPO foil nor with the recipe used to manufacture the foil.

Van Dyck at al. studied the rheological properties of three types of TPO, including the foil used in our setup, to understand some of the properties of the non-cross linking, thermoplastic foil, including relative viscosity [145]. As mentioned earlier, other group members are measuring elastic and viscosity related properties of the foil, including sheer stress. However, the ultimate goal is to use the TPO-A foil for PV solar applications, and the optimization made to the lamination processes are to integrate all steps of the solar panel manufacturing step into one step. Aside from the already cost effective utilization of materials, the process optimization further reduce production costs, an added advantage over other production process utilized by other researchers, as mentioned earlier.

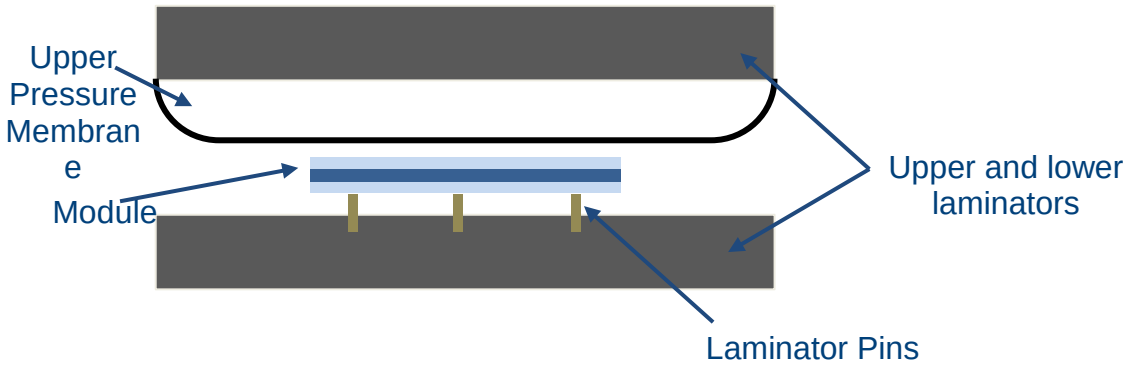

Figure. 6-8 Schematic showing a side view of the module within the laminator. Pins are used to lift the module, during the press-step. The pins lift the module to ensure pressure and temperature are uniformly distributed across the module.

The three basic parameters in the lamination process, which are temperature, pressure, and lamination time, are used as the basis for process optimization. Initially, temperature variations are monitored during the lamination process, given the different materials used in the setup, including glass, encapsulant, and copper wires with solder coatings, with each having material having their own coefficient of thermal expansion

(CTE). CTE denotes objects' size changes with changes in temperature. In other words, CTE is the fractional change in size per degree change in temperature at a constant pressure. Thus, temperature variations at constant pressure were first studied to provide more insight into the adhesion patterns at the encapsulant/cell interface as well as solder patterns at the wires/fingers interfaces, as temperature targets are set to temperature ranges around and above the melting point range of the SnBiAg and SnIn solder coatings on coper wires inside the modules.

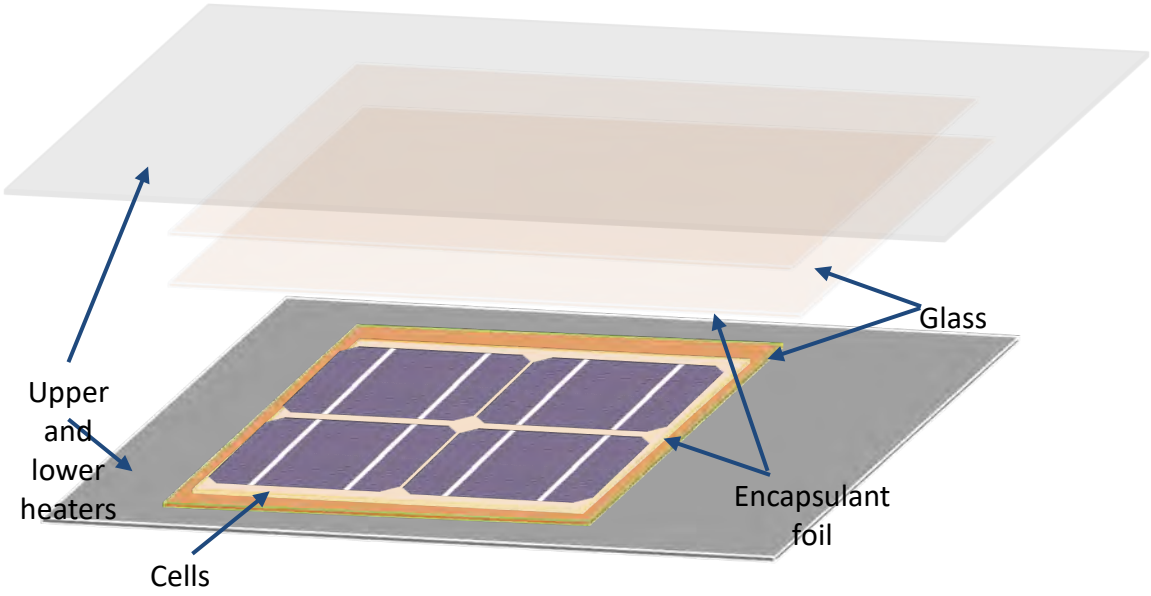

Figure. 6-9. Schematic of the module layout within the lamination system. Module cells are encapsulated within polymer foils and glass. Temperature and pressure variations are studied to ensure modular/mechanical strength post-lamination.

The reliability of process optimization is assessed and validated by utilizing several analysis methods in order to verify modules' performances, especially in the long term.

6.2.2. Electroluminescence Imaging Measurements

Electroluminescence (EL) imaging is a relatively quick measurement technique used to provide an outlook “map” of the electrical connection conditions and layout between the cell and interconnection wires in the post-lamination steps of modules. In an EL-imaging setup, the solar cell, or module, is connected to a power source to provide the cell with a constant forward current flow, thus, causing the Si cell to act as a light emitting diode (LED). Emitted photons at different wavelengths are then captured by the setup camera, providing insight into the electrical connection between the interconnecting wires and the cells. Figure 6-10 shows the experimental setup for EL imaging. The setup is set in a dark room where cells are connected to a power source, 8A current at 1.2V in our experiments, and a modified DSLR camera with an extracted IR lens is used to capture images after an exposure of 10 seconds. As in figure 6.11, the darker regions in the image indicate the absence of current flow in the region due to bad finger contacts, broken contacts, or other electrical shunts. EL imaging can also indicate damaged areas, such as micro cracks in cells or electrically separated cell areas in modules [193].

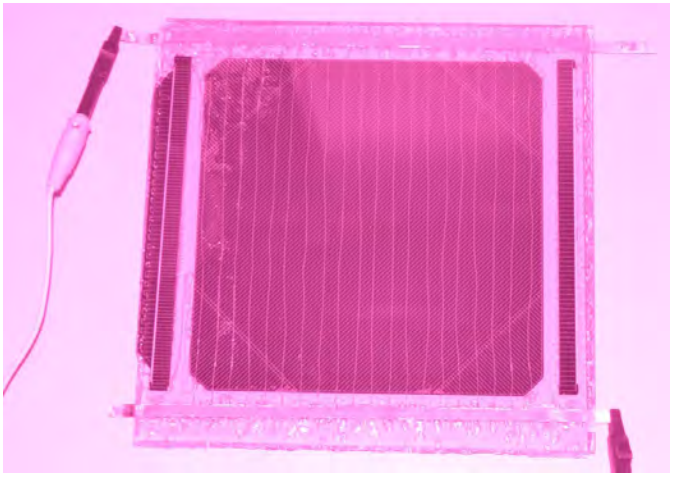

Figure 6-10, EL imaging setup: a solar cell is connected to a power source, while a camera (without an IR filter) is used to visualize cell and interconnection defects.

EL-imaging coupled with Current-Voltage (IV) characterization of modules provides a more comprehensive overview on current and expected electrical properties of the whole cell as well as the performance of modules in the long run, since these characterizations are not destructive to cells and modules in general. To provide sufficient information on the electrical performance of cells, IV measurements are taken in light and dark settings, as well as Isc and Voc. Other information such as contact resistance provides comparative information about the overall condition of the interconnect-finger contacts. The measurement conditions are set to standard conditions at 25 °C temperature. Light intensity exposure is set to 1 kW/m^2 , corresponding to the intensity of one sun, at 1.5 spectrum (AM 1.5), using a Xenon light source with filters, corresponding to the electromagnetic spectrum of sunlight reaching earth's surface.

In addition, thermal cycling is used to validate performances of the module after thermomechanical stresses are induced to the modules. IEC 61215 qualification standards correspond to accelerated stress tests to test c-Si modules' design, materials, and process reliability measurements against premature field failures. Modules are placed in a controlled environmental chamber where temperature is cycled through an extreme temperature range, from -40 °C to 85 °C, over the course of 200 cycles, or 1000 hours, since differences in CTEs due to different module materials creates stresses as the temperature is changed. The fast temperature variation provide an overview of long term thermo-mechanical reliability of the system for several climatic operations of modules against failures, including the accelerated degradation of solder joint interconnections and electrical failures as well as breakage and cracks in cells and modules. Fig. 6.11 shows an example of cracks and loose connections in the cell. Figure 6.13 shows degradation on the edges of the module.

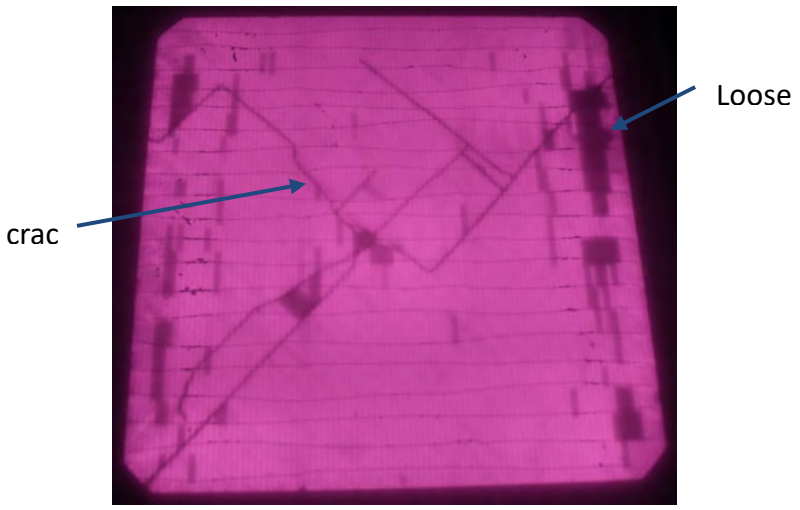

Figure 6-11. EL image of a cracked cell. The darker regions on the edges indicate the absence of current flow, due to loose connections. Crack patterns are also visible in the cell.

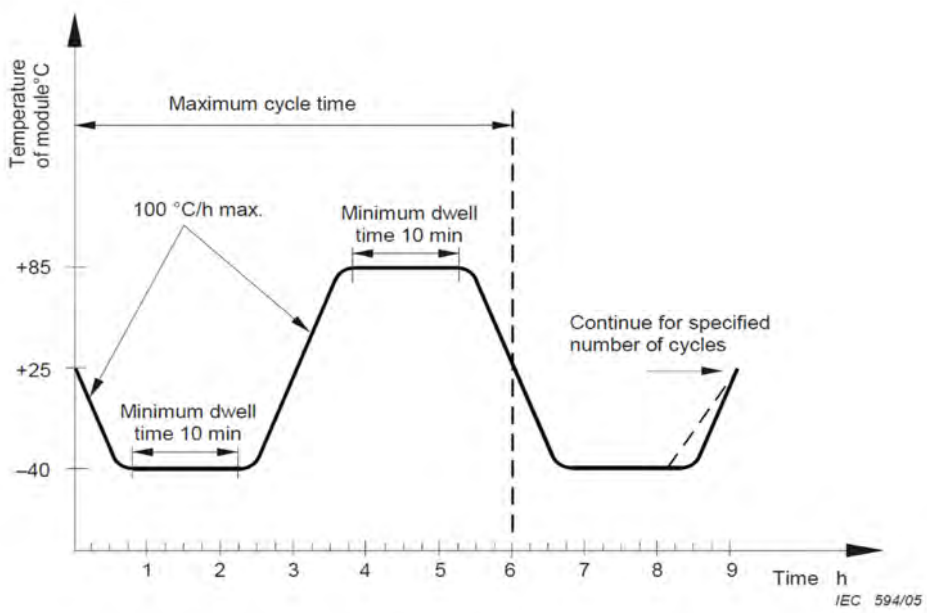

Figure 6-12. Accelerated thermal cycle of modules between -45 °C and 85 °C for performance reliability. Modules undergo several thermal cycles to study the modular and mechanical characteristics of the module under extreme weather conditions. [194].

6.2.3. Wires and Soldering

Bi57-Sn42-Ag1 has a melting temperature of 139 °C, as mentioned earlier. With significant differences in the CTE for the layout materials including borosilicate glass, c-Si, and TPO at 4.0 µm/m°C and 2.5µm/m°C for glass and Si respectively, and a range of 65-200 µm/m°C for TPO, depending of the foil material used. The melting range of solder is between 139-144 °C, taking into account non-uniformities in the solder coating across the copper wire, and an approximate melting range of TPO between 125 °C and 135°C. Thus, the lamination temperature of 155-160 °C would be was estimated to be ideal for lamination [145], [195], [196].

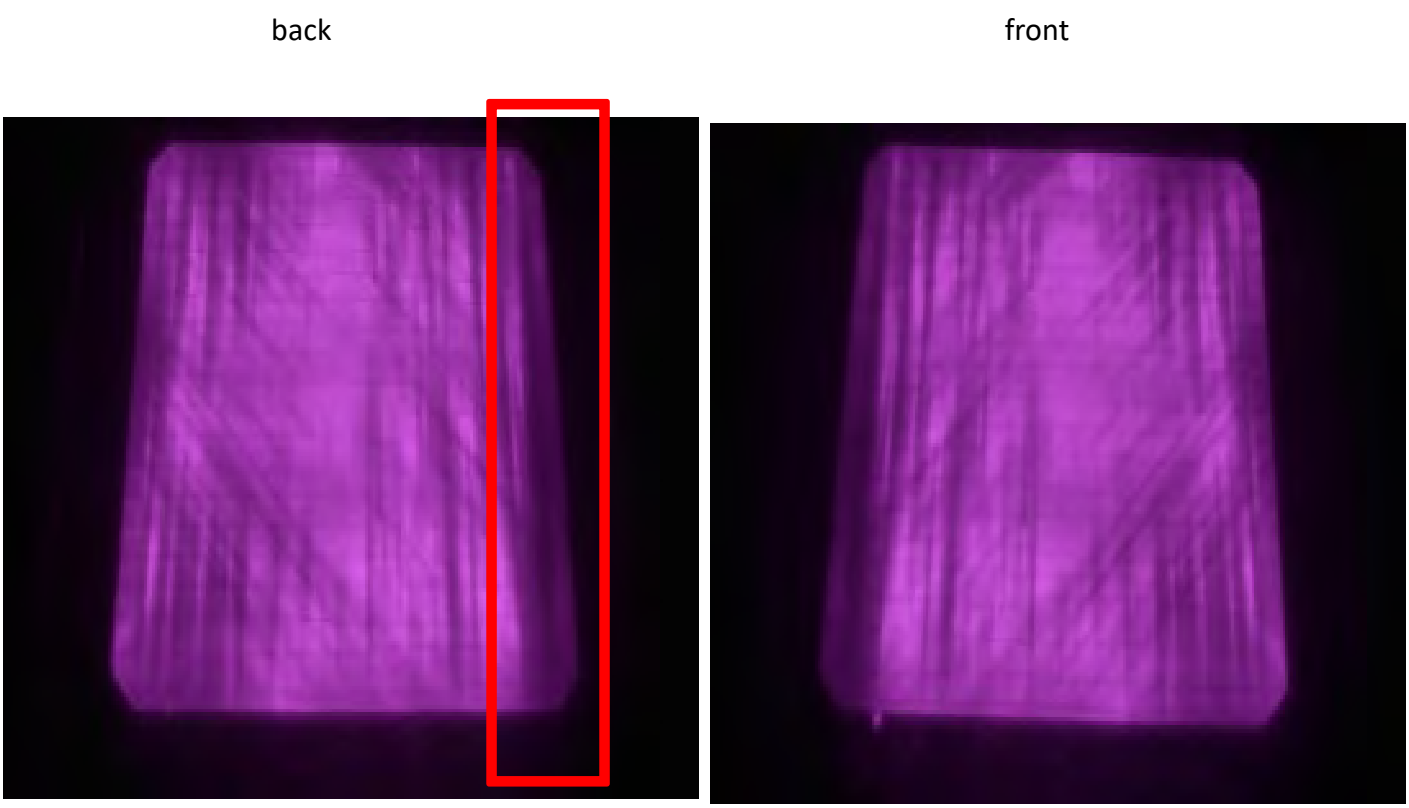

Figure 6-13. EL images of a bifacial solar cell in a module, using TPO-A as encapsulant. Darker regions shows no contact connection between wires and interconnects. Lamination process conditions are set to 155 °C, pressure at 700 mbars, and lamination time at 20 mins.

In general, the thermomechanical stresses within PV modules are induced by mechanical loads such as snow, or thermally due to environmental factors or to the components within the modules, such as heat generated by the cells and interconnections as well as the stresses induced due to the lamination process and thermal cycling. The stresses are due to the mismatch in CTE of the different materials within the module, where the time-temperature superposition of the phenomenological viscoelasticity principle holds true for most polymeric materials [197]. Since the young's modulus of the viscoelastic materials is a function of time and temperature, material behaviour, including creep and relaxation times, vary with temperatures variations. Thus, modules with soft encapsulant materials at room temperature become stiff at low temperatures for example, such as in the case of EVA where the encapsulant becomes stiff at low temperatures, and can no longer compensate high stresses in the module [198]–[200].

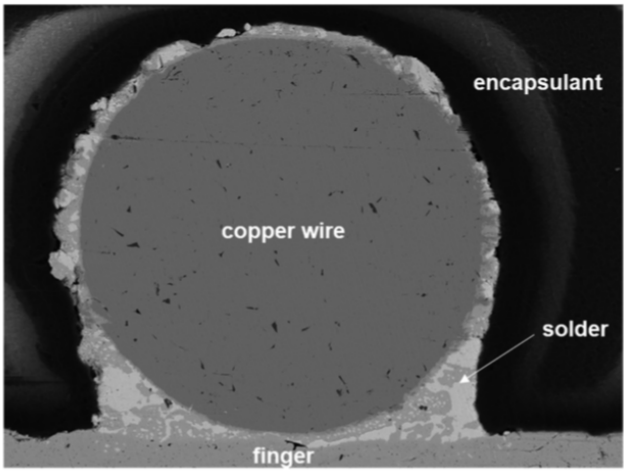

Figure 6-14. SEM image showing cross-sectional view of an ideal solder joint between a copper wire with SnBiAg solder coating and a finger on the cell. Solder from the wires binds to the solder of the finger [within the cell] as high temperatures melt the solder [145].

Initial results for the setup indicate that there are issues with having uniform electrical contacts across the cells, especially across the edges. The main contributor is loosened connections due to the viscoelastic nature of the enacapsulant, especially in the

thermoplastic polymer material. Despite the adhesive forces between the encapsulant and the glass, the relatively high stress relaxation rate of the polymers embedding the wires have most likely induced a high enough force to move and detach the soldered wires from fingers either during the lamination process or during thermal cycling. Thus, loosening the contact between fingers and wires. Another possibility is that the temperature within the module is not high enough to melt the solder on wires, thus the electrical contact between the wires and fingers is week to begin with, before starting to address internal forces. Figures 6-14 and 6-15 show a distribution of the solder accumulation pattern with respect to temperature and pressure ranges.

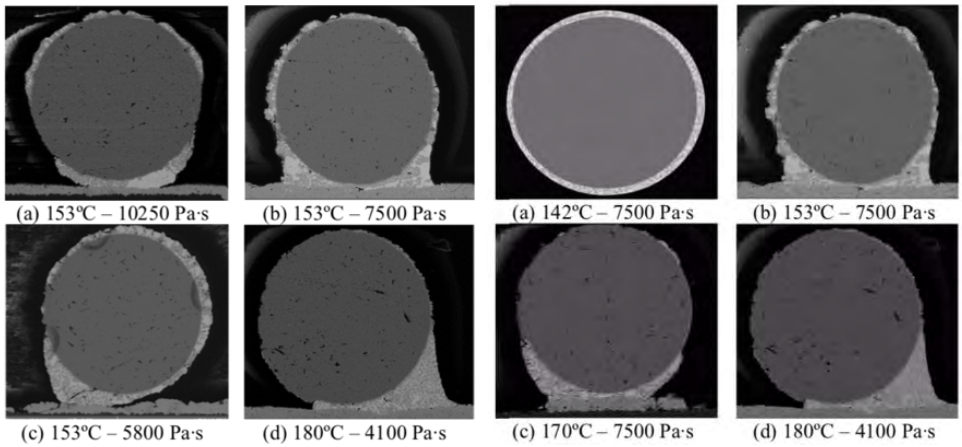

Figure 6-15. SEM image showing cross-sectional view of a solder joints between wires with a solder coating and a finger on cell. Lamination temperature and polymer viscosity affect solder joint formations within the cell. The temperatures displayed are the set temperatures of the laminator, not the temperatures within modules. High temperatures cause the majority of the solder to shift towards the finger, while a low pressure helps redistribute the solder onto the bottom layer of the interconnect. A balance between temperature and pressure ensures a maximum solder contact and distribution between the fingers on the cell and the contacts. [145].

Since the polymer is viscoelastic, creep deformation are temperature and applied stress dependant, as temperature increases cause a higher macromolecular mobility within the polymer matrix, leading to higher creep deformation. Thermoplastic polymers exhibit strong creep effects under constant loads due to the entangled molecular structure

and viscoelastic properties, even at room temperature, where strain accumulates as a result of long-term stress, causing time dependant deformation behaviours. Furthermore, compared to crosslinking polymers, such as EVA, internal molecular slippage within thermoplastic polymer matrices increases, especially above the glass transition temperature, further increasing deformations. The complexity of the creep model within a system is related to the viscoelastic behaviours of the different materials within the system, including the linear or non-linear viscoelastic dependency on time and temperature. The basic viscoelastic relationship can be described as [201]–[204].

$$E_c(t) = \frac{\sigma_0}{\varepsilon(t)} \qquad (6.7)$$

where E_c is the creep modulus, σ_0 and ε are the flexural tension and the extension within the polymer as a function of time t.

Following initial results at 155°C, another sample was laminated at 160°C while reducing the lamination time. The main purpose is to ensure that the temperature inside the module reaches the solder melting range as well as reduce the creep behaviour and subsequent deformations in the foil by reducing the time at which the polymer foil is pressed during the pressing step of the lamination. Figure 6-16 shows the similar lamination results at 155°C, in which connections also seem to be weaker on the edges of cell, however, slightly better uniformity, pressure distribution, and connections between wires and fingers at the center of the module than at edges, compared to 155°C at longer press-time.

The samples were placed in the thermal chamber, ESPEC Environmental Chamber, where temperature underwent several -40°C to 85°C thermal cycles, while humidity was not varied. Figures 6-17 and 6-18 show the degradation present after 25 cycles, and figure 6-19 shows the degradation in fill factor among the samples.

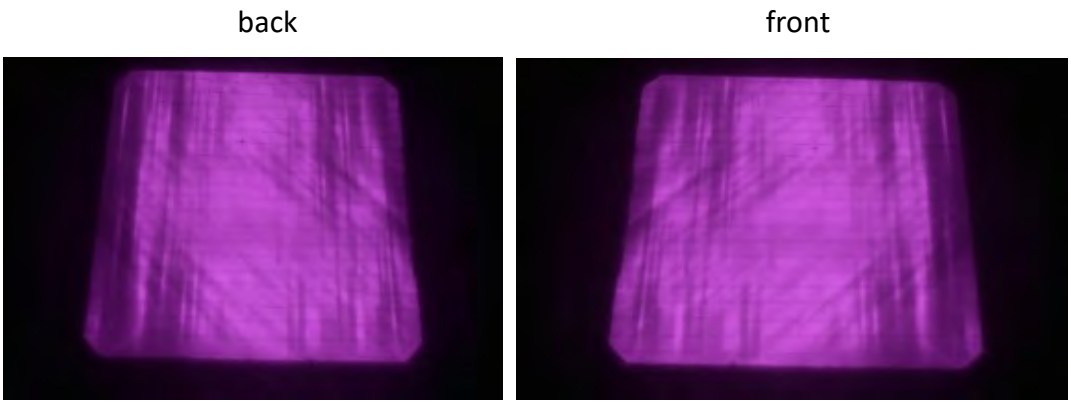

Figure 6-16. EL images of a bifacial solar laminated module [160°C, pressure: 700 mbars, and lamination time at 15mins]. The module shows that cell finger didn't bind with interconnections, especially along the side.

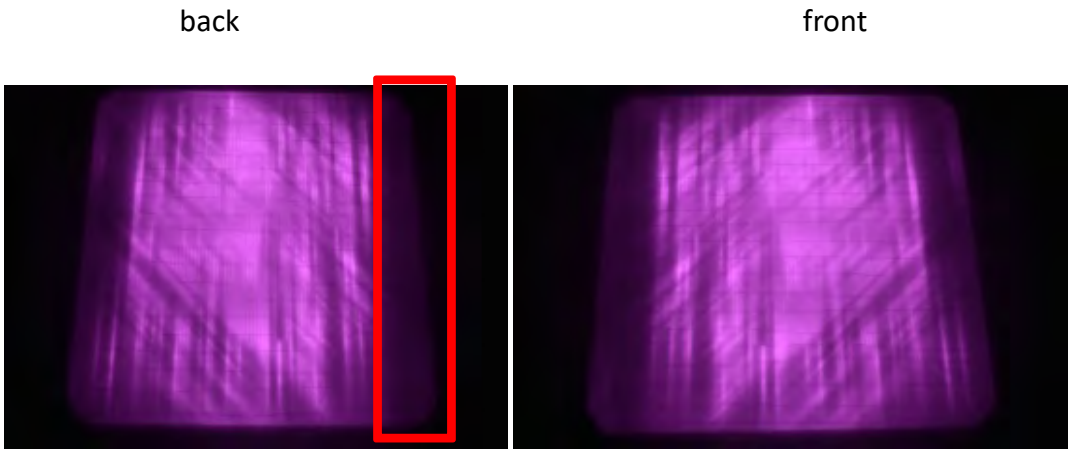

Figure 6-17. EL images of a bifacial solar cell in a module at 155°C after 25 thermal cycles. Suspected creeping effect results are more prevalent on the edges, as the polymer is slowly degrading due to the extreme temperature fluctuations of thermal cylcing.

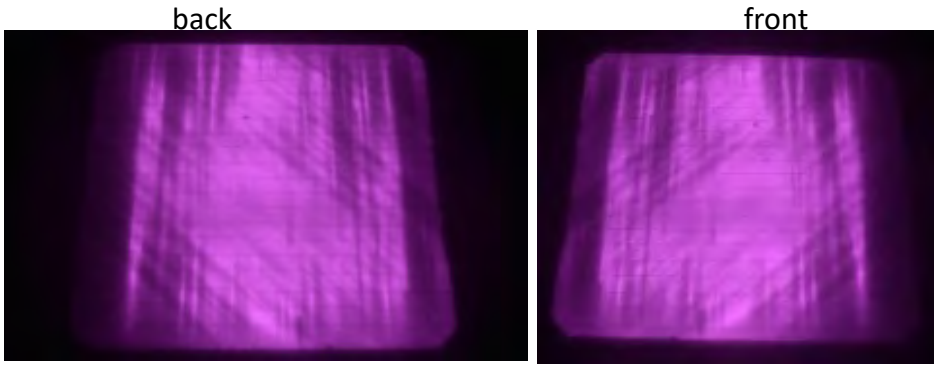

Figure 6-18. EL images of a bifacial solar cell in a module at 160°C after 25 thermal cycles. Degradation at the edge and corners of the cell indicate that the interconnection and finger binding no longer holds, thus, reducing cell performance.

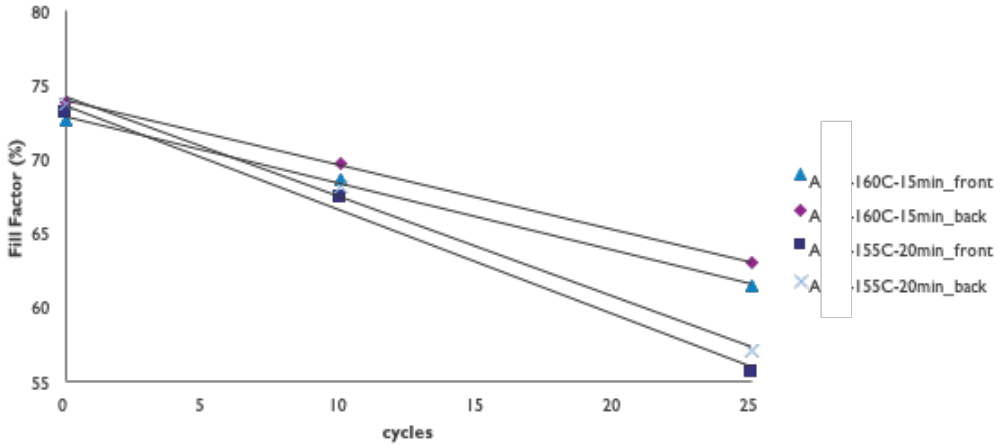

Figure 6-19. Plot of FF as a function of the number of cycles for modules prepared at 155°C and 165°C. The Cell performance is studied over thermal cycles. Significant degradation is shown, as expected, as internal connections within the module are not holding.

6.2.3.1. SnIn Wires

Following the previous results, BiSnAg wires were used instead of SnIn (tin indium) wires. BiSnAg have a dimeter of 190-200 mm diameter and a solder layer of 12 um thickness, whereas SnIn have a dimeter of 200 mm and a solder layer thickness of 4um. As expected, initial results, i.e. before thermal cycling, indicate that wires with a larger diameter and thicker solder layer have better electrical performance, as larger diameter

wires provide a wider surface area for contact with the fingers on cells, thus, a better contact between the wires and fingers. In addition, additional solder provides more solder material to form better soldering patterns between wires and fingers [145].

Figure 6-20 shows the relative change in fill factor in using wires with different materials, wire diameters, and solder thicknesses indicate significant reduction in performances of the modules with thermal cycling, regardless of the wire materials used or the solder thickness. However, as discussed earlier, the trade-off between using wires with larger diameters with wider surface contact area and power loss due to shading effects discourages the use of wires with larger diameters. In addition, the results indicate that using wires with smaller diameters, but with a thicker solder layer, may be the best approach towards a solution for the trade-off.

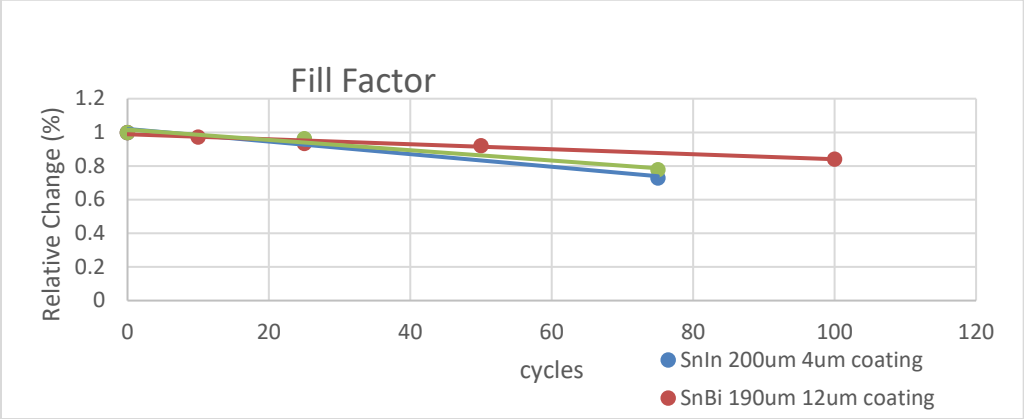

Figure 6-20. Relative change in fill factor is measured as a function of the number of cycles as we well as the wires materials and dimensions. Cell performance is significantly reduced regardless of the wire materials and dimensions, indicating degrading issues at the polymer – cell interface are more likely causing interconnection issues, regardless of solder and wires.

6.2.4. Real-time Monitoring Inside the Module: Temperature variations

Following the soldering results, it became imperative to investigate the thermal conditions within the module in order to determine the optimal lamination process temperature. Real-time monitoring of the temperature inside the modules during the lamination process, would provide insight into whether the temperature inside modules reaches laminator-set temperature targets. The ideal temperature exceeds thresholds required for solder material to melt in order to flow towards the cells' metallization and form a well-distribution of phases within the solder joint, thus, forming effective electrical bonds between wires and fingers on the cell. On the other hand, the temperature needs to be maintained within a certain range so that polymer viscosity does not decrease below a certain point, due to high temperature, otherwise, depending on the polymer viscosity, liquified polymer would flow underneath wires, thus, forming an insulating layer between the wire and the cell and preventing the formation of solder joints [145].

In order to monitor the temperature distribution inside the layers of the module in real-time, the experiment was set using thermocouples and a microcontroller readout. Type- K Thermocouple with diameter of 0.6mm and temperature range of -50°C -250°C (RS components Ltd.) were placed on each layer of the module. The thermocouples were connected to a microcontroller (Arduino Due) programmed with a custom code to read the temperature output from several thermocouples in real-time.

Figures 6-21 and 6-23 show the setup with several thermocouples attached to different materials and the microcontroller to test their temperature distribution throughout the lamination process. More details about the laminator and the lamination setup used is discussed in other sections.

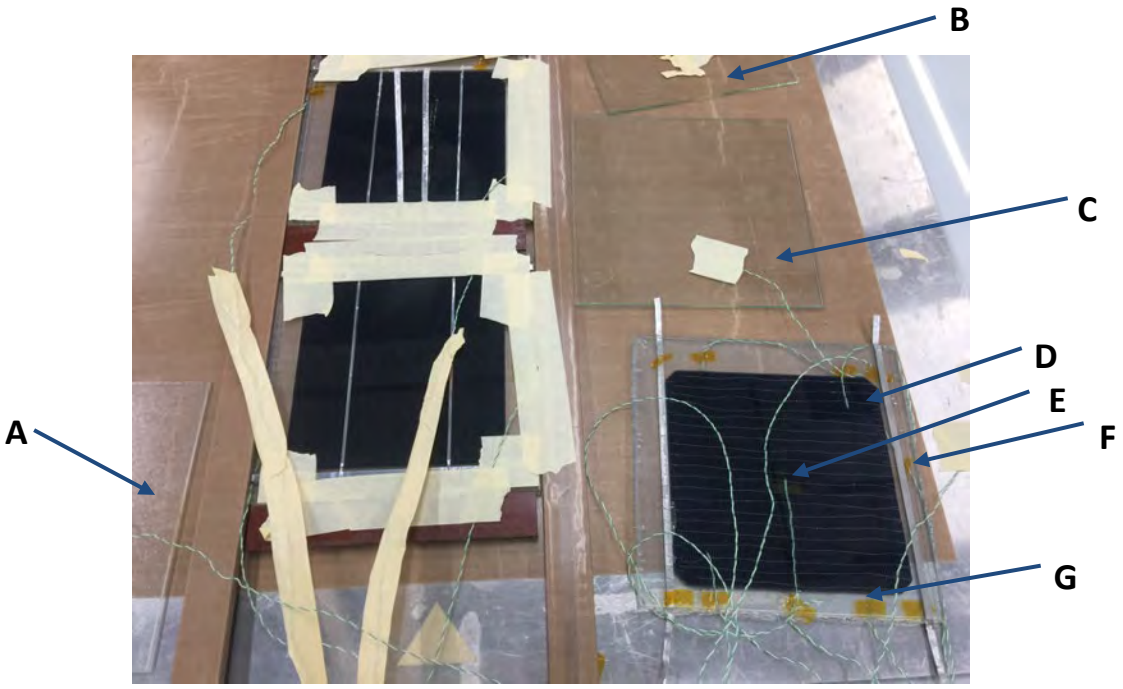

Figure 6-21 Thermocouples are placed on several materials during the lamination step to study the temperature distribution within the module. Thermocouples are placed onto glass A-C, glass (4mm textured, 3mm, and 4mm) respectively to study the temperature uniformity across the two opposite layers of the module. D and E, thermocouples are placed onto corner and centre of the front side of the solar cell respectively to study the temperature uniformity both sides of the cell. G, corner of the back side of the solar cell. F. Thermocouple placed at the TPO-A – cell interface to study the differences in temperatures variations throughout the lamination/encapsulation step. Not shown in the image, thermocouples placed on the aluminum plate, heating plates of the laminator, and the teflon sheet.

The preliminary results indicate that the temperature distribution within the module is not as uniform as originally expected. When the laminator is set to reach a temperature of 155°C during the process, the solar cell does not actually reach the set temperature, by around 10 °C, possibly due to the thermally insulating properties of the TPO-A foil, as shown in Figure 6-21. In addition, the temperature in some parts of the cell only starts to approach the melting range of Bi57-Sn42-Ag1, the solder coating layer on the interconnection wires, only towards the end of the lamination process.

Following these results, the temperature distribution starts to slowly plateau after 11 minutes of lamination, thus, a lamination period of 20 mins may be unnecessarily longer than needed. Thus, slightly increasing the process temperature to ensure that the temperature distribution within the module, particularly the temperature of the cell itself, is well within the melting range of the solder coating on the wires. In addition, the overall lamination time was reduced to 11 minutes. As discussed earlier, reducing the overall time the polymer foil is pressed helps reduce the creeping effect and deformation within the encapsulant layer.

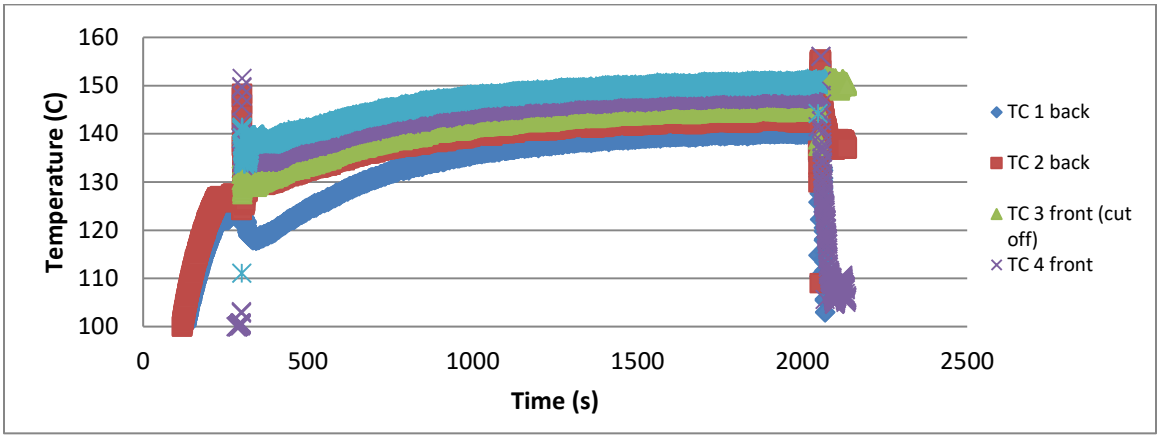

Figure 6-22. Temperature distribution of TPO-A within the module with the laminator set temperature at 155°C. The temperature of the materials inside the module do not reach the set temperature, even after 20 minutes (press-time) of lamination. The backside of the cell starts to approach the melting range of Bi57-Sn42-Ag1 towards the end of the lamination process.

Figure 6-23. Temperature variations studied during the lamination process A. Optical image of thermocouple placed in between TPO-A layers. B,C. Thermocouples are connected to a microcontroller (Arduino Due) to measure temperature readouts during lamination. D Temperature variations readouts are recorded throughout the lamination process.

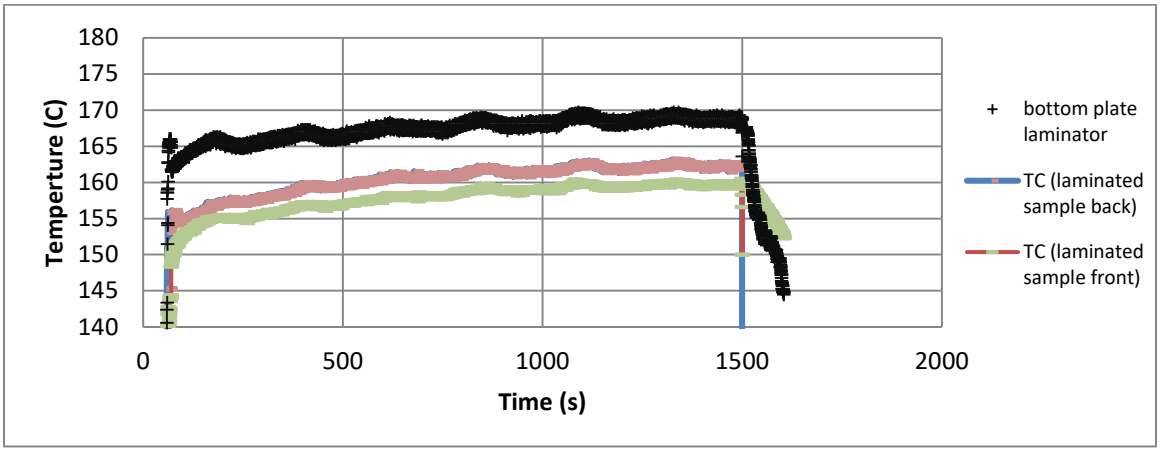

Figure 6-24. Temperature distribution of TPO-A within the module, where the laminator temperature is set to 165°C. The temperature of the materials inside the module were monitored to ensure that the temperature reaches the melting temperature range of the Bi57-Sn42-Ag1 solder-coated interconnects. By understanding the temperature variations, the lamination process time was significantly reduced, by reducing the pressing step to 11mins.

Figure 6-24 shows the temperature distribution inside the module when the temperature was set to 165°C. The results indicate that the temperature within the module reaches the intended melting range of the solder coating material on both sides of the module. Figure 6-25 shows the EL images of two types of TPO material. The slight enhancements in the process significantly improved the wires-fingers connections at the sides of the module. However, the degradation within the module after 50 thermal cycles was still significant, as the central regions of the module start to lose connections as a function of thermal cycles. Fill factor measurements in Figure 6-26 also confirm that the degradation in the modules' performances.

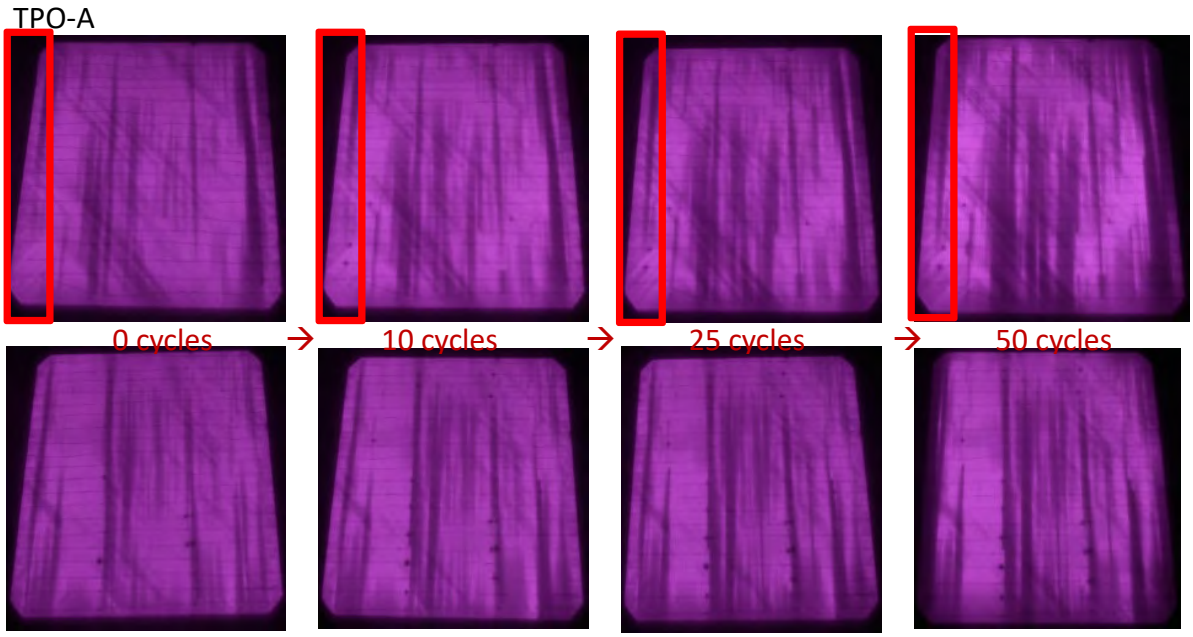

Figure 6-25 shows the EL images of two types of TPO material post lamination at parameters of 165°C, 700mbars pressure, and press-time of 11mins. Images show improved connections at the sides of the module. However, degradation appear within the module as a function of thermal cycles.

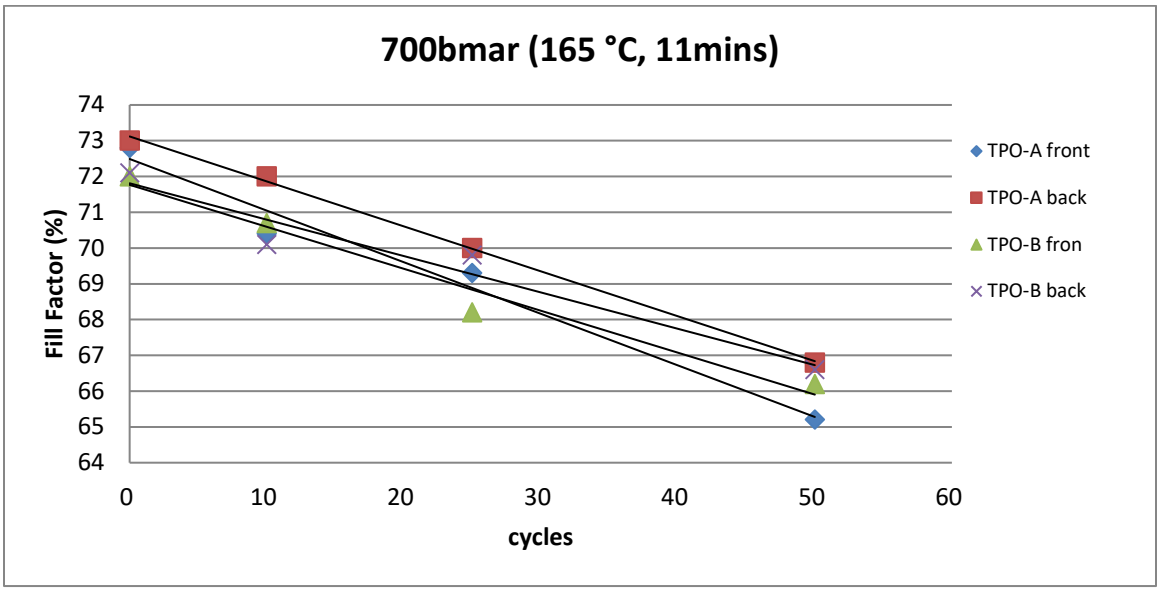

Figure 6-26. Significant degradation in performance of the samples prepared after 50 thermal cycles, as expected, due to modular degradation.

6.2.5. Pressure Effects on The Lamination Process

Time and temperature play an essential role in polymer rheology, as mentioned previously. On the other hand, pressure variations play an indirect role in affecting the viscoelastic properties and relaxation time in polymers. Polymers with bulkier and more dense side groups show greater pressure dependencies compared to less dense polymers with smaller side group chains. Increasing pressure on polymers with bulkier side groups, causes a reduction in the free volume within the polymer matrices, thus, resulting in an increase in the elastic modulus and changes in viscosity and the subsequent increase in polymers' stress relaxation times [184], [205]–[210].

An in-depth insight into the TPO's complex shear modulus and the complex viscosity in our setup would be essential in predicting polymer behaviour under pressure and temperature. As noted earlier, other group members are currently working on quantitative analyses, as well as the non-linear viscoelastic behaviour of TPO, i.e. the non-linear relation between tensile stress and tensile viscosity in the polymer. It followed from the previous reduced press-time experimental results, that reduced stress within the polymer, due to decreased pressing time during the lamination process and subsequent reduced creep effects, would follow if pressure during the press-step is reduced, which is also supported by the experimental results that followed.

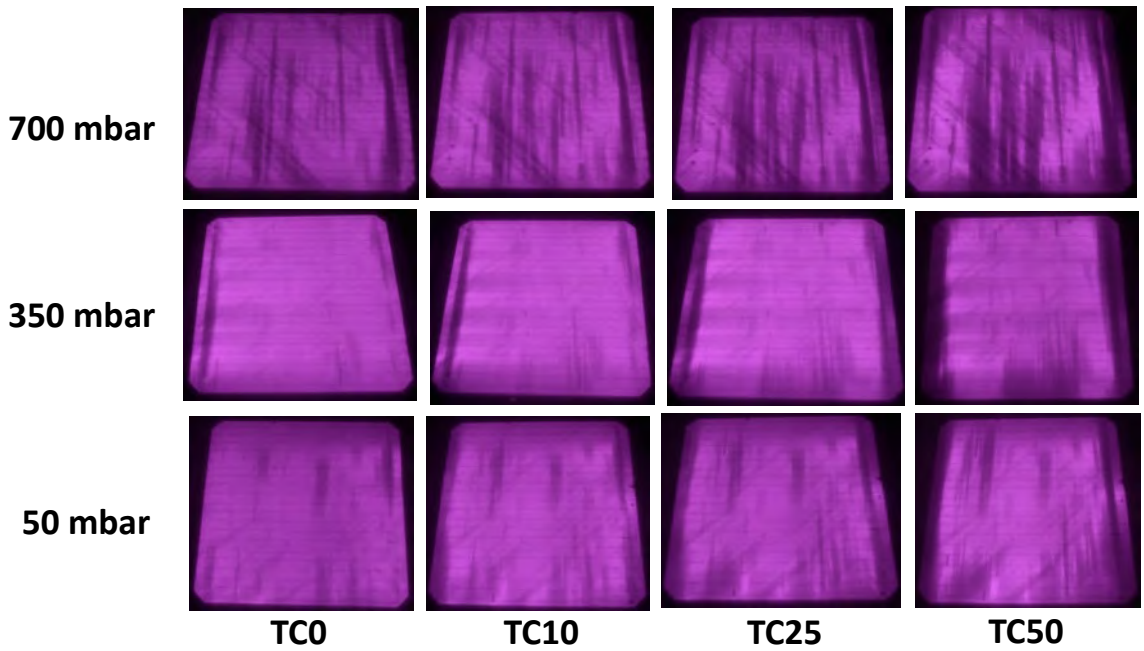

Figure 6-27. EL images of modules prepared at pressures 700mbars, 350mbars, and 50mbars during the press-step [165°C and 11mins]. Images show improved connections at the sides of the module at lower pressures. However, degradation persists within the module as a function of thermal cycles, regardless of pressure.

Figure 6-27 shows the EL images of modules prepared as pressure is reduced during the press-step at optimized temperature and time. Images show improved connections at the sides of the module at lower pressure most likely due to the reduced creeping effect at reduced pressure, as discussed earlier. The improved connections may be an indication that deformation within the polymer due to the induced internal stresses at higher pressure, or longer pressing time, may be inducing high enough forces to push or shift wires within the module causing loose connections. However, as in laminations at high pressures, the performance of the modules still degrades significantly after rounds of thermal cycling, figure 6-28. The series resistance increase in the module would perhaps support the theory behind degradation in performance and increased darker regions in EL images are due to more loose connections throughout the module after thermal cycling

due to the effects mentioned. Thus, decreasing pressure, and subsequently creep modulus, reduces the percentage of loose connections.

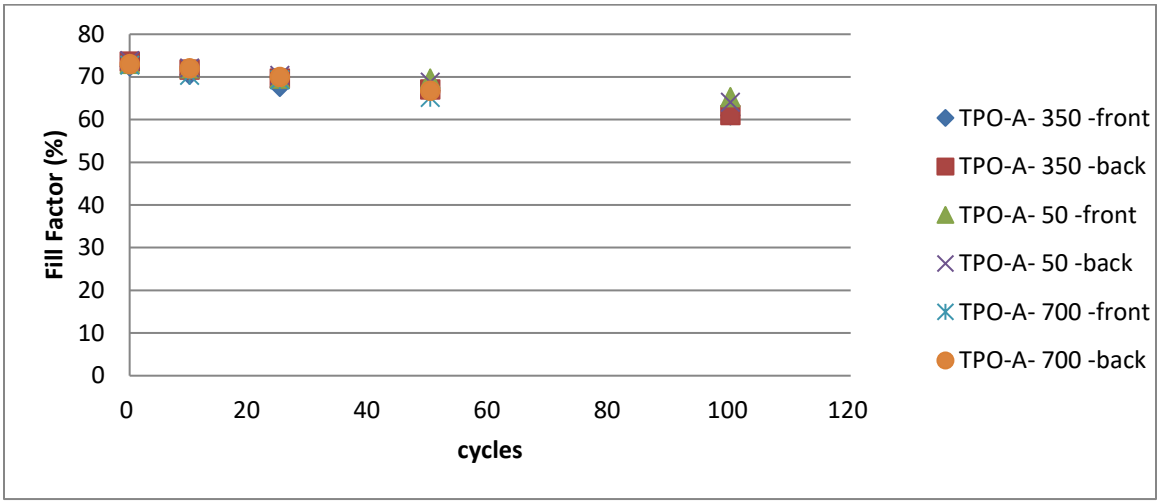

Figure 6-28. Fill factor of modules prepared at pressures 700mbars, 350mbars, and 50mbars, during the press-step of the lamination process [165°C and 11mins]. Performance degradation across pressure indicates that reducing the pressure during lamination causes better polymer- cell contact. The contact improvements don't hold against the extreme fluctuations during thermal tests.

Figure 6-29 shows that the series resistance increased by a significant margin, 42.28%, after 50 thermal cycles at 700 mbars, on the other hand, the series resistance increase for the samples prepared at 350 mbars increased several rounds of thermal cycles. In figure 6-30, variations in Isc are shown, and the changes in Isc are small and within the range of measurement error. A decrease in Isc indicates an increase in the inactive cell area, while an increase in the series resistance of the cell, in the absence of cracks in the cell or module, is mostly due to loosening connections. Despite the improvements in performance, the degradation in performance is still significant, as the target performance degradation is set to less than 5% after 200 thermal cycles.

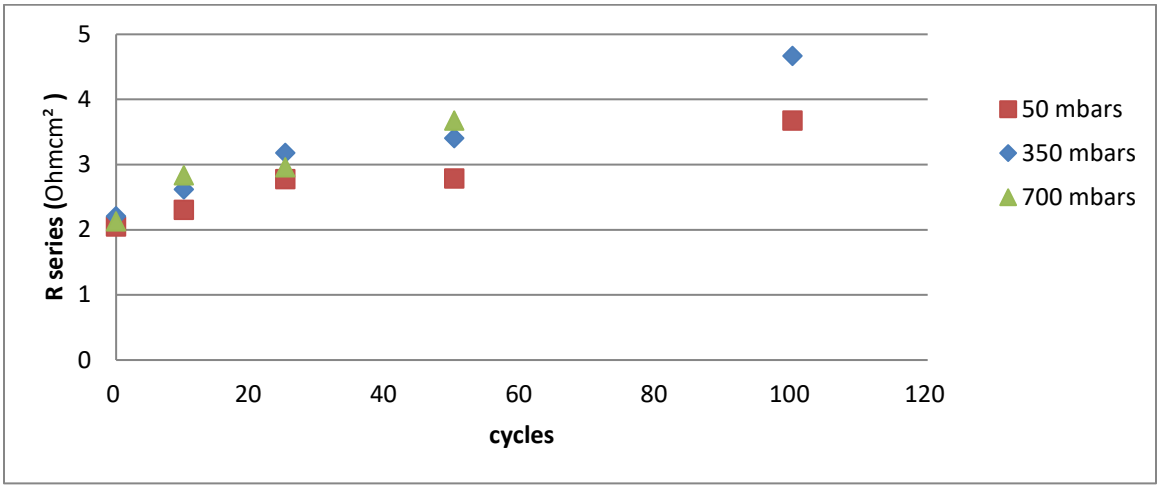

Figure 6-29. Series resistance within the modules prepared at pressures 700mbars, 350mbars, and 50mbars, during the press-step [165°C and 11mins]. Rs increased by 42.28% after 50 thermal cycles at 700mbars, by 52.68% after 100 thermal cycles for 350mbars, and 44.29% after 100 thermal cycles for 50mbars. This further emphasizes that connections the interconnect-finger interface are not present anymore in significant portions of the cell.

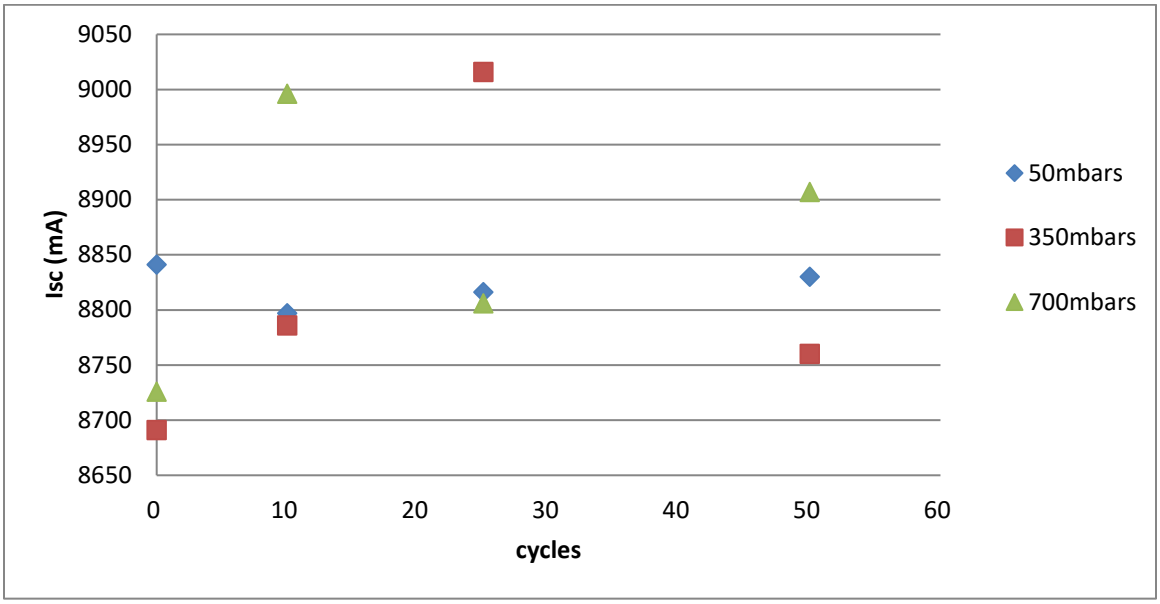

Figure 6-30. Isc of modules prepared at pressures 700mbars, 350mbars, and 50mbars, during the press-step of the lamination process 165°C and 11mins, as a function of thermal cycles. The changes in Isc are insignificant are small, and within the range of measurement error, as expected.

6.2.6. Composites and Other Enhancements to TPO-A

Following the previous results, there were several attempts at varying TPO-A materials and properties (from the manufacturer), including making TPO-A more viscous as well as increasing the melting temperature of the polymer. However, the performance was either worse to begin with or the degradation after a few thermal cycles was much more significant than that of TPO-A. TPO-A with higher viscosity would most likely exhibit a more elastic-like behaviour, due to the higher creeping modulus, especially during the pressing-step of the lamination process. As shown in the EL images, Figure 6-32, the effects indicate higher internal stresses on the cell and wires, thus a higher percentage of cracks in the cell. In addition, the encapsulants with high viscosity needs additional process time to flow and fill the gaps within the module, where remaining unlaminated patches may lead to delamination issues. On the other hand, given the temperature distribution variations within the module during the lamination process, discussed earlier, it is possible that the higher melting point, of the modified TPO-A, likely implies that the encapsulant layer did not uniformly melt across the module with remaining unlaminated patches, causing the modules to have unbalanced internal stresses, thus a higher number of cracks in the cell. However, a quantitative analysis would provide a more conclusive insight.

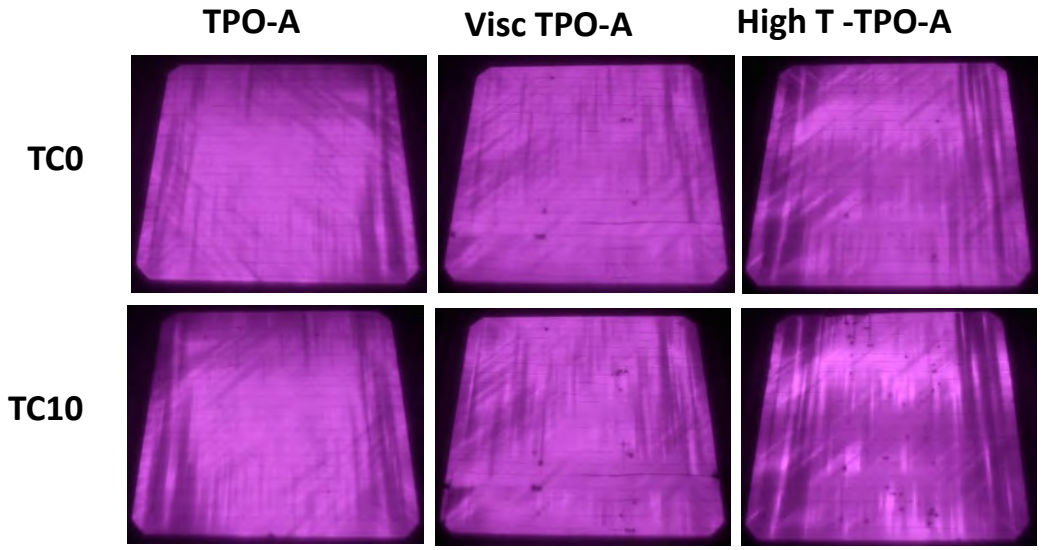

Figure 6-31. EL images of TPO-A and modified versions of TPO-A with higher viscosity and higher melting points as a function of thermal cycles. Images show cracks in the cells after 10 thermal cycles. Module stress, and associated stress at interconnect-finger interfaces, seem to be primarily affected by the polymer properties within the module.

6.3. Thermal Variations in The Encapsulant Layer Due to Wires and Aligned Fiber Glass Integration

In an attempt to study thermal variations within a PV module setup, thermal resistivity changes in encapsulant foils and composites were estimated as a number of parameters were changed. It is estimated that 2.2% to 17.5% of annual losses in performance of cells, and subsequently modules, is mainly due to temperature [211], [212]. A number of studies have shown thermal ambient effects on PV cells' performances [136]–[138], [213]–[215]. In addition, there is an increasing interest in the use of multi-wire interconnection concepts and schemes in c-Si PV applications, including 2-sided contacts, such as bifacial and busbarless cells. In such setups, there's a trend towards the increase use of composites utilizing woven fabrics, containing aligned and patterned fiber glass, as

means to increase mechanical durability along with the demonstrated optical and electrical potential in decreasing losses in performance due to shading and resistive transport losses [139]–[143], [213], [216], [217].

Thermal conductivity, the inverse thermal resistivity in systems, denotes the capability of material to conduct thermal energy across an object. Thermal conductance at the interfaces is mainly dependant on surface roughness and thermal conductivity differences in the materials at the interfaces as well as the contact pressure between the materials [218], [219]. Thermal conductivity of a sample, k, can be calculated using Fourier's law of heat conduction

$$k = \frac{QL}{A(\Delta T)} \qquad (6.8)$$

Where ΔT is temperature difference between the object's interfaces at a steady state energy flow, Q, across an object with length L and cross-sectional area A.

The two main methods used to measure thermal properties are steady-state methods, where thermal properties are measured by establishing a temperature difference, between two interfaces, that does not change with time, and transient methods, where energy or thermal flow between two interfaces is time-dependent. The transient thermal measurement method was initially developed to characterize the bulk thermal conductivity and the thermal contact resistance of underfill materials in die-die interfaces in 3D stacked structures for 3D- integrated circuits. Combined with thermal finite element simulations, thermal properties of the material, such as thermal conductivity can be measured [217], [219], [220]. The transient thermal measurements of the encapsulant material is utilized, using a thermal test chip with integrated heaters and temperature sensors, to study the thermal response variations in the thermally insulating encapsulant

material, thermoplastic polyolefin, TPO-A. The samples are prepared to represent the exact layup of solar cell modules, while varying parameters such as encapsulant thickness, in addition to varying the position of the wire interconnections within the encapsulant, and including multiwires woven with aligned grids of glass fiber, in the encapsulant foil. The method combined with thermal finite element simulations could potentially be used to characterize the bulk thermal conductivity of the encapsulant material and composites used as well as the thermal contact resistance at the different interfaces. Figure 6-32 shows the experimental setup.

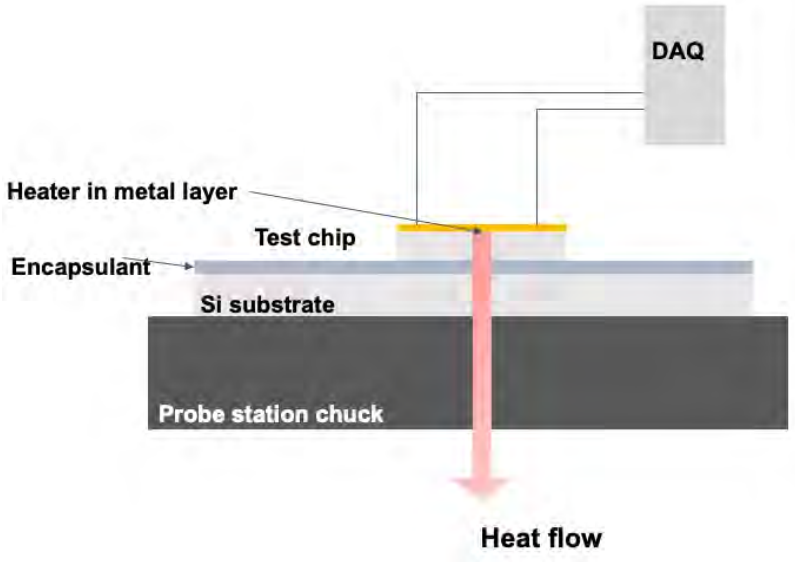

Figure 6-32. Schematic of the experimental setup to measure thermal variations within the module layers. A test chip is laminated onto a substrate with various encapsulant layer compositions. Heat flow across the layers is measured through the temperature sensor on the chip as the temperature variation is measured between the chip itself and the probe station chuck.

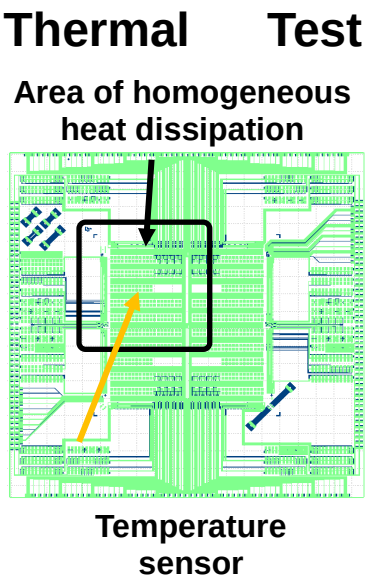

Figure 6-33. The layout of the thermal chip showing heater resistors and meander resistors acting as temperature sensors.

Samples were prepared by laminating polyolefin elastomer encapsulant in between a thermal test chip and a silicon substrate (800μm thick), figure 6-33. The samples are placed on the probe-station chuck, and a probe station and a data acquisition microcontroller (National Instruments DAQ), connected to a computer, are used to:

(1) apply a constant power to the heating elements of the chip,

(2) supply a constant current through the temperature sensor resistors, and

(3) collect voltage measurements from the latter resistors, illustrated in Figure 6-33.

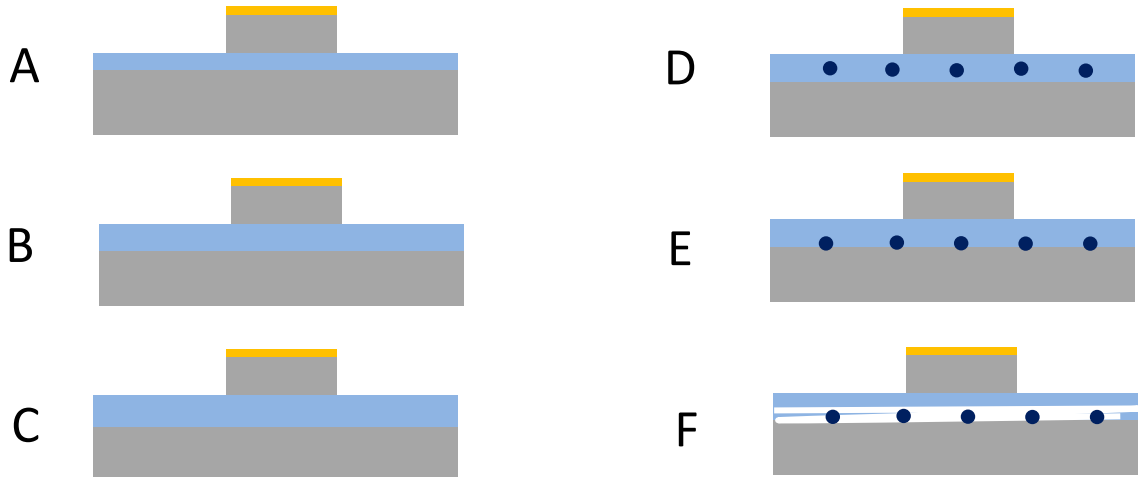

Figure 6-34 shows the schematic cross-section of each sample: samples with bare encapsulant and varying thickness. (A-C), encapsulant with metal wires completely decoupled from the samples. D, encapsulant with metal wire in contact with the cell, and F, metal wires in the glass fiber matrix. Temperature variations were measured across the different samples.

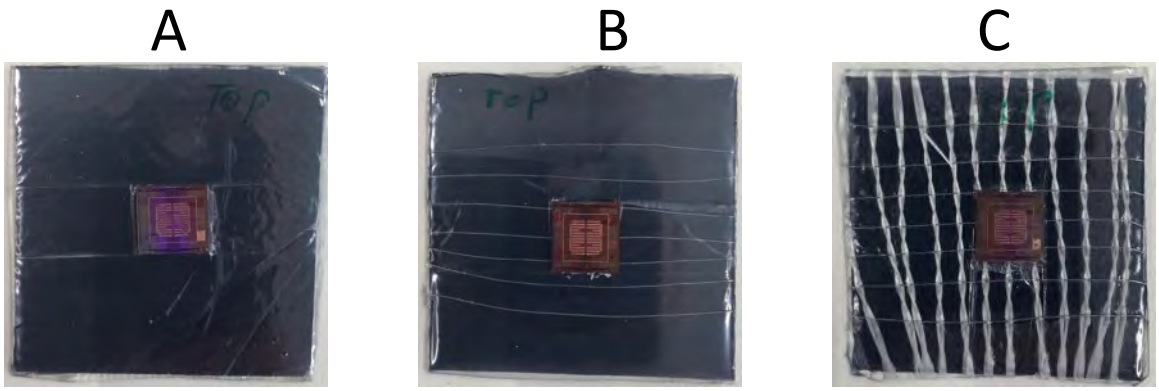

Figure 6-35. Images of some of the prepared samples. A. no metal interconnections. B. Metal interconnections embedded in encapsulant. C. Fiber-woven metal interconnections embedded in encapsulant. The samples were encapsulated as if they were regular modules to ensure the module lamination characteristics are not varied.

Voltage is applied as a square wave function to the heater resistors for power dissipation in the test chip, while the transient response of the sensor resistor voltage is measured (Figure 6-34. B). The voltage variations at the sensor resistor yield a local temperature, and the temperature coefficient of resistance for the sensor resistor material

is used to calculate the average temperature increase in the test chip. The samples undergo one heating-cooling cycle, in which the samples are heated up for a specified amount of time, figure 6-34.A, then, the samples cool down. Thermal impedance determination is where constant power PL is fed into the sensor module by a current flow, and a certain pre-determined junction temperature T_j is reached after a transient period. After turning off the power to the sensor module, the cooling down of the module is recorded.

The thermal resistance $R_{th(x-y)}$ is the difference between two temperatures T_{x0} and T_{y0} at t=0, divided by the power PL, and the time dependent thermal impedance $Z_{th}(t)$ between the two points x and y is calculated as [217], [221]

$$Z_{th} = \frac{V_{d,0} - V_d\,(T)}{\sigma . P} \qquad (6.9)$$

where $V_{d,0}$ is the initial voltage on the sensor at the chuck temperature T_0, $V_d(T)$ is the sensor voltage at temperature T, σ is the resistor sensitivity, and P is the dissipated power.

In addition, the top side of the chip is covered with thermally insulating material, thus causing the heat generated at the chip to preferentially flow through the encapsulant towards the chuck, which acts as a heat sink. A reference measurement, where the test chip is directly placed on top of the substrate (i.e. with no encapsulant present) is used to determine ambient heat losses and convectional heat dissipations. The dissipated power is obtained as follows:

$$P = V_{applied}\, I_{measured} \qquad (6.10)$$

where $V_{applied}$ is the voltage applied to the heater and $I_{measured}$ is the measured current of the heater resistor.

Figure 6-37 shows the outcome of the transient measurements where the thickness of the encapsulant was increased (sample types A-C). The increase of steady-state temperature as the thickness of the thermally insulating encapsulant increases is expected as explained by equation 6.11, which states the relation between thermal resistance and material thickness.

$$R = \frac{\Delta T}{QL} \quad (6.11)$$

where ΔT is the change in temperature, Q is the heat flow rate, and L is the thickness of the material.

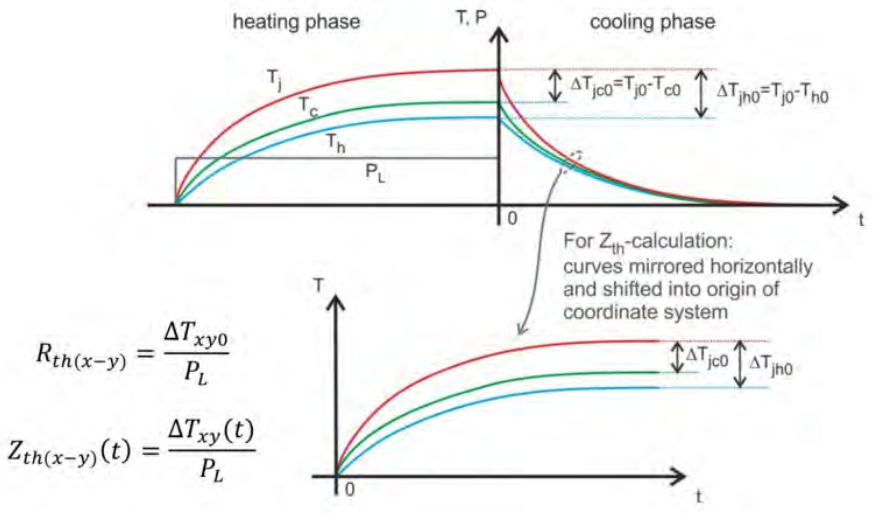

Figure 6-36. Principle approach to transient, time dependent, thermal impedance measurement. The thermal resistance is affected by the material thickness [221].

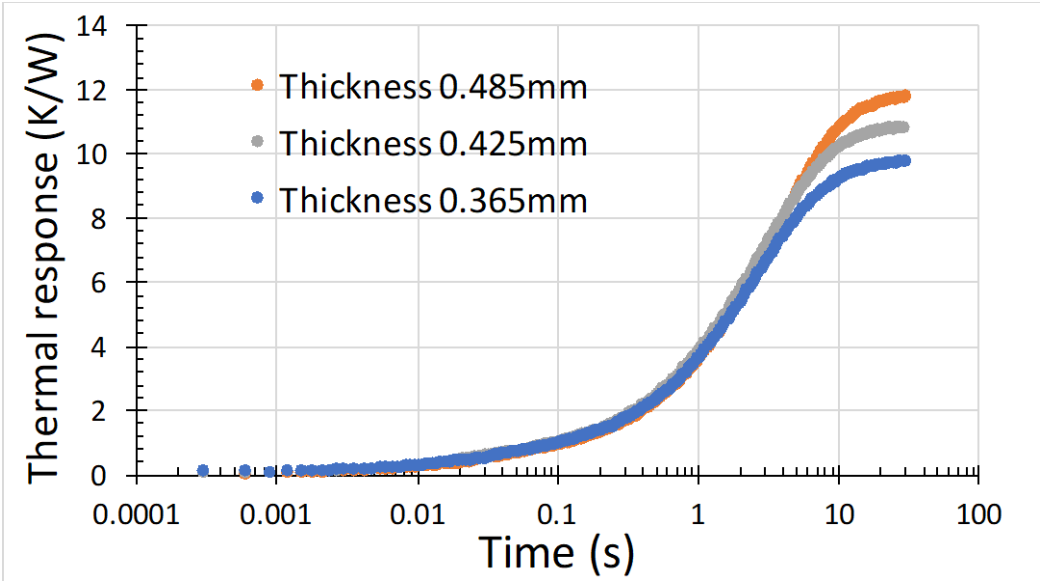

Figure 6-37. The thermal response is measured due to the thickness of the encapsulant, TPO-A, is varied. The thicker the polymer layer, the higher the thermal response, as expected, as the polymer acts as a thermal insulator.

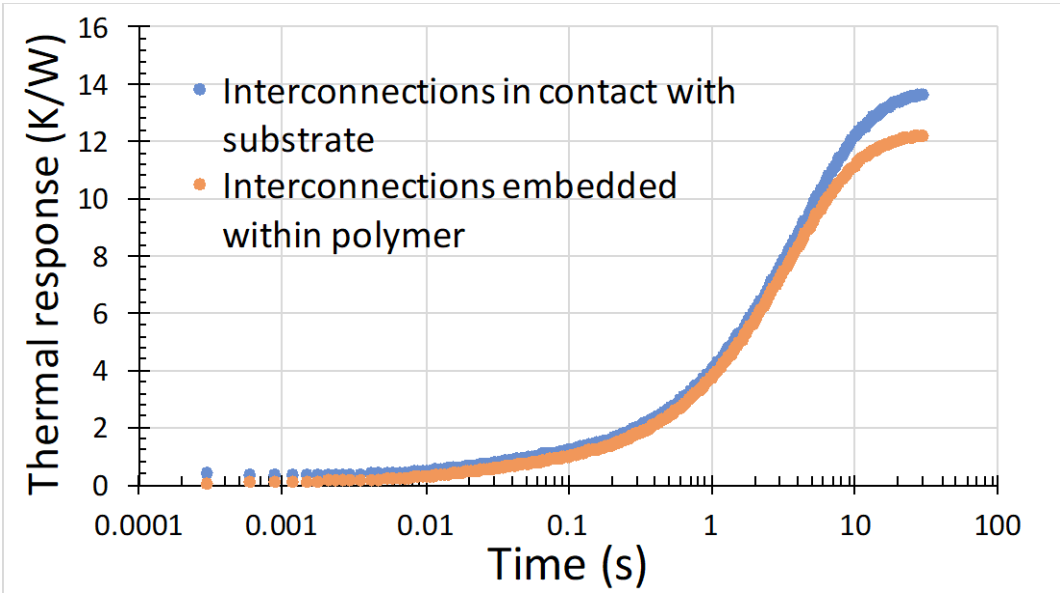

Figure 6-38. The thermal response is measured due to the addition of metal interconnects within the encapsulant layer itself (sample type D) or at the surface of the polymer layer to ensure contact with the substrate (sample type E). Interconnects (thermal conductors) in contact with the substrate ensure a more uniform thermal distribution, as expected.

The samples with metal interconnections (D-E) have a higher thermal response compared to the bare encapsulant (A-C), which is likely due to the increased thickness. Embedding interconnections within the encapsulant (D) causes a lower thermal response compared to the case when the metal interconnection wires are in contact with the Si substrate (sample type E), as shown by Figure 6-38. Intuitively, this could be explained by the heat sink effect induced by the wires, by drawing away heat laterally. The closer the wires to the heat source (with sample type D closer than E), the more they will sink heat from the source, and the lower the thermal response.

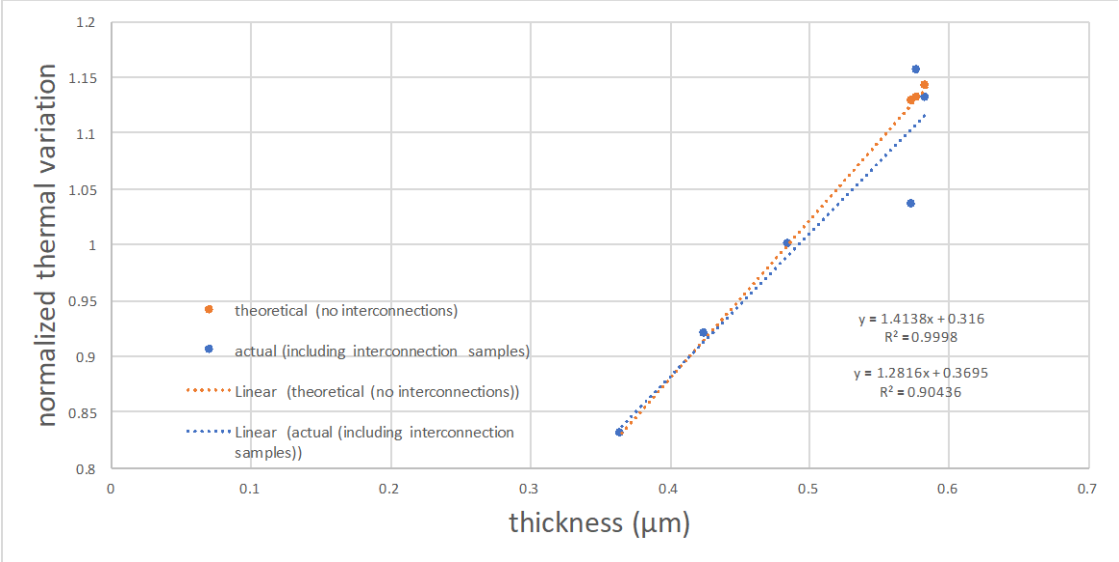

Figure 6-39. Using the relation between thickness and temperature variation, temperature variation values for samples with higher polymer thicknesses were extrapolated. The actual responses match the theoretical values, indicating the likely heat sink effect induced by the wires, by drawing away heat laterally.

Alternatively, including glass fiber-woven metal interconnection wires results in a minimal alteration of the thermal response compared with non-fiber-woven samples as illustrated in Figure 6-40. However, when compared with an encapsulant of similar thickness with no interconnections, the fiber-woven sample indicates a slightly lower

thermal response, thus suggesting that embedding fiber-woven interconnection helps to slightly lower the thermal resistivity, however, the overall thermal effects are insignificant.

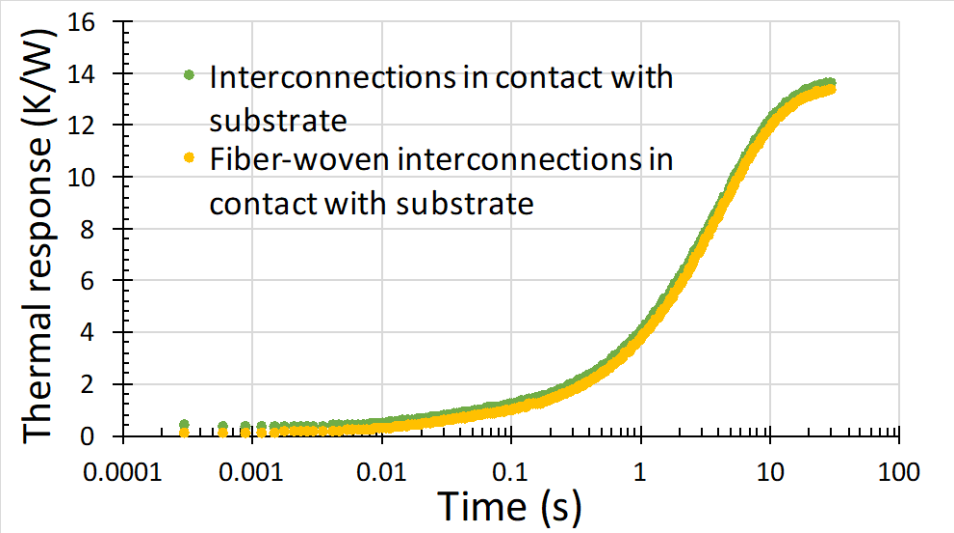

Figure 6-40: The variation in thermal response between samples when a fiber-woven interconnect is added. The thermal response is insignificant, indicating that the added materials (bringing mechanical strength to the polymer layer) do not affect the module response (from a thermal perspective).

Following transient thermal measurements, the impact of thermal properties of encapsulant on the overall impact of energy yields in PV modules were simulated in moderate and desert climates. Oldenburg, Germany, is used to represent a city with moderate climate, and Kuwait City, Kuwait, is used to represent a desert climate. In order to simulate energy yield impacts of varying encapsulant material and properties, especially under a desert climate, accurate modelling of material properties and arrangements are essential in order to obtain accurate thermal management within the module. Thus, physics- based exploratory modelling of PV energy conversion was used for the simulation. The modeling takes into account previously measured environmental conditions, consisting of a time series of irradiation (global horizontal, direct normal, diffuse horizontal), ambient temperature, wind speed, and direction. In addition, cell electrical and

thermal behavior, optical absorption and generation, as well as thermal conduction, convection and radiation are set by the material properties of the different layers. A full description and demonstration of this modelling approach can be found in [213]. In this regard, the impact of varying some encapsulant properties, such as altering encapsulant material from polyolefin to EVA as well as varying polyolefin thickness, on the overall impact of energy yields in PV modules is studied. Figure 6-41 shows the module layers are from back to front: back sheet (Polyvinyl fluoride), encapsulant (EVA), Si wafer, encapsulant (EVA), and glass.

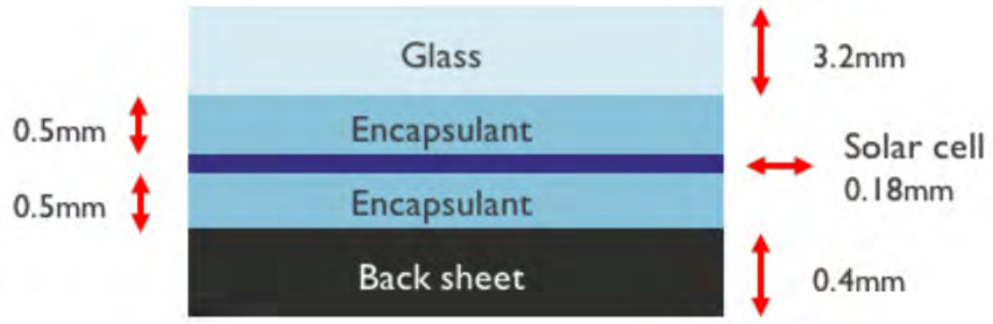

Figure 6-41 Simulated module layup (glass - backsheet) with materials and layer thicknesses [213].

The simulated modules face South under both climates, where the modules in Kuwait City are tilted at 30° from horizontal, representing the optimal highest annual in-plane insolation. On the other hand, the module tilt angle in Oldenburg is 40°, less than optimum, corresponding to the higher latitude of the city [213], figure 6-42. Figure 6-43 shows module temperatures in Oldenburg and Kuwait city throughout the year due to measured environmental conditions.

Figure 6-42 shows the simulated annual energy yield in Oldenburg, as encapsulant material is varied from polyolefin to EVA. Encapsulant thermal behavior in the two

encapsulant materials appear to have negligible impact on the energy yield in the module. On the other hand, increasing polyolefin thickness significantly from 1 layer to 5 layers, insignificantly decreases the annual energy yield of the module, as the energy yield gets reduced by 0.31%.

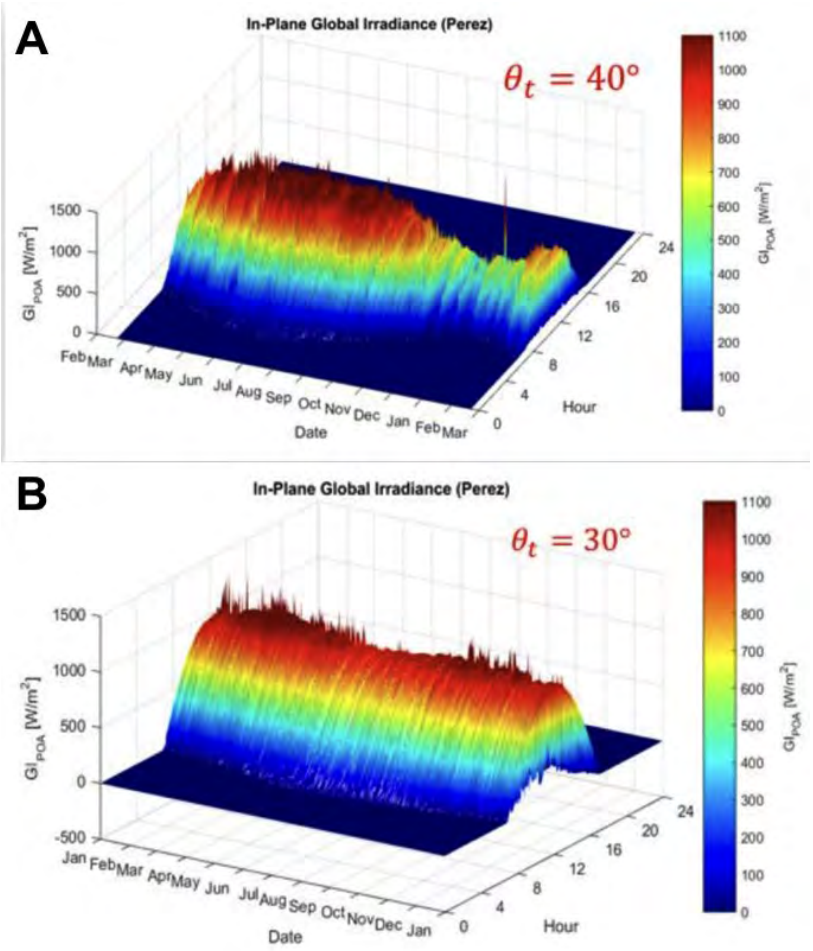

Figure 6-42. Measured irradiance quantities transformed into in-plane global irradiance values on the PV module surface, according to the Perez model [213], at tilt angles θ_t=40° in Oldenburg (A) and θ_t=30° in Kuwait (B).

The reduction in energy yield results are consistent with the transient temperature response measurements discussed earlier, as the encapsulant with the least thickness experienced the least thermal resistance. Figure 6-40 shows negligible thermal response

within the module after fiber woven interconnections were added. Consequently, the material, surrounding the solar cell within the module, with the least thermal response causes the least energy yield losses.

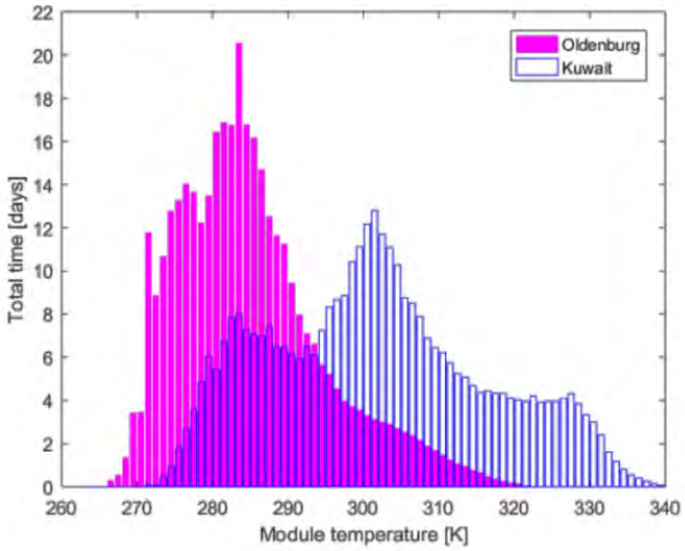

Figure 6-43. Module temperatures in Oldenburg and Kuwait city throughout the year due to measured environmental conditions. The latitude difference between the cities indicates that energy yield for Oldenburg is better in the summer days. In Kuwait, the overall temperature distribution is more uniform.

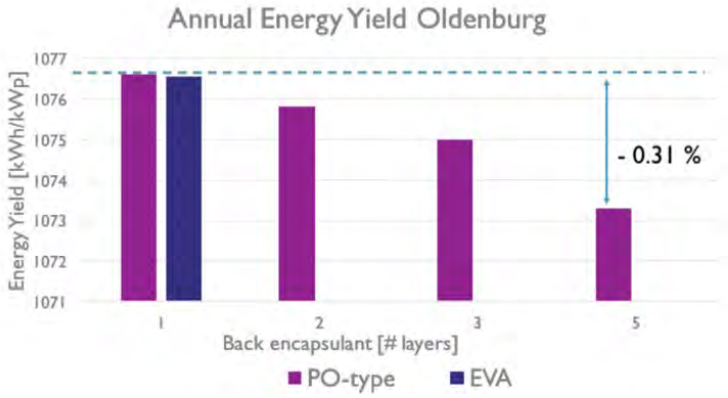

Figure 6-44. Annual energy yield in Oldenburg, comparing responses of using encapsulant material polyolefin and EVA as well as varying polyolefin thickness. Increasing polylefin thickness reduces annual energy yield by 0.31%, and changing the encapsulant to EVA has negligible effects.

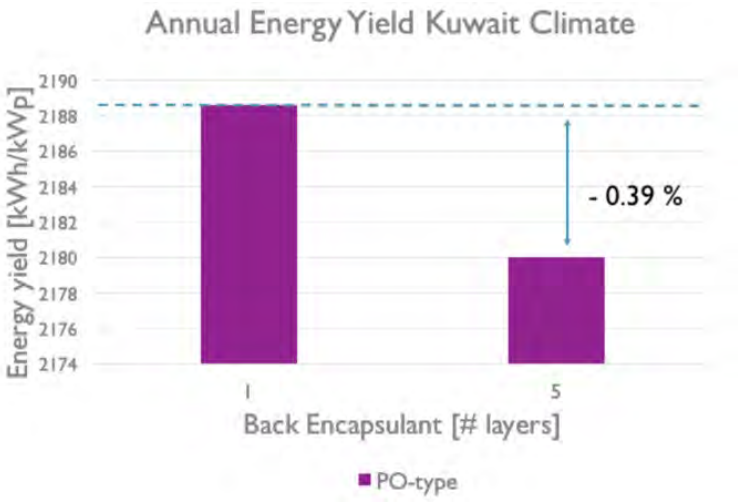

Figure 6-45. Annual energy yield in Kuwait. Increasing polyolefin thickness reduces annual energy yield by 0.39%.

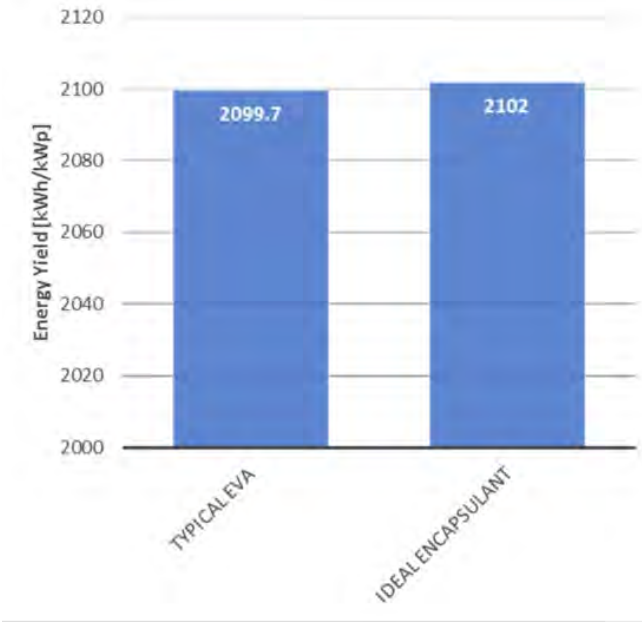

Figure 6-46. The impact of thermal properties of EVA on the overall energy yield in ideal conditions, at no thermal resistivity and no thermal capacity, vs in a typical case in Kuwait conditions and interdigitated back contact solar cells used. In the typical EVA case, the energy yield is reduced by 0.11%.

On the other hand, Figure 6-45 shows the simulated annual energy yield in Kuwait, as TPO thickness is significantly increased from 1 layer to 5 layers. Due to environmental conditions, the annual energy yield in Kuwait, more than doubled compared to Oldenburg, but still the encapsulant thermal effect on the overall energy yield of the module is insignificantly reduced by 0.39%. In addition, the impact of thermal properties of EVA on the overall energy yield in ideal conditions, at no thermal resistivity and no thermal capacity, is compared to the typical case in Kuwait conditions. Interdigitated back contact solar cells (IBC) type is used in the module, as in figure 6-47. Simulation results show that even with IBC, exhibiting the most absorption among solar cells, the reduction in energy yield is negligible at 0.11%.

Thus, the impact of different thicknesses of encapsulant and of interconnection wires either directly or partly contacting the cells is compared. Preliminary measurements of embedding aligned fiber glass within the encapsulant foil has minimal effects on the thermal response, compared to when no fiber glass were embedded. Furthermore, simulation results show that altering encapsulant material from polyolefin to EVA as well as varying TPO thickness has a negligible impact on the overall impact on energy yields in the PV module.

6.4. Results: Integrating Optimized Parameters to Weaves and Other Materials Into The Encapsulant Foil

Despite the insignificant energy losses introduced into the module by adding an aligned fiber glass weave and associated thermal response, the reinforced durability introduced due to the composite foil enhances the mechanical durability of the module.

The mechanical properties of fiber reinforced composites are dependent on environmental factors including temperature and humidity as well as the chemical stability at the interface fibers-matrix bonding interface. Fiber properties, including its strength and modulus depends on parameters such as fiber length as well as whether the fibers are woven or chopped, also contribute to the chemical and mechanical stability within the composite. On the other hand, depending on the applications of the composite, fibers can be integrated by simply laying the fibers on the polymers during the composite preparation step, or the fibers can be laminated, under high pressure and temperature, to ensure that the fibers are embedded well within the polymer matrix. In addition to the mechanical and chemical advantages of reinforced composites over polymers in some applications, the use of filler materials, including glass fiber, reduces the overall materials cost, as less polymer material is required to prepare composites, thus making them cost effective for applications where polymer integration would be an issue due to their relatively higher implantation costs. However, some of the setback of using glass fibers is that they are highly hygroscopic, as they tend to absorb moisture from the air and surrounding environments, leading to loss of interfacial adhesion and decreasing fiber strength within composites. In addition, fiber glass integration may be an issue in stress induced applications, as stress may lead to the glass fibers cracking or breaking, thus, degrading interfacial adhesions and cause durability issues. Further, filament fractures within a region may disseminate fractures and cracks into the fiber-polymer matrix or along the interface, thus, complicating precise prediction of long-term behavior [222]–[230].

In addition, poor fiber–matrix interfacial adhesion may negatively affect the physical and mechanical properties of the resulting composites due to the surface incompatibilities. However, the treatment of glass fibers with epoxy or coupling agents

compatible with the polymer matrix enhances the mechanical properties of the compounded polymers. The treatments promote chemical and mechanical bonding between the fibers and the polymer matrix, thus, enhancing rigidity of the polymer matrix and protecting the glass fiber reinforcement material from environmental damage, such as humidity, for extended periods. Custom treatments are also used to enhance particular features within a matrix over other features, such as increasing in the elastic modulus while reducing tensile strength properties. For example, silane based epoxies contribute to the formation of a water-resistant polymer network between the bulk polymer matrix and the glass reinforcement as well as the reduction of filament fractures due to the formation of a more rigid matrix. Furthermore, the orientation of fibers within plays an essential role in the formations and orientations of bonds between the fibers as well as at the fibers- polymer matrix interfaces and, subsequently, affecting the overall chemical and mechanical durability of the composite. With suitable compositions and orientation of fibers utilizing custom desired properties and functional characteristics of composites equal to steel and higher stiffness than aluminium [231]–[234].

As noted before, with thermal cycling, polymers start exhibiting a rapid degradation in mechanical properties, as reduced elastic modulus in high stresses regions lead to micro damages and increased crack propagation in the polymer matrix. On the other hand, fiber reinforced polymers have lower elastic modulus reduction, compared to polymers with no integrated reinforced materials, as applied strain effects are mitigated due to the added fibers, as the presence of elastic fibers can slow the stress relaxation rate of polymers in which they are embedded. Following past results, and since the degradation results are mostly due to the polymer viscoelastic properties, composite encapsulant material options needed to be investigated.

In addition to the mechanical advantages that composites provide to maintain the durability of the module, the integration of fibers mitigates the thermal effects within the module on the viscoelasticity of the encapsulant materials as well as the performance of the cell. The various thermal effects include the effects due to the module operations such as the heating up of the cells and interconnections or external effects such as accelerated thermal cycles or environmental ambient conditions. The integration of fibers within the polymer matrix significantly reduces the CTE within the module, thus, providing them with better resilience against environmental damage. In the case of polypropylene for example, impregnating glass fiber-reinforcement reduces the CTE of the resulting composite by around 50% to 70%, in other polymers such as polyester for example, the CTE reduction is more significant and reduces the value in the composite to around 20% of its value in where no reinforcement fibers are added [196], [202].

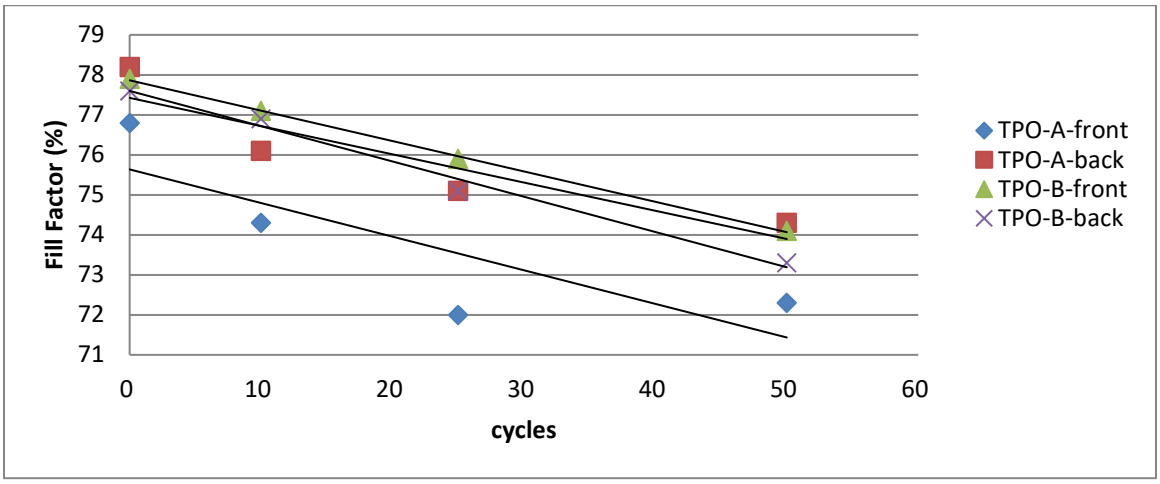

Figure 6-47. Fill factor of modules with weaves as a function of thermal cycles. Adding the thermal weave produced less performance degradation over thermal cycles, indicating that the weave helped maintain polymer uniformity despite temperature fluctuations.

Initially, a weave made of aligned glass-fiber covered with black EVA was attempted. The weave is not the most ideal layer to be added within the module for several

reasons, including that the thickness of the aligned fibers embedded with EVA make it really difficult for the layer to get effectively embedded into the polymer foil as well as efficiently transmit light through the weave layer. In addition, the weave dimensions are limited to sizes below the cell dimensions, thus, limiting the mechanical advantages of adding the weave, compared to having the weave covering the whole module area. None the less, the results obtained were very promising.

In the module layout, the weave is stitched in between the polymer foil and the interconnection wires. When the weave is stitched in this manner, the weave pushes against the wires onto the cell. During lamination, the weave then provides a more uniform pressure onto the wires, as the internal stress effects due to the deformations within the polymer are mitigated by the added weave, thus, providing a better overall contact between the wires and fingers throughout the cell.

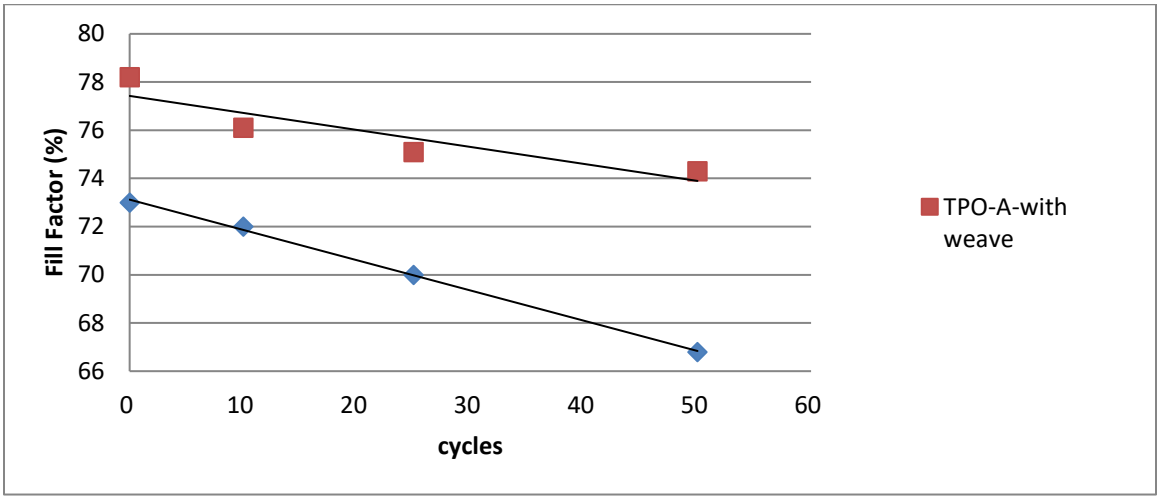

Figure 6-48. Comparative study demonstrating the differences in fill factor when the weave was integrated with TPO-A during the lamination process under identical conditions. Adding the weave, significantly reduces performance loss.

Under identical lamination parameters, the enhancements in the electrical performance of the module are quickly realized as degradation in the fill factor are at -5.86% after 50 thermal cycles, compared to -10.44% in the absence of reinforcement fibers. Following the results, custom composite material were used in the setup, where TPO-A is reinforced by randomly oriented fibers.

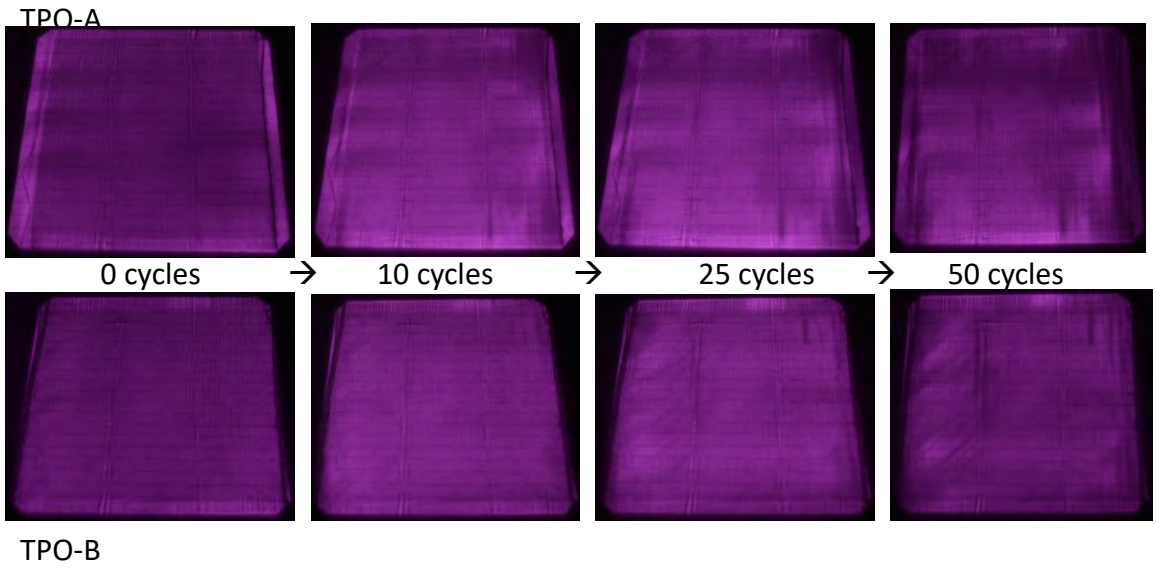

Figure 6-49. EL images of TPO-A and TPO-B with an embedded weave as a function of thermal cycles. Images show reduced viscoelastic creeping effects compared to modules without a weave.

The integration of fibers within the polymer matrix causes the interfacial shear stress transfer at the fiber-matrix interface without causing structural changes at the interface, thus slowing the stress relaxation of viscoelastic polymers and allowing the polymers to retain internal stresses for longer periods of time. The subsequent effect is reduced creeping effect within the composite, equation (6.7). The results have been demonstrated experimentally and in finite element analysis simulations for aligned and randomly oriented fibers. For composites with transversely oriented short and elastic glass fibers, the creep modulus is more polymer matrix dependent, thus, the effect of

temperature on creep behaviour is more significant in the transverse direction, compared with the longitudinal direction. Therefore, custom composites with emphasized creep resistance can be custom made and compared to randomly oriented fibers within composites. However, the mathematical complexities of the formulating non-linear models corresponding to the material properties makes it challenging to simulate accurate predictions of viscoelasticity patterns. In addition, for industrial applications, where cost-effective solutions predominate, seem to favour randomly orientated fibers, which have reduced material costs and are less sophisticated than impregnating aligned fibers within composites [202], [223]–[225], [231], [234]–[236].

Following the past results, a custom composite material was prepared using TPO-A as the base polymer material and impregnating randomly oriented fibers to form a composite, composite TPO-A (cTPO-A). Just as TPO-A is used in the module layout, interconnection wires are stitched into the cTPO-A layer in a specific pattern, based on optimization and stitch patterns discussed by Ibrahim and Tom in their thesis.

Figure 9-50. Optical image of custom composite TPO-A.

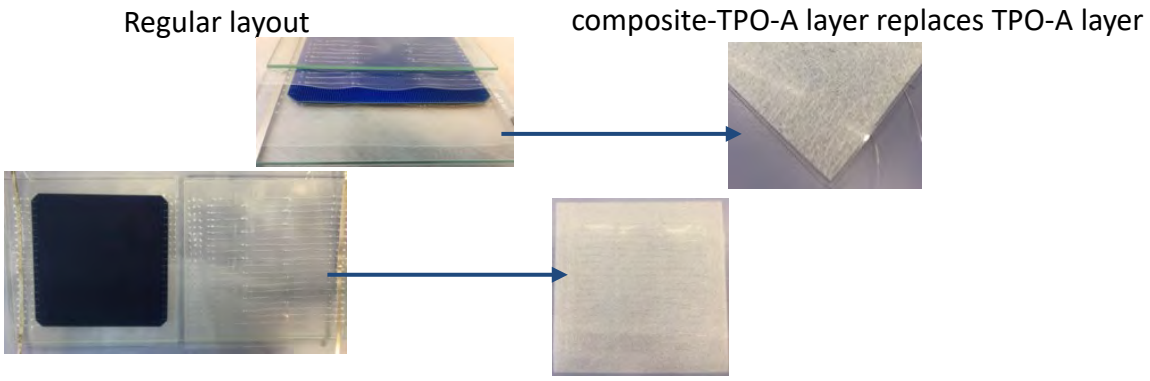

Figure 6-51. The same module layout is used where the TPO-A layer is replaced with the composite TPO-A layer.

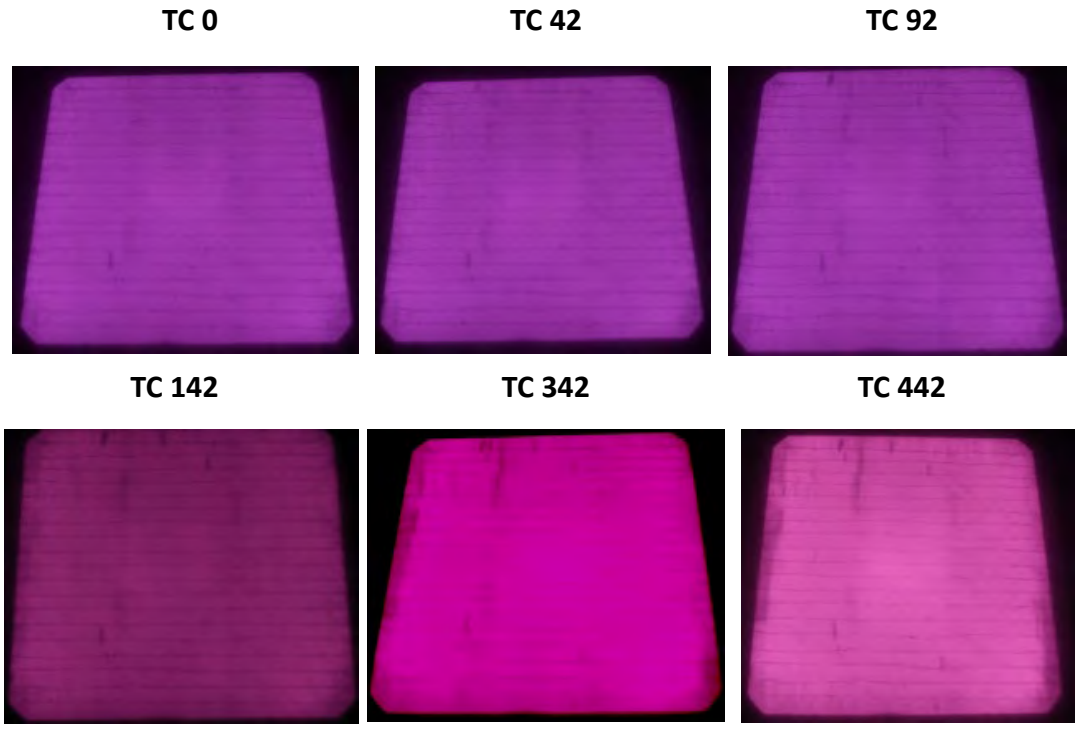

Figure 6-52. EL images of the module with cTPO-A as a function of thermal cycling. Viscoelastic creeping effects start to become more apparent in the module on the edges of the cells after 342 and 442 thermal cycles.

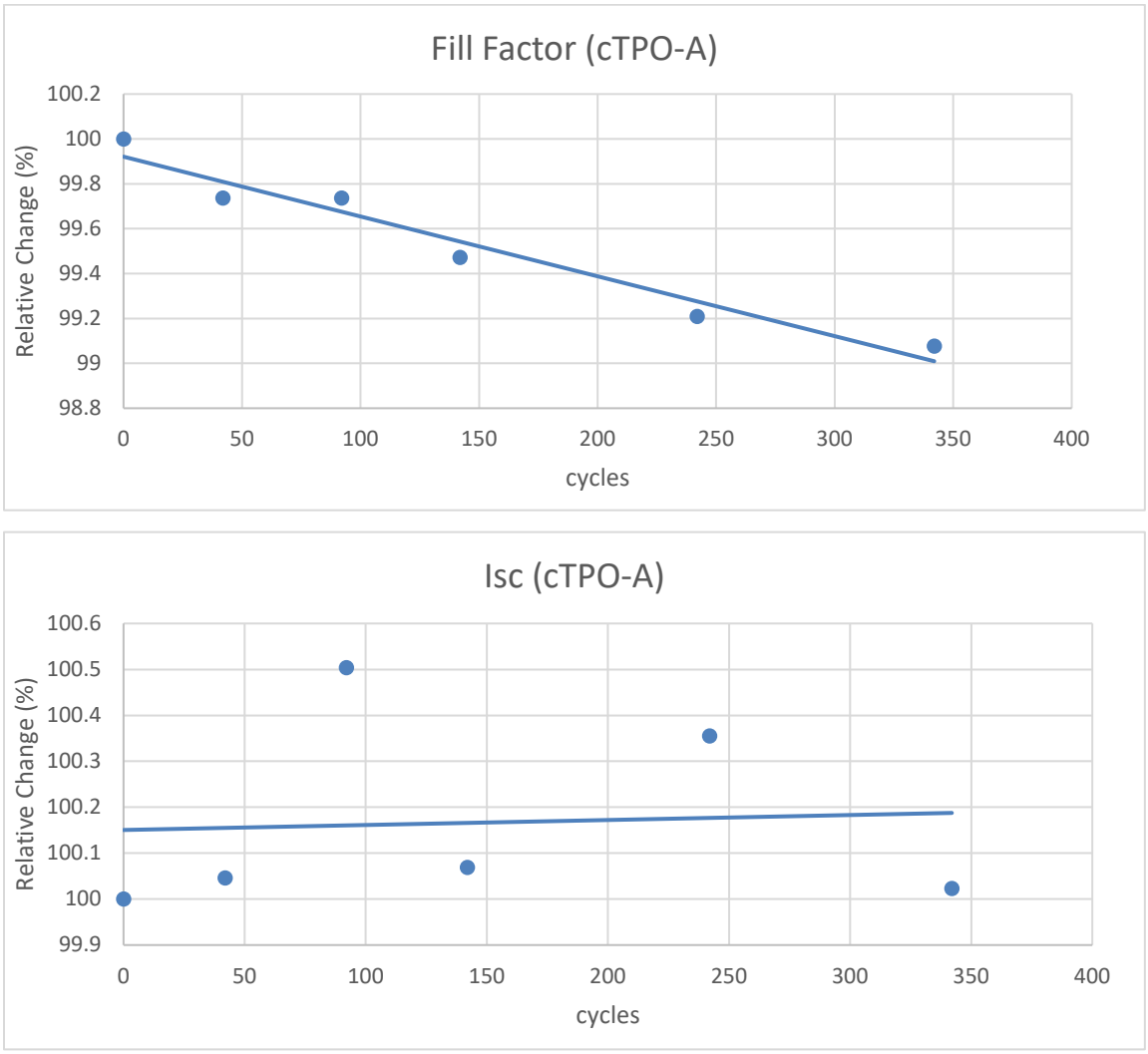

Figure 6-53. Relative change in fill factor and Isc in the modules with cTPO-A as a function of thermal cycling. Fill factor degradation is less than 1% after 342 cycles and the Isc change is within less than 0.5% change.

The results in Figure 6-53 are consistent with the theoretical discussions mentioned earlier, as composites with reinforced fiber provide reduced viscoelastic creeping effects, and reduced chances of deformations within the composite. In addition, the mechanical sturdiness of the composite maintains the wires from moving in the module, thus reducing the probability of loosening connections. Figure 6-54 shows the differences between in fill factor and Isc degradation between the samples prepared with

TPO-A and cTPO-A. In the sample shown in Figure 6-54, the fill factor degradation after 442 thermal cycles is -0.92% and -0.14% for the front and backsides of the module respectively, and the changes in Isc are 0.02% and -0.28% for the front and backsides of the module respectively. The degradation in fill factor in multiple cTPO-A samples is -2.64% ± 1.73% after 300 cycles, figure 6-55, which well below the accepted value of 5% degradation in fill factor after 200 cycles.

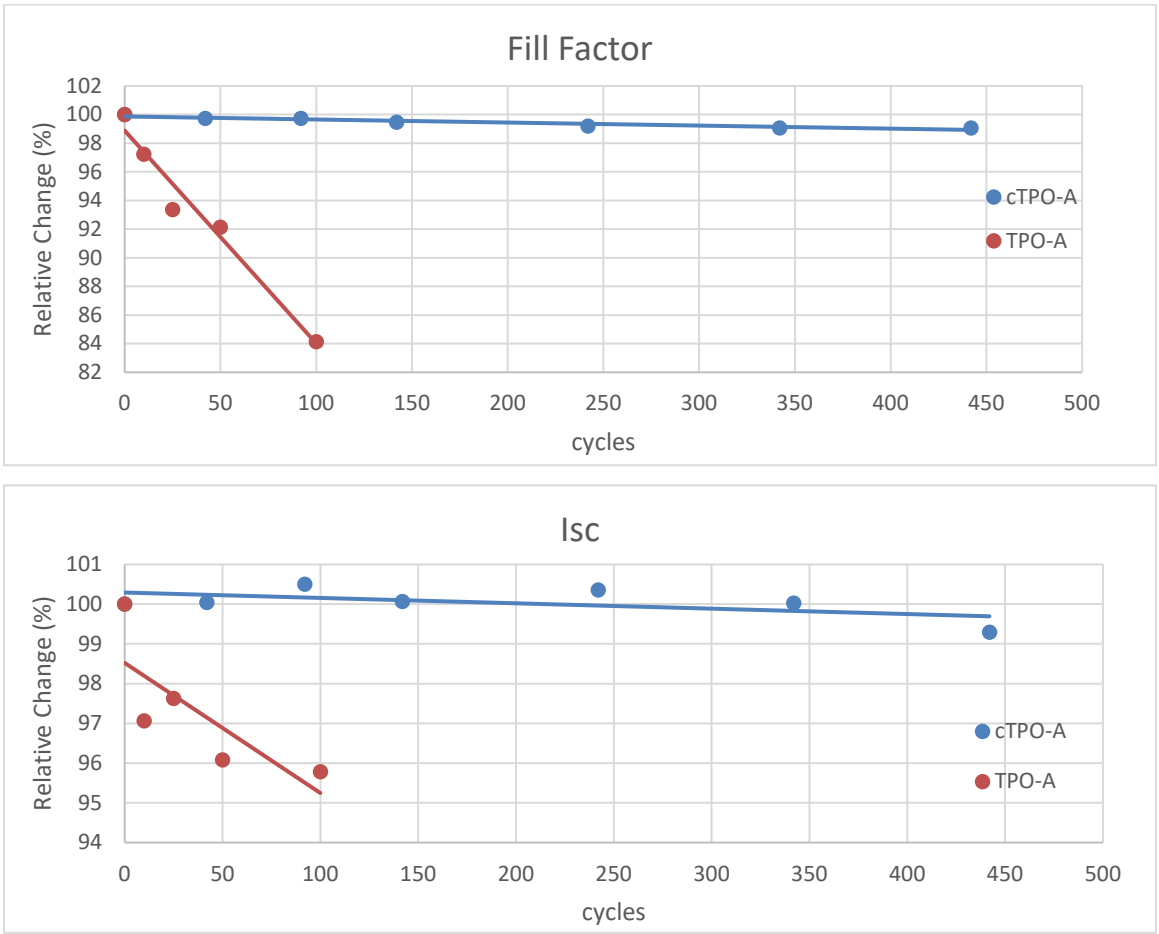

Figure 6-54. Relative fill factor and Isc degradation in cTPO-A and TPO-A samples as a function of thermal cycling. Adding the fiber layer significantly reduces degradation within the cell, reflecting a better overall performance and modular integrity over thermal cycles.

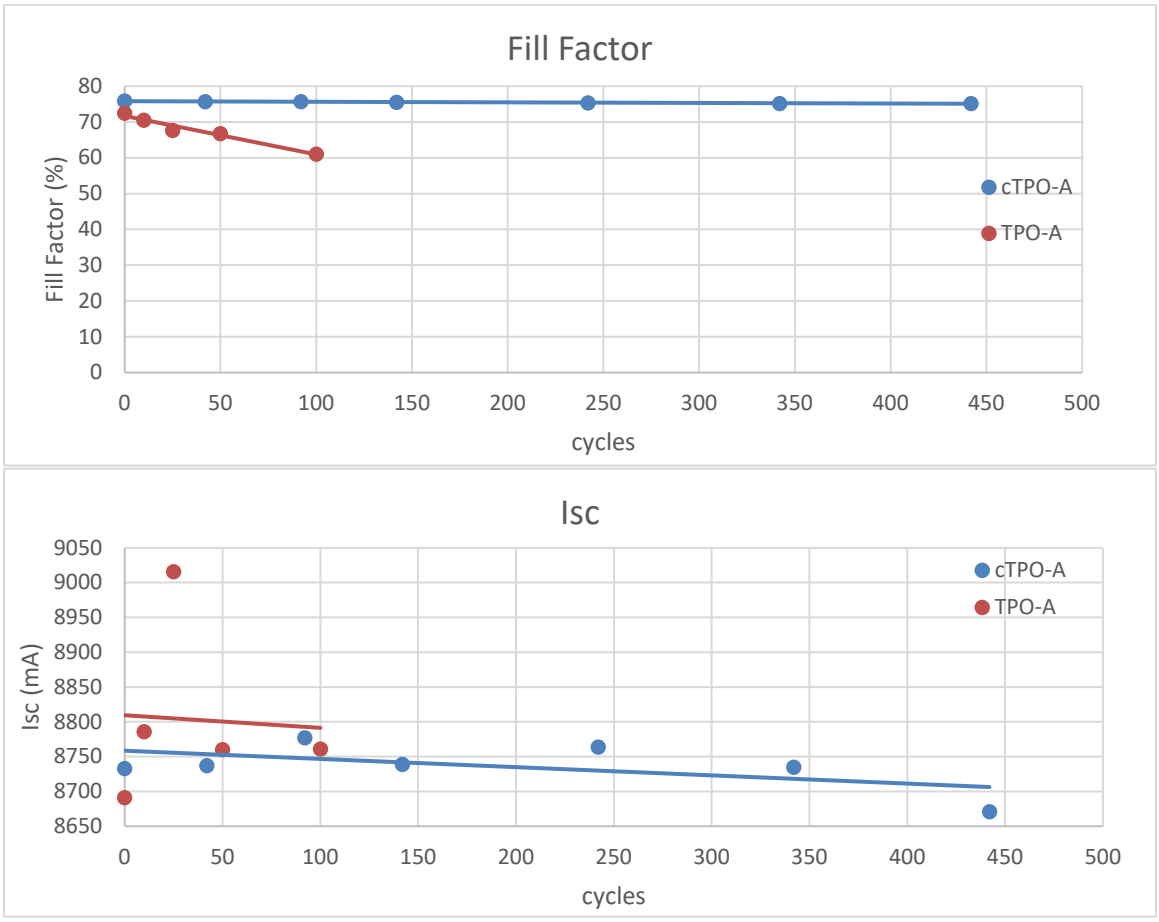

Figure 6-55 . Fill factor and Isc degradation in cTPO-A and TPO-A samples as a function of thermal cycling. Changes in Isc for TPO-A appear to be more random than c-TPO-A, indicating a better modular integrity for the cTPO-A modules.

In conclusion, following previous validations of the novel multi-wire interconnections in bifacial silicon PV solar applications based on traditional stitching, or using transparent contact foils with integrated wires, process optimization were developed to start transitioning the process from the research level stage into an industrial process scaled for the commercial development of bifacial silicon PV solar in various modules and panels applications and integrations.

The optimization mentioned, including utilizing custom materials, allow for excellent electrical and thermomechanical reliability of modules to withstand extreme

environmental conditions. However, the necessary optimization will interfere with the performance of optical sensors' integration within a PV solar module. Polymer composites with embedded optical fibers cause additional internal reflections and refractions misrepresenting original positions or angles of incident light sources. On the other hand, by integrating sensors and real-time monitoring within modules, more advanced outlooks into module performance is realized, as well as proving the potential to include several types of sensors within the module for IoT applications as well as smart grid integrations.

7. Conclusion and Future Work

In this thesis, new designs of 3D vector optical sensors for the use in angular proximity detection applications were demonstrated. Using a macroscale prototype, the theoretical operating principle aspects of a single pixel and two pixel systems were investigated and validated. In addition, the author has developed a microfabrication process in silicon to fabricate a readout compatible mesa pyramid pixel as well as the fabrication of a CMOS compatible inverse pyramid pixel design featuring embedded photodiodes, as p-n junctions are created on pyramids' facets.

The process is optimized so that mesa and inverse pixel designs were fabricated on the same silicon substrate. Difficulties during the fabrication process and alternative processes were discussed and employed. Experimental verification of the principles of operation, characterization, and performance validation of mesa micro-sized vector light pixels were discussed. The advantage of these 3D design over planar ones include that a one pixel system allows for angular estimations and provides spatial proximity of incident light in 2D. Estimation methods using optimized equations for one pixel and two pixels systems were utilized for 2D and 3D angular estimations and spatial positioning, as well as provide the basis for estimations for larger array systems. However, further research and studies including error analysis and signal processing for one pixel, two pixel, and array systems are still required. A CMOS fabrication process needs to be realized and developed for standard foundry processes. The current designs limit detection to the angle ranges discussed in chapters 2 and 4. While increasing the array size reduces the detection limits on each pixel, thus, the array, the design was originally intended to reduce

computational requirements. Designs in Si with more facets, such as hexagon designs, or designs in other materials allowing more flexibility in fabricating facets at more inclined angles (more than Si's 54.7°) may be an interesting case study. Such designs may allow a better compromise than current designs for an overall less number of pixels per array and/or computational requirements.

In addition, carbon nanoparticles-based thin films and composite were studied for their thermoresistive responses. The appeal in utilizing low cost deposition processes for the deposition of thin films at room temperature is for the easier integration of such films with the optical sensors mentioned for various detection and other applications beyond the response regions of Si sensors. VOx thin films were later realized to be more suitable for integrations into 3D optical sensors, mostly due to their higher TCR responses and the use of a cost-effective deposition method. Such integrations are essential in augmented and virtual sensing application as well as autonomous applications, due to their reduced power and computational requirements.

One potential practical application for the 3D optical sensors is their utilization as solar trackers within PV solar panels. Such sensors would orient the panel towards the sun based on relative light intensity. Embedding sensors within modules requires validations and optimization for an effective powering and connecting the embedded sensors within. The novel multi-wire interconnections technology was studied, and optimization and validations in materials and layouts were discussed. Embedding temperature sensors within solar modules for real-time monitoring during the fabrication process demonstrated the potential of embedding sensors for real-time monitoring applications, especially essential in remote monitoring applications. On the other hand,

due to the materials optimization and the use of composites containing optical fibers, embedding optical sensors within solar cells proves to be counter intuitive.

The integration of sensors within solar modules and panels for IoT applications and smart systems is within its first stages, and numerous optimization and integrations are on-going before the full integration of sensors within modules, especially with constant advancements in IoT connectivity.

On the module side, there could be a number of optimization on the materials side, including simulations into the use of different types of fibers within composites as well as other transient thermal measurements with finite element simulations. Custom thermomechanical and electrical properties for modules should be studies to achieve the right compilation of utilizing various encapsulant materials, novel materials and technologies, and interconnection schemes, alongside with different embedding methods, for further customized integration of solar and modules in applications, including cars and buildings.

Additional tests to further validate the custom integration of composite c-TPO-A include thermal tests with humidity variations, as well as PID testing. In addition, cross-sections of samples to be used for SEM images were prepared, however, SEM images were to not be released yet. Additional tests to study internal reflections due to fiber integration within composites, such as fiber glass, would provide a better insight into additional possible advantages of further utilizing customized composites into solar applications.

Technology optimization in sensing technology and renewable energy integrations are essential in bridging the gap between much-needed wide-scale utilization of clean

energy alternatives and the necessary infrastructures required for development and feasible implementations. In this approach, we've experienced various challenges in several aspects of such complex integration, leading to easier, feasible integration as well as an interesting set of future challenges for student researchers and collaborative projects.

Appendix A. Solar Tracker Design and Initial Tests/ IoT in Smart Energy System

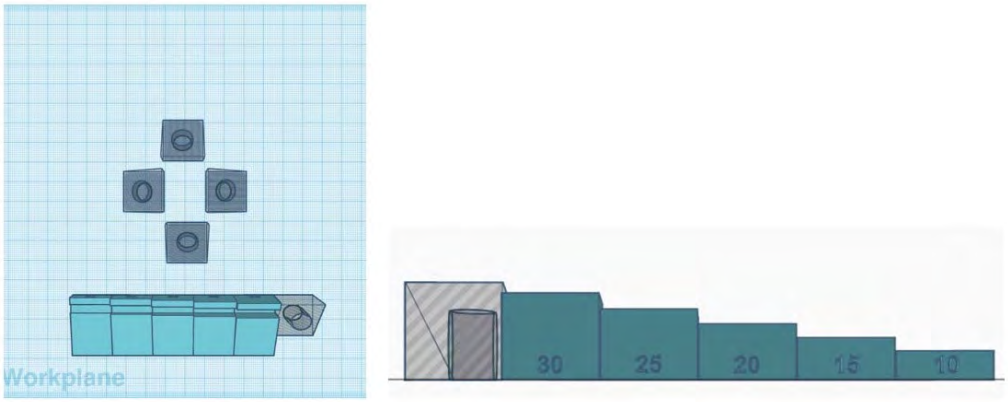

Figure. Solar tracker module placed on PV solar panel. Thingverse-thing:2415083 was not printed as a part of the setup. Custom modified angled setups, angles 10°- 30°, were printed and used in the solar tracker module.

In an attempt to demonstrate the integration of an external, macroscale size, solar tracking system capable of relaying module performance in real-time, my colleagues at EnergVille and I designed a 3D printable system that can be integrated into a solar PV module. The goal of the project was to compare power generation in fixed modules with PV module that rotates along with the sun. The results were going to be compared with a similar setup where Perovskite solar thin films replace the c-Si in the module, and the two modules would be compared in real-time as energy generated is monitored in real time as well. We built a part of the system, where some of it were used in the AI for Earth project, but we didn't get a chance to finish the whole setup.

Appendix B. Microsoft AI for Earth Portfolio and Summary of Project

AI for Earth Grantee Profile
Ibrahim Elchami- Lead Researcher
Agricultural Hubs in Smart Cities

Summary:

Canadian and European cities are increasingly adopting the Internet of Things (IoT) and AI integration into city components and smart system grids. Combining the expertise and efforts of renewable energy, agritech, and AI researchers, we're studying the rapid development of hardware-AI integration solutions in agriculture, along with the wider-scale implementable transition towards renewable energy generation and optimization systems.

Such solutions are urgently needed to address major global challenges within the next few decades, including food sustainability and security, environmental migrations, and an inevitable global transition towards renewable energy power systems. Adopting multidisciplinary, IoT and Edge AI integrations will pave the way towards creating portable, autonomous and energy efficient agricultural hubs in smart cities, effectively provisioning active solutions for a number of global challenges.

Sensors, forecasting, and AI

The inability of current agricultural forms to produce sufficient yields to accommodate the substantial growth in population, has further advanced the recent technological implementations of Internet of Things devices (IoT) and Artificial Intelligence (AI) in agriculture, introducing new integrations in the world of Smart Farming and Agritech applications [D1,D2]. In addition, significant socioeconomic migrations have pushed

younger farmers away from farmlands, where the average farm sizes are in continuous decline.

Furthermore, according to the latest Statistics Canada report [D3], 2018 registered the most significant decrease in net farm incomes in Canada at 45.1%, the largest percentage decrease since 2006, the year records started. This followed a 2.8% decline in 2017. The loss in income is mainly attributed to rising operational costs and relatively flat revenues from the sale of agricultural crops and livestock, amidst changes in mandated regulations to limit carbon and nitrogen oxide based emissions in agriculture [D4,D5].

Continuous monitoring of nutrients' concentrations in agricultural soil is vital in optimizing crop yield and quality, and it has been encouraged by the Ministry of Agriculture and Agri-food in Canada. Periodic soil management has been effective at minimizing nutrient input costs as well as providing avenues for farmers to efficiently utilize available soil and water resources [D6,D7,D8]. Stats Canada has also provided historical data on soil nutrients' significance and usages in Canada [D9].

Nitrate, Phosphorus, and potassium (NPK) represent vital nutrient information for agricultural soil. Technological integration in NPK measurements has been limited, where the majority of current periodic soil management methods heavily rely on manual, discrete soil sampling, where the process is relatively expensive, especially in larger fields [6,9]. More importantly, the process usually takes 3-6 weeks, rendering the monitoring methods less effective, if effective at all, since farmers are receiving information on their soil health 3-6weeks too late, when the window to make changes to maintain crop quality and quantity would have already passed.

In utilizing new technologies, agricultural data can be captured and analysed to provide farmers with the sufficient reporting and decision-making tools, within actionable time-frames, including predicting future harvest yields [D10]. Sensing devices are used for continuous monitoring of resources in IoT systems, thus, allowing farmers to produce higher quantities of plants monitored and grown to data-enhanced qualities, all while significantly maximizing data-driven decisions. Utilizing resources efficiently further reduces operational costs as well as the burden on natural resources, effectively reducing over-nitrification during and post-harvest stages, as well as subsequent associated emissions [D11, D12].

With the advancements in agriculture, data analytics in Smart Farming and Agritech introduces an insight into farms' demands on connected city infrastructure such as water systems and active reductions in emissions, as well as a wider and easier implementation of renewable energy in agriculture.

What we're working on: Agriculture

One aspect of our project included talking with farmers across North America, Belgium, The Netherlands, Turkey, and Australia to understand current challenges in obtaining and integrating the necessary hardware and software implementations in indoor and outdoor farms.

In Canada, we're currently working on developing custom sensors for accurate soil nutrients concentrations, including NPK. The sensing devices also include sensors to measure soil water content, temperatures, and pH levels, as well as air quality and gas sensors to collect data on Carbon and Nitrogen oxide concentrations in farms. Initially, batteryless nodes were the goal, completely running off regenerative sources such as soil

and solar. However, due to vast variations in weather and soil patterns, we've opted to use hybrid sources for power sensing devices, such as battery and solar, where the devices connect to a weather API to utilize forecasted weather data and optimize power usages accordingly. That is, the system would run on solar power, when available, and run on solar-rechargeable batteries otherwise.

In Belgium, we're working on a portable agricultural box, with sensors similar to the ones used in outdoor farming. After building two prototypes, some community leaders in Brussels granted us access to an underground space to convert into an agricultural hub. The idea is for the system to eventually run partially or fully-autonomously, after rigorous data collection as well as sufficient model and integration optimization.

We've opted to develop a system to start collecting the data in specific patterns, in order to minimize feature engineering and an eventual easier integration into machine learning models, to be used to predict harvest yields, as well as plants' health monitoring during the season.

We've also started testing building some disease detection models to understand, and more accurately digitize, correlations among pesticides' usages in farming. We're aiming to gear the research towards an eventual, hopefully significant, reduction in pesticides' usages as well as associated emissions, without sacrificing plants' quality or overall yields.

In this approach, we're using Edge AI, where a custom disease detection and classification model is running on an MCU with a camera module. We've trained a simple model to detect diseases on basil plants leaves based on input images. However, in training the model, more data including the percentage of disease in a plant leaf needed

to be taken into account, the leaf coloration, and detect the leaf dimensions. The combination provides a better insight into the plants' overall health.

Indoors, MCUs are integrated as a part of the system. Outdoors, the MCU are attached to a drone, depending on farms' sizes. However, the overall feasibility of the outdoor integrations are challenging, Edge AI is perfect for such an application. Images acquired get classified on the MCU before being transferred into storage.

Smart Sustainable Cities: Energy

Historically, managing traditional urban developments and associated challenges has been mostly limited to cities' unique and infrastructural systems operating with limited data-driven decisions, as well as the common lack of sufficient information sharing between systems. As a part of a student-led initiative to introduce IoT and AI into public spaces and facilities, which included starting our Canada's first smart public parks research project, several cities in Canada and the EU were engaged to start research projects focused on the effective collection of data and its utilization in city applications aspects, such as monitoring facilities' usages and maintenances as well as predictive analysis for energy systems. City managers were transparent about making expensive, wide-scale city projects with very limited data, and sometimes, intuition-led decisions in the past, and some cities were eager to engage in research.

The continuous demand for innovative solutions has prompted cities to start integrating technological advancements into the cities' core infrastructures as well as public spaces and services systems to improve the overall quality of life for citizens. The solutions are aimed towards addressing the various social and socio-economic challenges, more rampant within larger cities. In addition, smart city research initiatives

and projects in the EU and North America are being increasingly implemented. Some examples include Antwerp's City of Things and Smart City research at IMEC in the EU and the US. The integrations have enhanced existing services and provided additional research avenues for virtual and transformational infrastructure systems including energy, water, sewage, and transport, offering substantially versatile capacity to simulate and propose data-driven solutions to address sustainability, environmental, and human-capacity issues, in addition to the unique urban challenges. Even in its earliest stages, the Digital Twin of the city of Antwerp project has presented significant insight into the vast potential of such integrations.

In some smart city systems, sector digitization and paths are set towards fully-sustainable transitions. Some examples include Metro Vancouver's multimodal transportation authorities' integration with Azure and the City's path towards a system-wide transition to a smart water grid. On the other hand, energy and power systems and the transition towards sustainable alternatives has proven quite complex. The main current setbacks are related to the high penetration of renewable energy sources, such as wind and photovoltaic solar, into the power system. Specifically, the intermittent power output of systems, due to inconsistent supply of wind and sun for example, poses different challenges on the planning, operation, and control of the power system networks. The research focus of Smart Grids, primarily describing the electricity sector, has been regarding ICT, smart meters, electricity storage technologies, and local (electric) smart grids, most of which are stand-alone and hybrid-systems, not intended for wide-scale implementation, not to mention inter-sector integrations [D13, D14, D15, D16].

The rapid rise in integrations of ultra-low power/low cost sensing devices, wide-scale implementations of real-time IoT systems, and data analytics has provided an

avenue to address intermittent power output challenges, as well as potentially allow for the feasible implementation of a 100% renewable energy system in Europe, without consuming an unsustainable amount of bioenergy. A main feature that needs to be embedded are the various IoT and AI technologies into a platform, i.e. intermittency forecasts due to expected weather fluctuations, integrated analysis for energy (generation, storage, and consumption) forecasting, and a connected network of sensor nodes providing real-time insight and communication between the different aspects of energy generation, storage, and consumption systems.

The advantage in such an intricate system is in the transferability of its stand-alone components into other sectors, allowing for quasi-seamless integrability within other systems' aspects.

What we're working on: Energy

The smart photovoltaic (PV) grid is a network connecting a number of solar PV modules together. Energy harvesting and performance data from individual modules are communicated among the network, as modules act as nodes within the network. Thn, the data gets uploaded onto a shared platform, where researchers and users can remotely monitor performance levels of connected modules. We're connecting individual panels consisting of some solar PV modules to MCUs to collect performance data on each panel. Nodes communicate panel performance data as well as other parameters, such as temperature, from individual panels through a gateway.

In a further validation step, real-time data was acquired from an online weather report station and correlated weather data with the collected performance data from PV modules, in order to optimize the energy efficiency output of the PV system. If the weather

forecast indicates intermittent sunny weather, the microcontroller sends a message that the energy output should be optimized to increase efficiency of the available energy. The message is then relayed by decreasing the energy consumption, in this case sending a few devices to power savings modes.

As a part of future integrations into smart city systems, we're aiming to connect the system with the agritech systems mentioned, where the system connects to the smart city infrastructure, and potentially a city's digital twin. We're still working on optimization and integration feasibilities, before integration into agriculture.

In another approach, we're aiming towards standardizing the collection of energy data among institutions. Through the approach, substantially is aimed to reduce countless hours spent on feature engineering, potentially building an open-source database for all energy-related data.

Connected Systems in Smart Sustainable Cities: Population and Climate change

The global urban population is expected to grow by around 63% by 2050, with an overall global anticipation population growth of 30%. The anticipated growth of cities creates unprecedented sustainability challenges, associated with increasing demands for public services [D17, D18]. In addition, climate change effects are starting to become more noticeable in the last few years, as parts of the world are unprecedentedly frequented with record hot and cold weathers, followed by record high fluctuations, floodings, hurricanes, and other natural disasters. Farmers' yields are in constant jeopardy, with inconsistently changing challenges. The unpredictability of harvest yields is a vital parameter to the food security equation, as well as subsequent economics equation, as shortages of food will also yield unpredictability in markets.

In addition, climate change, along with other factors in the unpredictability of seasons, is not only heavily affecting wildlife, as the list of affected species grows by the day. With increasingly rampant weather fluctuations and extreme conditions, environmental immigration are becoming more common, as severe natural disasters are forcing people to leave their home regions, sometimes abruptly. The World Bank estimates that Latin America, sub-Saharan Africa, and Southeast Asia will generate 143 million more climate migrants by 2050. Such migrations will exacerbate humanitarian and food security crises.

Moving forward:

Developing autonomous, energy efficient agricultural hubs in smart cities may showcase the collaborative cutting-edge research approaches into several fields. However, the goal is not to showcase projects, rather, it’s to potentially develop and lead by example. The rapid development and implementation of feasible solutions in agriculture as well as early full-integration of renewable energy generation and optimization are urgently needed. The integrations of such solutions with currently stand-alone smart city aspects would help us address unprecedented population growth, changes in ecosystems, and sustainability challenges.

Resources, updates, and further readings:

City of Things, Smart City research, Digital Twin of the city of Antwerp Energyville: Research on sustainable energy and intelligent energy systems. Periodically updated progress on some aspects of projects: Ibrahim's page , Community and hub progresses in Brussels Informedin.

Special thanks to the collaborators Dr. Hans Goverde, Prof. Johan Loeckx and the Artificial Intelligence Lab Brussels, VUB, Prof. Amin Milani Fard, Prof. Hasan Cavusoglu, e@UBC, and the labs and researchers involved with sensor research at UBC, Julie Foulon, Girleek , and MolenGeek , as well as the many undergrad, grad, and coop students.Thank you to the Microsoft's AI for Earth team as well as Microsoft personnel who were more than happy to engage and provide mentorship and support along the way, Hubert Duan and the rest of Canada's National AI Team.

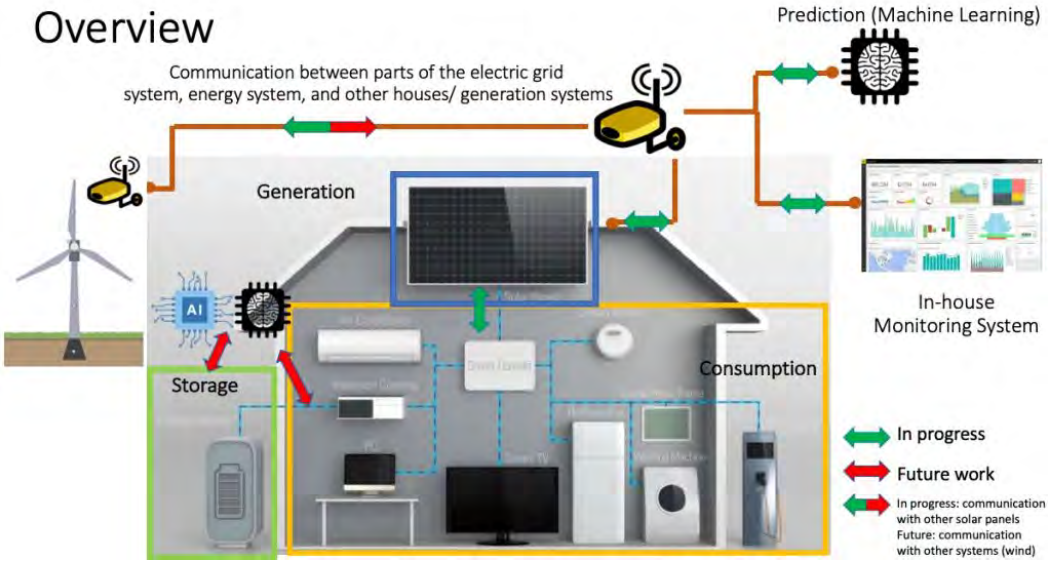

Figure. One aspect of the energy system mentioned in the project summary above.

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Appendix C. Fabrication Details

The following process flow details the fabrication process and parameters used in this thesis.

1- **RCA Cleaning Step**

#	**Process step**	**Process Details**
1-1	RCA SC-1 clean	DI H_2O: 5parts,Ammonium Hydroxide (NH4OH), 30%: 1 part Hydrogen Peroxide (H_2O_2), 50%: 1 part Temperature: 80°C Time: 10mins
1-2	DI water rinse	>3min
1-3	HF dip	DI H2O: 10parts HF, 48%: 1part Room temperature Time: 30 seconds
1-4	DI water rinse	>10min
1-5	RCA SC-2 clean	DI H_2O: 6parts Hydrochloric Acid (HCl), 30%: 1part Hydrogen Peroxide (H_2O_2), 50%:1part Temperature: 80°C Time: 10mins

1-6	DI water rinse	>3min
1-7	Drying wafers	N_2 spin dry then hotplate dry at 120°C for ~3mins

2- **Oxidation/ Create Windows for Si Etch Step**

#	Process step	Details
2-1	Wet Thermal Oxidation	Dry N_2 flow through bubbler: 4 scfh Vapor DI H_2O Temperature: 1100 °C Time: ~55 minutes
2-2	Oxide patterning (Lithography) - Photoresist: Shipley 1813 - Developer: MF-319	Resist spinning: at 3000rpm for 35 seconds Soft bake (hotplate): 1min at 100°C Exposure: 8.3 seconds Develop: 1min at room temperature (slight agitation Hard bake (hotplate): 2mins at 115 °C
2-3	Oxide Etch: Transene Buffered Oxide Etchant	~6m40s- 7min at room temperature (slight agitation)

2-4	Photoresist removal	Photoresist strip in Acetone bath followed by IPA then DI H_2O baths

3- **Anisotropic Si Etch**

#	Process step	Details
3-1	Si Etch (Etch rate varies based on how many times the solution has been used)	TMAH %25 solution + %10 IPA Temperature: 90-95 °C Time: ~18-22 minutes
3-2	Oxide removal: Transene Buffered Oxide Etchant	~6m40s- 7min at room temperature (slight agitation)
3-3	DI water rinse	>3min

4- Oxidation/ Create Windows for Diffusion Step

#	Process step	Details
1-1 – 1-7	**RCA Cleaning Step**	
4-2	Wet Thermal Oxidation	Dry N_2 flow through bubbler: 4 scfh Vapor DI H_2O Temperature: 1100 °C Time: ~55 minutes
4-3	Oxide patterning (Lithography) - Photoresist: Shipley 1813 - Developer: MF-319	Appendix B: Spray Deposition Soft bake (hotplate): 1min at 100°C Exposure: 76 seconds Develop: 1m30s at room temperature (slight agitation Hard bake (hotplate): 2mins at 115 °C
4-4	Oxide Etch: Transene Buffered Oxide Etchant	~6m40s- 7min at room temperature (slight agitation)
4-5	Photoresist removal	Photoresist strip in Acetone bath followed by IPA then DI H_2O baths

5- **Modified RCA Cleaning Step**

#	**Process step**	**Process Details**
5-1	RCA SC-1 clean	DI H_2O: 5parts,Ammonium Hydroxide (NH4OH), 30%: 1part Hydrogen Peroxide (H_2O_2), 50%: 1 part Temperature: 80°C Time: 10mins
5-2	DI water rinse	>3min
5-3	Modified HF dip	DI H2O: 100parts HF, 48%: 1part Time:30s (room temp)
5-4	DI water rinse	>10min
5-5	RCA SC-2 clean	DI H_2O: 6parts, Hydrochloric Acid (HCl), 30%: 1part Hydrogen Peroxide (H_2O_2), 50%:1part Temperature: 80°C Time: 10mins
5-6	DI water rinse	>3min
5-7	Drying wafers	N_2 spin dry then hotplate dry at 120°C for ~3mins

6- Diffusion

#	Process step	Details
6-1	Ramp up	Temperature:800°C Time: 17.5mins at 10°C/min Dry N_2 flow: 4 scfh
6-2	Phosphorous diffusion: Solid source: PDS® products phosphorus n-type source wafer, PH-1000N	Temperature:975°C Time: 30 minutes Dry N_2 flow: 4 scfh
6-3	Ramp down	Temperature:975°C Time: 17.5mins at 10°C/min Dry N_2 flow: 4 scfh
6-4	Oxide removal: Transene Buffered Oxide Etchant	~6m40s- 7min at room temperature (slight agitation)

7- Low Temperature Oxidation/ create contact cuts/vias for metallization step

#	Process step	Details
1-1 – 1-7	**RCA Cleaning Step**	
6-2	Wet Thermal Oxidation	Dry N_2 flow through bubbler: 4 scfh Vapor DI H_2O Temperature: 800 °C Time: ~3hrs 25mins
6-3	Oxide patterning (Lithography) - Photoresist: Shipley 1813 - Developer: MF-319	Appendix B: Spray Deposition Soft bake (hotplate): 1min at 100°C Exposure: 76 seconds Develop: 1m30s at room temperature (slight agitation Hard bake (hotplate): 2mins at 115 °C
6-4	Oxide Etch: Transene Buffered Oxide Etchant	~2m30s- 3min at room temperature (slight agitation)

6-5	Photoresist removal	Photoresist strip in Acetone bath followed by IPA then DI H_2O baths

8- Metallization / Lift-off

#	Process step	Details
5-1 – 5-7	**Modified RCA Cleaning**	
8-1	Oxide patterning (Lithography) - Photoresist: Shipley 1813 - Developer: MF-319	Appendix B: Spray Deposition Soft bake (hotplate): 1min at 100°C Exposure: 76 seconds Develop: 1m30s at room temperature (slight agitation Hard bake (hotplate): 2mins at 115 °C
8-2	Aluminum sputtering	DC plasma sputtering Pressure: 2E-3 mbar (Ar) Voltage/Current/Power: 419V/ 240mA/ 100W Time: 42mins

		Expected deposition rate: 8.1nm/min Thickness: ~340 nm
8-3	Lift-off	Photoresist strip in Acetone bath followed by IPA then DI H_2O baths

Appendix D. Spray Coating (SonoTek) - Shipley S1813- AZ MiR 703 Photoresist SOP

The author prepared the following basic complementary guide to the Spray Coater Standard Operating Procedure (SOP) provided by 4D Labs, portions of this guide previously appeared in the 4D Labs SOP [237]. For more detailed explanations of the parameters used in this section, please refer to section 3.4 “Spray Coating vs Spin Coating to Achieve Uniform Layers of Photoresist.”

In order to deposit Shipley S1813 photoresist using spray coating, several hardware variables and parameters were adjusted to optimize the SonoTek ExactaCoat automated spray coating system. Some of the parameters include the flow rate of solution, chamber shaping air, spray path speed and positioning, as well as sonication power during deposition. All of these parameters are controlled through the Portal software.

Since S1813 solution has low viscosity, there was no need to dilute the solution. The same parameters can be used to deposit AZ MiR 703 photoresist solution without dilutions.

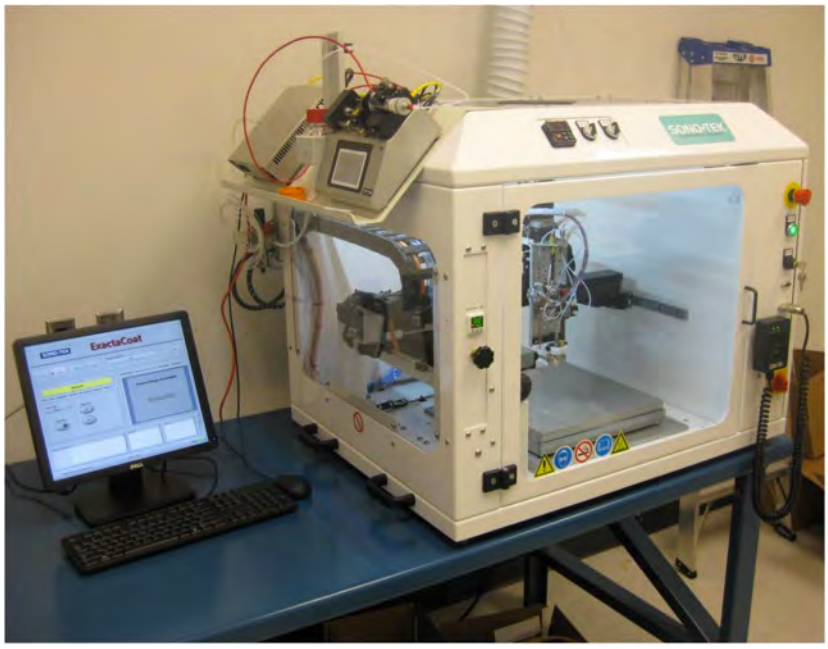

Figure 8-1: SonoTek ExactaCoat Spray Coater automated spray coating system [87].

Operation

1. Startup

• Start Portal software

• Click continue and software will do an auto-system check.

• Ensure that the proper fluid lines are connected such that your fluid will go as follows:

Syringe -> Line 5 (Photoresist line) -> Valve 1 -> Spray nozzle

Sample Loading

• Load the spray solution into the syringe by placing the tube in the solution and withdrawing the syringe.

• Remove the syringe from the pump and remove any air-bubbles from the syringe by positioning the syringe upside-down and dispensing the air back into the stock solution.

• Connect syringe directly to Line 5- photoresist line

• Place syringe in compartment and tighten screw to hold syringe.

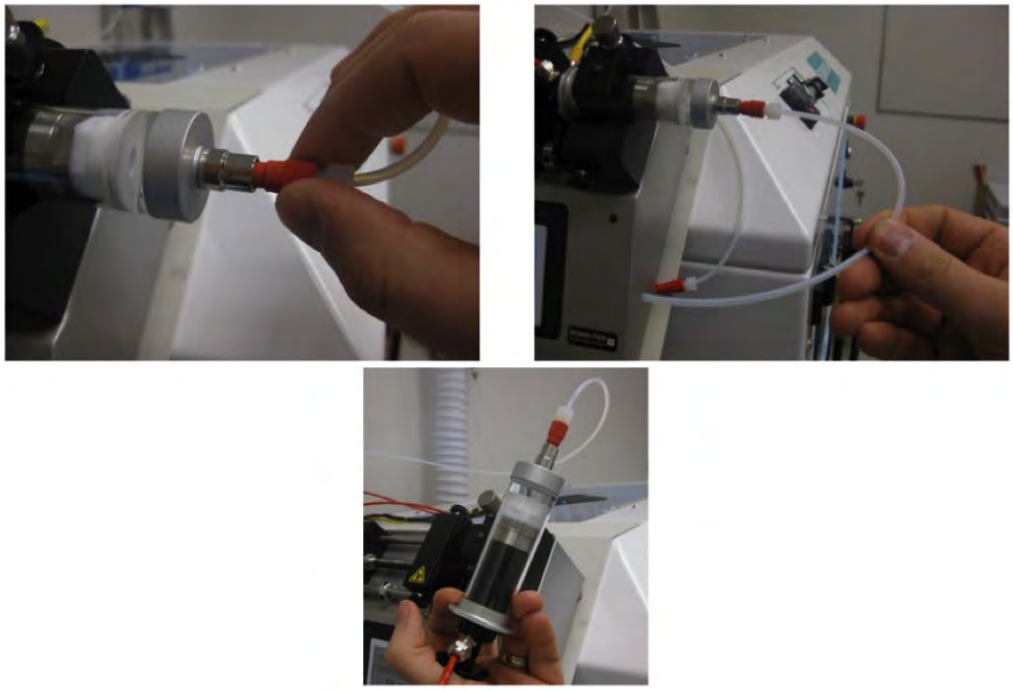

Figure 8-2: Load the spray solution into the syringe, connecting the lines, and making sure that there are no bubbles in the system [87].

Sonication causes bubbles in the photoresist solution as the solution is mixed in the nozzle before deposition. Thus, in order to decreases the chances of island formation in the resist layer as the solution is deposited, sonication should be turned off.

Figure 8-3: The SonicSyringe should be turned off [87].

- Place the substrate on the vacuum/hot plate (using plastic transparency or aluminum foil around the substrate to protect the stage from overspray of the solution).
- Turn on vacuum switch to “On” in order to hold the substrate in its position during deposition. “Zone 1” represents the center area of the plate.

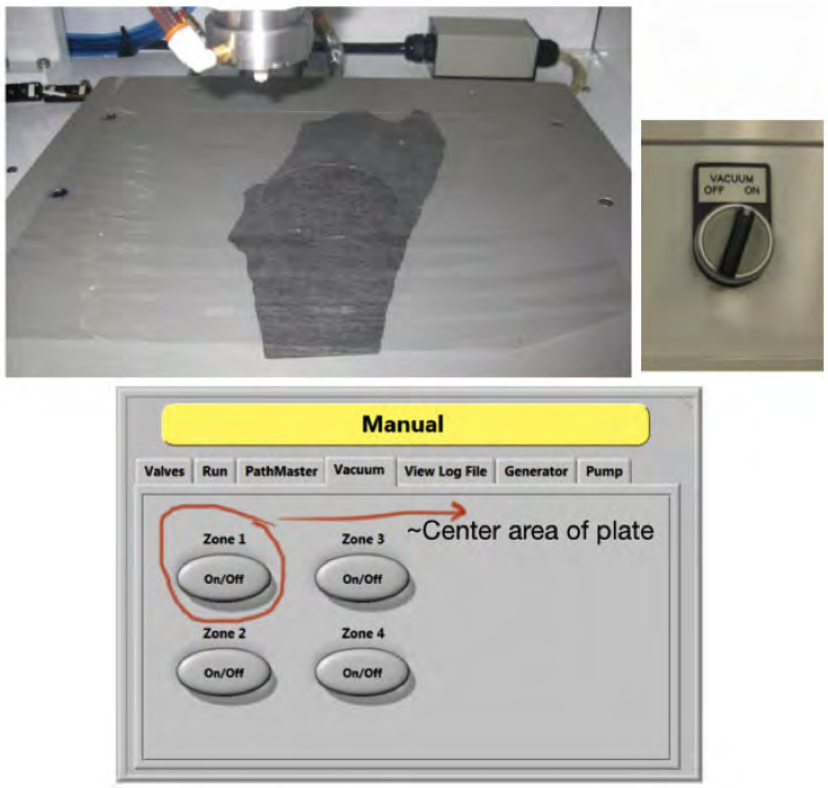

Figure 8-4: The vacuum/hot plate with the vacuum switch and control [87].

Software

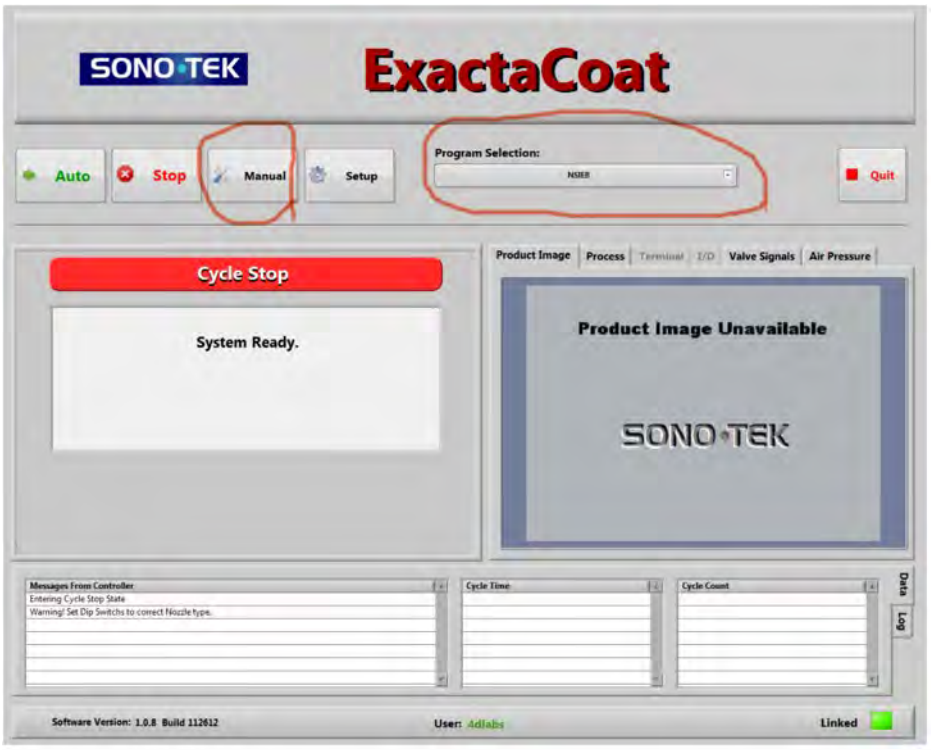

Figure 8-5: ExactaCoat GUI to control the spray coating system [87].

- From “Program Selection” drop down menu select any user to get the program running. We are changing the parameters anyways. Then, press “Manual” button
- In Valves tab: select “Spray 1” from the “select valve” drop list

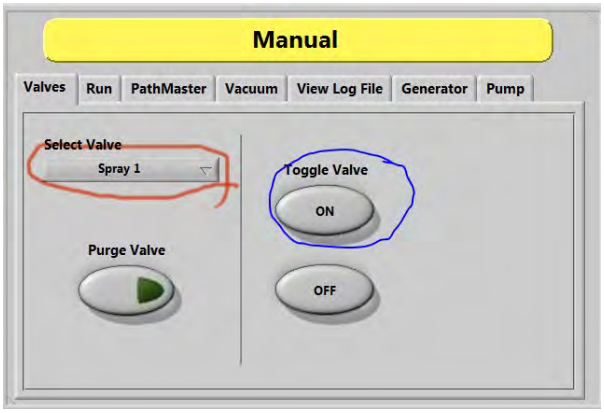

Figure 8-6: Select Spray 1 from the valve drop list.

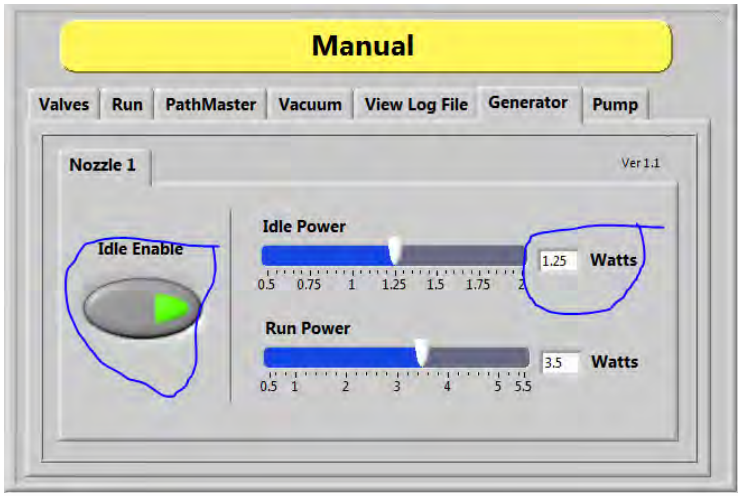

Figure 8-7: Power changes in the Generator tab.

- Select the “Generator Tab”
- Making sure that the Idle power switch is ON, change Idle power to 1.25 Watts, and run power to 3.5 Watts.

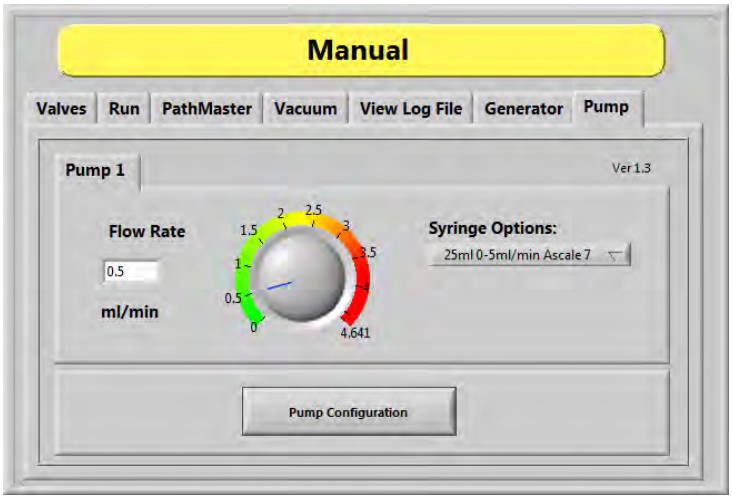

Figure 8-8: Power changes in the Generator tab.

- In the “Pump” tab, change the Flow rate to 0.5 mL/min

Path Programming

- open “path programming” to run custom program
- Select “s1813 photoresist” program from drop down menu

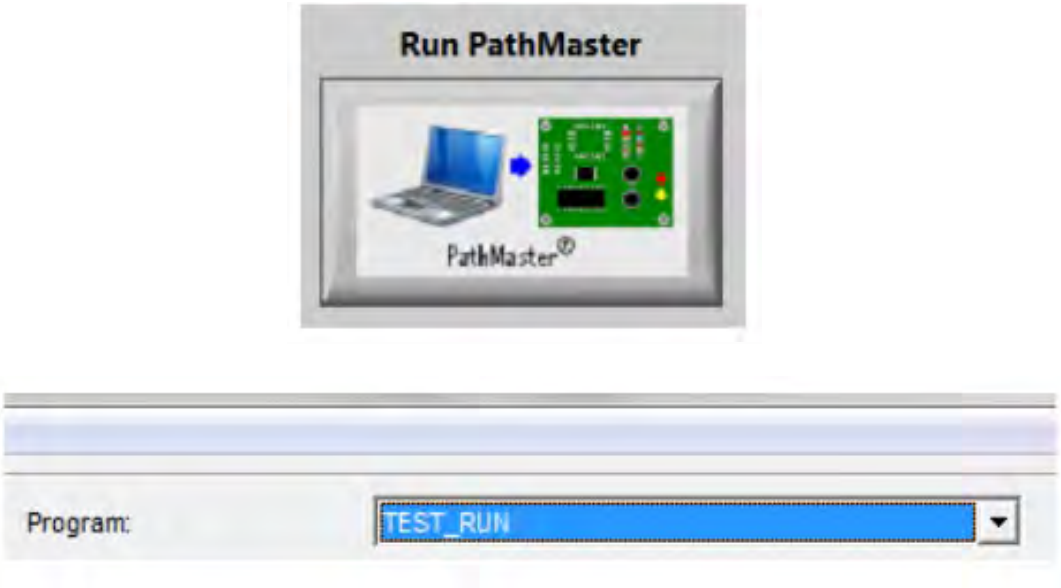

Figure 8-9: Select “s1813 photoresist” program in PathMaster.

“s1813 photoresist” program should include the following functions with Area dimensions to create a rectangular area big enough to spray coat the whole wafer.

100,90,10

100,215,10

215,215,10

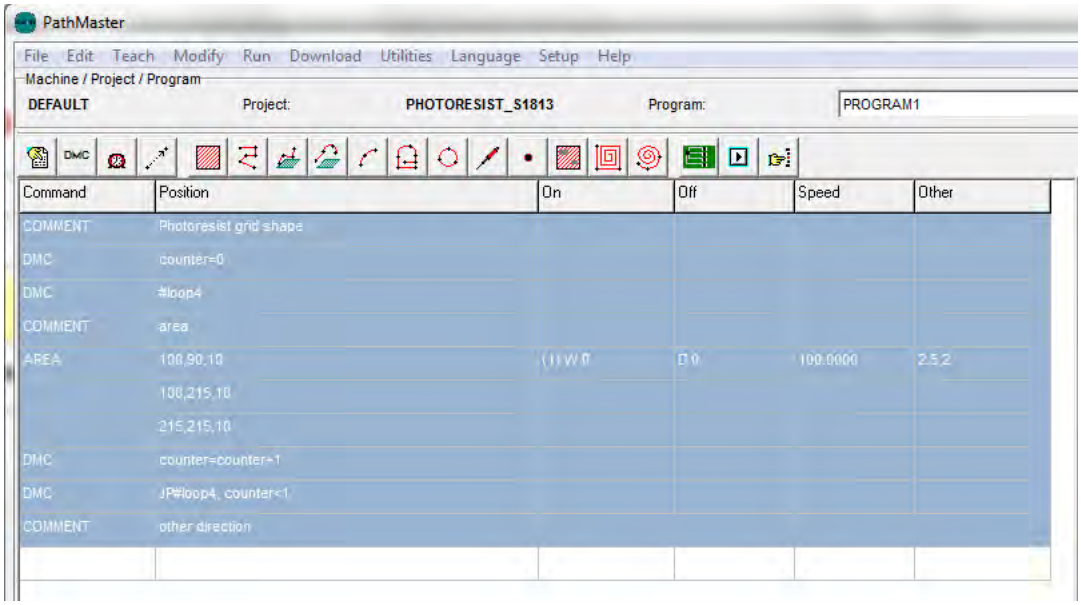

Figure 8-10: The “s1813 photoresist” program.

Deposition Process:

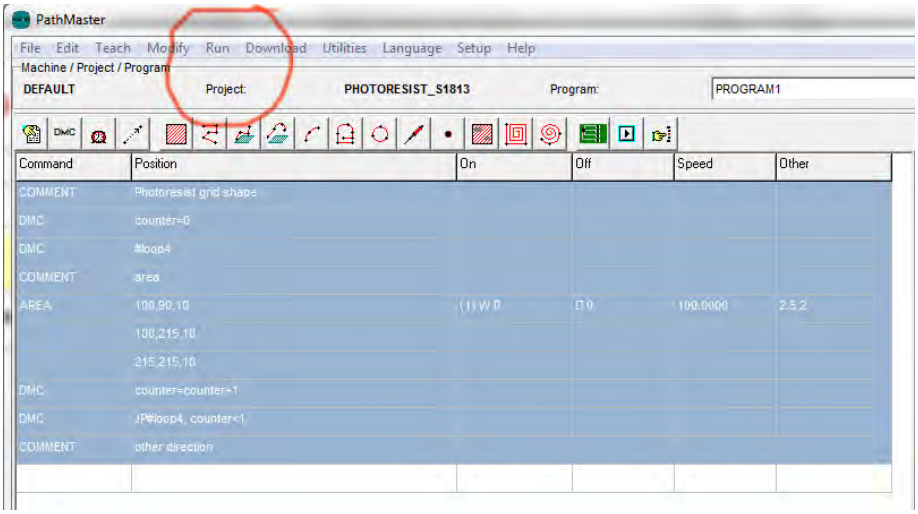

Figure 8-11: The “s1813 photoresist” program.

• To run the program:

Run -> all program

- **Make sure to press “Toggle valve ON” before every deposition**

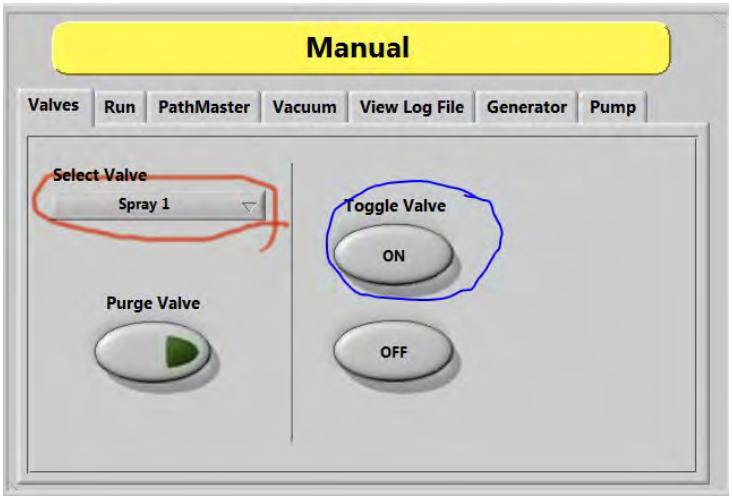

Figure 8-12: Toggle Valve “ON” in the Valves tab.

- **Make sure that “Dry” an not “WET” is checked. Then press “Start”.**

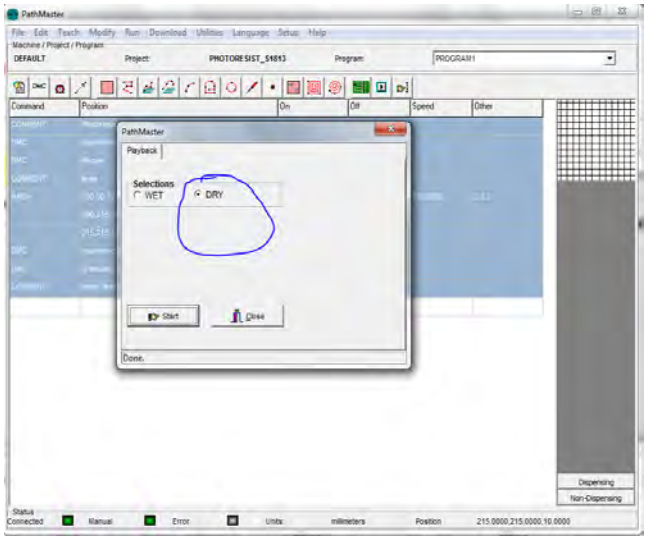

Figure 8-13: “Dry” run should be checked in the program.

Cleaning Process

- Withdraw the solution from the lines into the syringe by pressing the left arrow on the bottom of the syringe pump control panel.
- Use acetone to clean the syringe.
- Use acetone to wash away any resist remains in the lines.
- Repeat the acetone washing step.
- Withdraw acetone from the lines.
- Use IPA to wash the lines.
- Fill the line with acetone again, and leave the acetone solution in the lines overnight.

Next day

- Withdraw the acetone solution from the lines.
- Use IPA to wash the line.
- Clean the syringe using IPA

Shutdown Process

- Follow the 4D labs manual.

Appendix E. Publications and Awards

List of Publications

El-chami, I., Dixon-Luinenburg, O. and Bahreyni, B., 2016. Multiwalled carbon nanotube and graphene–polystyrene nanocomposites for bolometric detection. Journal of Vacuum Science & Technology B 34, 042001 (2016); https://doi.org/10.1116/1.4945804. AVS

My contributions: I was the lead investigator on the paper, wrote the manuscripts, developed the proposed concepts, built simulation models, designed experiments, fabricated samples, designed and built testing setups, and performed experimental verifications.

Shafiei, M., El-chami, I., Rintoul, L. and Bahreyni, B., 2017. Morphology of electrospun poly (ethylene oxide) ultra-fine fibres with incorporated MoO3 nanoparticles. Materials & Design. Volume 113, 5 January 2017, Pages 76-83. https://doi.org/10.1016/j.matdes.2016.10.011. Elsevier

My contributions: I was the co-lead investigator on the paper, wrote significant parts of the manuscript and revisions, developed parts of the proposed concepts, built simulation models, co-designed experiments, and performed experimental verifications.

El-chami, I., Vosoogh-Grayli, S., Zhuo, D. and Bahreyni, B., 2016. A vector light detector for proximity sensing applications. In 2016 IEEE SENSORS Proceedings (pp. 1-3).Orlando, FL, USA. DOI: 10.1109/ ICSENS.2016.7808584. IEEE

My contributions: I was the lead investigator on the paper, wrote the manuscripts, developed the proposed concepts, built simulation models, designed experiments, fabricated samples, designed and built testing setups, and performed experimental verifications.

El-chami, I., Zhuo, D.H., Vosoogh-Grayli, S. and Bahreyni, B., 2017, June. A silicon vector light sensor for proximity sensing applications. In 2017 19th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS) (pp. 163-166). 18-22 June 2017. DOI: 10.1109/TRANSDUCERS.2017.7994013. IEEE.

My contributions: I was the lead investigator on the paper, wrote the manuscripts, developed the proposed concepts, built simulation models, designed experiments, fabricated samples, designed and built testing setups, and performed experimental verifications.

Shafiei, M., El-chami, I., Rintoul, L. and Bahreyni, B. "Effect of Experimental Parameters on Morphology of Electrospun MoO3 Incorporated Polyethylene Oxide Nanofibres" International Conference on One-Dimensional Nanomaterials (ICON) 2016, Washington DC Metro Area. National Institute of Standards and Technology.

My contributions: I was the co-lead investigator on the paper, wrote significant parts of the manuscript and revisions, developed parts of the proposed concepts, built simulation models, co-designed experiments, and performed experimental verifications.

El-chami, I., Dixon-Luinenburg, O. and Bahreyni, B. “Application of carbon nanotube and graphene nanocomposites for fabrication of micro-bolometers.”

2015 IEEE SENSORS. 1-4 Nov. 2015. Busan, South Korea, South Korea. DOI: 10.1109/ICSENS.2015.7370514. IEEE

My contributions: I was the lead investigator on the paper, wrote the manuscripts, developed the proposed concepts, built simulation models, designed experiments, fabricated samples, designed and built testing setups, and performed experimental verifications.

Grayli, S.V., El-Chami, I., Bahreyni, B. and Leach, G. “Room temperature deposition of highly sensitive vanadium oxide films for infrared light sensing applications.” 2015 IEEE SENSORS. 1-4 Nov. 2015. Busan, South Korea, South Korea. DOI: 10.1109/ICSENS.2015.7370601. IEEE

My contributions: I was the co-lead investigator on the paper, wrote a part of the manuscript, developed parts of the proposed concepts, and performed experimental verifications.

Govaerts, J., Borgers, T., Nivelle, P., Van Dyck, R., El-Chami, I., Issa, I., Hoogewijs, T., van der Heide, A., Voroshazi, E., Szlufcik, J. and Poortmans, J.. “Progress in encapsulant-integrated multi-wire interconnection.” In 35th European Photovoltaic Solar Energy Conference and Exhibition-EUPVSEC (pp. 71-74), 2018. DOI: 10.4229/35thEUPVSEC20182018-1CO.1.3 WIP Renewable Energies.

My contributions: I was a part of a team working on the technology, contributed to the development of proposed concepts, fabricated samples, designed and built testing setups, and performed experimental verifications.

El-Chami, I., Oprins, H., Cherman, V., Horvath, I., Goverde, H., Govaerts, J., Borgers, T., Voroshazi, E. and Poortmans, J., “Determining the thermal behaviour of encapsulants and its impact on energy yield.” In 35th European

Photovoltaic Solar Energy Conference and Exhibition-EUPVSEC (pp. 273-277), 2018. DOI: 10.4229/35thEUPVSEC20182018-2AO.5.2.WIP Renewable Energies.

My contributions: I was a part of a team working on the technology, wrote the manuscripts, co-developed the proposed concepts, fabricated samples, designed and built testing setups, and performed experimental verifications.

Borgers, T., Govaerts, J., Van Dyck, R., El-Chami, I., Nivelle, P., van der Heide, A., Dourmen, G., Bervoets, R., Vastmans, L., Moors, R. and Manganiello, P.,. "INTERCONNECTION 1, 2, 3, 4.0: BUILDUP TOWARDS A PV TECHNOLOGY HERO?." In EU PVSEC Conference Proceedings (pp. 1-5). DOI: 10.4229/EUPVSEC20192019-1AP.1.2 WIP Renewable Energies.

My contributions: I was a part of a team working on the technology, contributed to the development of proposed concepts, fabricated samples, designed and built testing setups, and performed experimental verifications.

Research and extracurricular achievements and awards

- Mitacs Accelerate intern, University of British Columbia (2020-2021)
- Microsoft AI for Earth Grant award (2019-2020)
- Katholieke Universiteit Leuven (KU Leuven) international scholar scholarship (2017, 2018, 2019)
- Finalist- SFU Community Student Engagement Competition (2017/18,2018/19)
- Top 25– Microsoft Online Challenge–AI: Sustainable Life, Toronto (2019)
- Winner of the Lions' Den Pitch award– What The Hack (2019)
- Winner of the audience award– What The Hack (2019)
- Winner of the healthcare section – What The Hack (2019)

- Most liked project - Deloitte Online Garage Hackathon – Mobility– Amsterdam, Netherlands (2019)
- Finalist- Medical Device Development Centre 2019 Student Awards (2019)
- 3rd place - Lumohacks Hackathon – Vancouver, Canada (2018)
- Winner - Best hardware team - Lumohacks Hackathon –Vancouver, Canada (2018)
- Winner - MolenGEEK IoT Hackathon, Brussels, Belgium (2018)
- Winner- Coast Capital Savings Venture Idea Prize (2017)
- International co-op award SFU (2017)
- Graduate Fellowship MSE- Simon Fraser University (2016, 2017)
- SFU - International travel research award (2016)

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