Development of a MEMS Fabrication Process for Self-assembly of On-chip Antennas

by

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Abstract

This thesis describes the development of a fabrication process for building efficient 60 GHz on-chip antennas. Using a polymer micromachining process, a self-assembly method was developed to vertically raise the antennas. Vertical on-chip antennas can offer higher efficiency compared to planar antennas. The self-assembly method provides flexibility to create three-dimensional structures with different shapes. The curl and the direction of self-assembled curved structures can be controlled with simple changes in the design layout.

The fabrication process uses SU-8 polymer and the antennas are fabricated by coating the self-assembled polymer structures with metal. Micromachining using polymers is inexpensive, fast, and useful for a CMOS compatible MEMS fabrication process because most processing steps do not involve very high processing temperatures. This fabrication process can be completed within a day using university-level cleanroom equipment. This fast turnaround time makes the fabrication process ideal for prototyping antennas and other three-dimensional MEMS devices.

Several fabrication processes were developed and tested during the research. Many of the advances focused on making efficient on-chip antennas while keeping the cost and time for fabrication low by using the polymer micromachining. A thick dielectric layer of SU-8 was used to increase the efficiency of the antennas by increasing the spacing between the more lossy CMOS substrate and the metallic antennas. The associated transmission lines were fabricated on the dielectric layer with a patterned metal layer. The self-assembled SU-8 antenna structures were coated by metal layers on each side to cover the whole antenna structures with an even thickness.

Keywords: MEMS; polymer; SU-8; On-chip antennas; 60 GHz; CMOS
Dedication

I dedicate this work to God who stands by my side and leads me every step of the way, my parents who traded everything they had for my sake, and my lovely wife.
Acknowledgements

I would like to acknowledge Dr. Ash Parameswaran for his guidance and support over the past years. I would like to thank Dr. Rodney Vaughan and Dr. Behraad Bahreyni for serving as my co-supervisors and helping me complete this thesis project. I would like to thank Dr. Alireza Mahanfar who helped me start on this project, design antennas, and perform measurements. I would like to acknowledge Canadian Microelectronics Corporation and Orange Labs in La Turbie for providing measurement facilities for the antennas.
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<th>Full Form</th>
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<tbody>
<tr>
<td>ASK</td>
<td>Amplitude-shift Keying</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide Semiconductor</td>
</tr>
<tr>
<td>CTE</td>
<td>Coefficient of Thermal Expansion</td>
</tr>
<tr>
<td>CVD</td>
<td>Chemical Vapour Deposition</td>
</tr>
<tr>
<td>DI</td>
<td>Deionized</td>
</tr>
<tr>
<td>FSK</td>
<td>Frequency-shift Keying</td>
</tr>
<tr>
<td>IPA</td>
<td>Isopropyl Alcohol</td>
</tr>
<tr>
<td>ISI</td>
<td>Intersymbol Interference</td>
</tr>
<tr>
<td>LIGA</td>
<td>Lithographie, Galvanoformung, Abformung</td>
</tr>
<tr>
<td>MEMS</td>
<td>Micro-Electro-Mechanical-Systems</td>
</tr>
<tr>
<td>OOK</td>
<td>On-off Keying</td>
</tr>
<tr>
<td>OTA</td>
<td>Over-the-air</td>
</tr>
<tr>
<td>PECVD</td>
<td>Plasma Enhanced Chemical Vapour Deposition</td>
</tr>
<tr>
<td>PGMEA</td>
<td>Propylene Glycol Methyl Ether Acetate</td>
</tr>
<tr>
<td>PPM</td>
<td>Pulse-position Modulation</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>RFIC</td>
<td>Radio Frequency Integrated Circuit</td>
</tr>
<tr>
<td>RIE</td>
<td>Reactive-ion Etching</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning Electron Microscope</td>
</tr>
<tr>
<td>SoC</td>
<td>System-on-Chip</td>
</tr>
<tr>
<td>SiP</td>
<td>System-in-Package</td>
</tr>
<tr>
<td>TMAH</td>
<td>TetraMethyl Ammonium Hydroxide</td>
</tr>
<tr>
<td>UV</td>
<td>Ultra Violet</td>
</tr>
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</table>
1. Introduction

This thesis presents the development of a fabrication for building efficient on-chip millimeter-wave antennas for 60 GHz. The main focus is to tailor a fabrication process, which provides tools for antenna designer to build various types of microwave antennas integrated on top of radio frequency integrated circuits (RFICs). As the operating frequency increases, the size of antennas becomes small enough to be built on a small chip in batch using micro-electro-mechanical systems (MEMS) fabrications. MEMS technology refers to integration of mechanical elements, sensors, actuators, and electronics with sizes on the order of micrometers using microelectronics fabrication technologies. This chapter discusses some of the important concepts of microfabrication and transmission at the frequency of interest, and the motivation for the work.

1.1. Scaling Effects

When designing microstructures, the main forces that affect microstructures are quite different from those in macro scale. Table 1.1 shows the scaling laws that are of importance in micro scale [1]. The physics behind some of the scaling behaviour can be highly complicated and this aspect is not elaborated in the thesis. While some of the dominant effects would work in favour for MEMS devices, some need to be considered carefully when designing microdevices. In micro scale, devices are extremely light and the effect of gravity can be ignored. With much large surface per volume, micro devices are very useful for making sensors such as chemical and flow sensors. However, the device designers should pay special attention to high friction and stiction. The high friction leads to fast wear where moving parts are located and stiction can permanently pin down freestanding structures to the substrate surface.
### Table 1.1.  Selected length scale dependencies of design parameters for MEMS [1].

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Scaling</th>
<th>Comments</th>
</tr>
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<tbody>
<tr>
<td>Length (L)</td>
<td>L¹</td>
<td>Fundamental</td>
</tr>
<tr>
<td>Area (A)</td>
<td>L²</td>
<td>Fundamental</td>
</tr>
<tr>
<td>Volume (V)</td>
<td>L³</td>
<td>Fundamental</td>
</tr>
<tr>
<td>Surface area/volume (A/V)</td>
<td>L⁻¹</td>
<td>Fundamental</td>
</tr>
<tr>
<td>Mass (M)</td>
<td>L³</td>
<td>Assumes scale-independent density</td>
</tr>
<tr>
<td>Inertial force (F)</td>
<td>L³</td>
<td>Scales with mass</td>
</tr>
<tr>
<td>Power (W)</td>
<td>L²</td>
<td>Assumes scale-independent density</td>
</tr>
<tr>
<td>Power/volume (W/V)</td>
<td>L⁻¹</td>
<td>Assumes scale-independent density and power/mass</td>
</tr>
<tr>
<td>Structural natural frequency (ω)</td>
<td>L⁻¹</td>
<td>Given scale-independent modulus and density</td>
</tr>
<tr>
<td>Electrostatic force (Fₑ)</td>
<td>L²</td>
<td>Assumes scale-independent permittivity, dielectric breakdown voltage</td>
</tr>
<tr>
<td>Magnetic force (electromagnet) (Fₑₑₑₑ)</td>
<td>L⁴</td>
<td>Assumes scale-independent maximum current density</td>
</tr>
<tr>
<td>Magnetic force (permanent magnet) (Fₑₑₑₑ)</td>
<td>L³</td>
<td>Assumes scale-independent magnetic strength</td>
</tr>
<tr>
<td>Piezoelectric force (Fₑₑₑₑ)</td>
<td>L²</td>
<td>Assumes scale-independent piezo-mechanical constants, breakdown voltage</td>
</tr>
<tr>
<td>Surface tension</td>
<td>L¹</td>
<td>Assumes scale independence</td>
</tr>
</tbody>
</table>

### 1.2. Photolithography

Photolithography is a process where light exposures are used to pattern a layer of photoresist. Photoresist is a photosensitive polymer, whose solubility change in a corresponding photoresist developer when exposed with light. If photoresist becomes more soluble upon exposure and the exposed areas dissolve, it is called a positive photoresist (Figure 1.1). On the other hand, if exposed areas of photoresist become less soluble and unexposed areas are removed after development, it is called a negative photoresist.
Figure 1.1. Photolithography of a positive and a negative photoresist.

1.3. Etching in MEMS

After a photoresist layer is patterned, it is often used to etch the layer below the photoresist layer. The etching can be categorised into isotropic and anisotropic etching. In an isotropic etching, the material of interest is etched away without a directional preference. Therefore, the etch rate is equal in all directions. Hydrofluoric acid (HF) is an isotropic etchant, which has a high selectivity to silicon dioxide (SiO$_2$) over silicon (Si). On the other hand, certain directions are etched at different rates in an anisotropic etching. For example potassium hydroxide (KOH) etches silicon wafers at different rates depending on the crystallographic planes, where the (100) plane is etched 400 times faster than the (111) plane.

Reactive-ion Etching (RIE) is a type of dry etching where radicals are generated in plasma to remove deposited materials on a wafer. The plasma is generated by an electromagnetic field under a very low pressure. The benefit of RIE is directionality of etching where materials are etched away vertical to the wafer and the exact pattern of a layer can be transferred to a different layer below. In RIE, metals such as Au or Al are used as etch masks, which would be previously patterned using a photoresist.
1.4. **Bulk Micromachining**

Bulk micromachining involves etching of a substrate to create microstructures with either wet or dry etchants [2]. Wet etching is performed in a liquid medium such as HF and KOH. Using bulk micromachining processes, pressure sensors [3] and micropumps [4] were fabricated. Capacitive pressure sensors operate based on a thin membrane which is patterned using an anisotropic etching with a doped layer as an etch stop. The thin membranes in micropumps are made similarly and are actuated by thermal, piezoelectric, or electrostatic means to create positive and negative pressure for fluid movement.

1.5. **Surface Micromachining**

In surface micromachining, thin films are added to a substrate and are patterned to create MEMS devices [2]. Typically used materials for surface micromachining are metals, polycrystalline silicon, nitrides, oxides, and polymers. These materials can be directly deposited on a wafer and patterned, or a sacrificial layer can be used between the substrate and the structures to fabricate freestanding structures. Freestanding structures are attached to a substrate using anchors, such as cantilevers and bridges. The sacrificial layer is removed at the end of the fabrication whereas the structural material remains behind. With surface micromachining, microdevices with extremely small features can be fabricated with ease, such as micromotors which operate with electrostatic or magnetic force to rotate rotors [4, 5].

1.6. **Silicon in MEMS**

Silicon is a widely used material in microelectronics and the silicon that are predominantly used in MEMS devices are single crystal silicon and polycrystalline silicon. Single crystal silicon is grown from a seed crystal and every atom of silicon is contained within one lattice. The advantages of single crystal silicon are the lack of grain boundaries and predictable mechanical and electrical properties [6]. The single
crystal silicon has almost no residual stress, but due to the anisotropic nature of the material, some of the mechanical properties change depending on the direction.

Polycrystalline silicon, on the other hand, has isotropic material properties as silicon micro crystals are more randomly aligned. The distribution of crystals occurs due to the nature of deposition technology, which are typically chemical vapour deposition (CVD) or sputtering. In CVD, a wafer is exposed to precursor gases of target material that reacts with the substrate surface to produce a desired layer. Sputtering is a process where atoms of an interested material are ejected from a solid target due to bombardment of ion particles and deposited on a wafer. However, Polycrystalline silicon suffers from residual stress and the level of stress and the material properties change depending on the process parameters [7]. Annealing is used to reduce the amount of residual stress in polycrystalline silicon.

Silicon is a semi-conductor and introducing impurities can significantly change its electrical properties, which makes it useful for many electrical applications. For MEMS applications, the mechanical properties of silicon make it ideal for many applications. The etch rate of silicon can be changed with doping which enables very simple fabrication for creating microstructures. However, integrating the polycrystalline silicon MEMS devices with integrated circuits is challenging because of high processing temperatures that are required which in turn damage the integrated circuits [8].

1.7. Assembly in MEMS

As MEMS fabrication processes are based on technologies for fabricating microelectronics, conventional MEMS structures are predominantly two-dimensional. While this characteristic allows compact packaging of MEMS devices, three-dimensional structures are highly desirable for certain applications such as micro-optics [9], electromagnetic, and thermal applications. In order to achieve high aspect ratio microstructures, assemblies of predominantly two-dimensional microstructures are required.
1.7.1. **Manual and Automated Assembly**

For manual and automated assemblies, the assembled parts of the microstructures need mechanical linkages such as hinges [10], torsion bars [11], and suspended springs [12], which are used to allow the motions necessary for the assembly to take place. Then, external forces are applied on the structures with tools such as three-axis manipulators, which have a small enough tip to move only certain parts of microstructures. The three-axis manipulators are controlled by hand and the assembly takes time and precision, and repeatability of assembly is dependent on the skill of the users. These manipulators can be replaced with robotic arms to assemble the microstructures, but the cost for the system is high and the assembly is performed serially, still requiring a long time to complete a large number of assemblies.

Automated assemblies are accomplished by using microactuators to manipulate microstructures to assemble. These microactuators are mechanically linked to the structures and the linkages are typically buckling systems and hinges. While hinges provide a true rotation for assembly, the buckling systems provide good electrical routing. Electrostatic actuators [13-16], thermal actuators [17], magnetic actuators [18], and one-time actuators based on non-uniform residual stress [19] have been previously used for assembly, but they all require a large footprint on the chip, adding cost and complexity to the devices.

1.7.2. **Self-assembly**

Self-assembly of microstructures enable fabrication of three-dimensional structures without the need of an external mechanism. Thus, self-assembly can reduce the fabrication cost dramatically by reducing the time required for assembly and removing the real estate needed for the microactuators. Residual stress has been used for self-assembly for both micro and nano-structures [20-24]. The intrinsic stress developed during the deposition of structural materials, such as silicon nitride, chromium, molybdenum-chromium, gold, and polycrystalline silicon, curl the freestanding microstructures when they are released from the substrate. The disadvantage of using multimaterial layers for self-assembly is temperature sensitivity where a difference in the coefficient of thermal expansion (CTE) would cause the structure to move with
surrounding temperature. This may be useful for actuator applications, but is not very desirable for static structures.

Some self-assembly methods allow bending of only certain parts of microstructures, which provides flexibility to create highly complex three-dimensional structures. Thus, the self-assembled structures can be combination of flat and curved structures. Surface tension of molten solder and photoresist has been used for self-assembly [25-28]. The molten materials are placed between two flat structures and the degree of self-assembly is determined by controlling the volume of the materials. When the wafer is heated, the materials melt and the surface tension force causes the structures pull towards each other. However, to achieve high precision for self-assembly, mechanical locks need to be used to stop the assembly when desired angles are obtained.

Another method of accomplishing self-assembly is based on shrinkage of polyimide which is placed between anisotropically etched silicon structures. Because of slanted sidewalls, a difference exists between the width at the top and at the bottom of polyimide structures as shown in Figure. As polyimide cures, it shrinks in volume and because the top portion of the polyimide is wider than the bottom, the width of top would change by greater magnitude than the bottom and a self-assembled angle is produced at the joint.
1.8. Brief Introduction to 60 GHz Communications

1.8.1. Application

Recently, 57-64GHz spectrum has been released for wireless transmission applications for high data rates [30]. Millimeter size antennas are required in order to accommodate the operation frequency. Because of the reduced size of antennas, a system-on-chip along with the antenna could be potentially integrated into any electronic devices that would benefit from very high data transmission rate. However, the attenuation is severe making it most suitable for close-range applications. Home electronics can benefit by eliminating the signal wires and replacing them with high data rate wireless communication using the 60 GHz transmission. For instance, several home electronics manufacturers offer wireless screens and speakers for home theatre systems. This way, visible part of the systems can be made compact and lightweight. Similarly, cables between speakers and audio sources are eliminated.
1.8.2. **Modulation**

Several modulation schemes have been proposed while the best modulation format is still to be determined. Orthogonal frequency-division multiplexing (OFDM) and single carrier transmission with frequency-domain equalization provides the lowest complexity to mitigate severe intersymbol interference (ISI), while frequency-shift keying (FSK), amplitude-shift keying (ASK), on-off keying (OOK), and pulse-position modulation (PPM) provides low implementation complexity in the transmitter and receiver, but low spectral efficiency [29]. Discussion of the details of these modulation schemes are outside the scope of this thesis.

1.9. **Motivation**

System-on-chip (SoC) and System-in-package (SiP) architectures integrate the radio-frequency (RF) front-end, which converts signals at the original incoming frequency, as well as analog-to-digital converters, and signal processing blocks. What has not been adopted widely is the integration of antennas onto a chip or a package. Typically, off-chip antennas are used in conjunction with the transceiver circuitry in a wireless system. The signal path between the antennas and the chip is accomplished by using a matching circuit and other radio-frequency components, but it contributes to loss of signal-to-noise ratio (SNR). Thus, receivers would lose sensitivity for reception and transmitters would waste more power for radiation. Developing a method for integration of antennas for mainstream radio-frequency front-end fabrication such as CMOS would be highly desirable.

For commonly used wireless communication frequencies, the sizes of the antennas required are quite large and integration of those antennas on a chip is not feasible as antenna dimensions are much larger than the chip dimensions. However, at the 60 GHz band, the size of the antennas becomes quite small making it physically possible to integrate them on chips [30-32]. Several works have been done previously on development of on-chip antennas [33-40].

Commonly used on-chip antennas are planar antennas as typical integrated circuits and MEMS devices are planar [41, 42]. By using the commonly used fabrication
processes, the development time would be shorter and the results would be easier to predict. But these planar antennas are not suitable for CMOS substrates as they have low resistivity in order to prevent the latch up problem where undesired short circuits are realized. A planar patch-type antenna on top of the low-resistivity substrate would be inefficient due to the high electric field in the patch cavity and the effect would be magnified at high frequencies, such as 60 GHz.

In order to address the issues of fabricating patch-type antennas on the low resistivity CMOS substrate, antennas were fabricated on a polymer substrate [43, 44]. A CMOS compatible fabrication process, which can fabricate patch antennas supported by post structures, was presented. The above method of distancing the patch antennas from the low resistivity substrate improves radiation efficiency, but part of the radiated power is from surface waves, which are normally difficult to control, and are undesirable.

Monopole-type antennas have advantages over planar antennas because they do not suffer from substrate cavity loss of patch-type antennas and are less affected by ground plane losses. As presented in a previous work [45], a vertical dipole showed better electric field strength in the far field even on an lossy ground compared to a horizontal dipole. Two important performance metrics of communication systems are range and data-rate, and they are directly dependent on the efficiency of the antennas.

Several monopole antennas have been reported in the literature. An array of monopole antennas has been presented where monopole structures are made with SU-8 posts to obtain vertical structures and are then coated with sputtered gold [46, 47]. Using this method, the frequency range is limited because the lengths of the monopole structures are determined by the thickness of the SU-8 layers. Magnetic assembly can be used for assembling multiple antennas at once and solve the issue of having limited length [48], but the alignment of assembled structures is limited to a single direction restricting polarization, pattern, and frequency of the antennas to the performance of basic vertical monopoles.

In this thesis a new method for fabricating self-assembled antennas is presented where the lengths, assembly angles and curvatures, and shapes are independently defined using photolithography. For fabricating a vertical monopole antenna, the base of
the antenna is curved by self-assembly to prop up the antenna structure vertical. With the radius of self-assembled curvature as small as 420 µm, vertical part of the antenna is fabricated with a straight tip attached to the curved base. With the developed method, the self-assemblies occur only on parts of the areas of microstructures where they are necessary and different sizes and types of antennas can be fabricated at the same time. This flexibility would allow integration of antennas for different frequencies in a compact system. For example, monopoles of different azimuth and elevation angles can be fabricated to provide different polarizations and be used for diversity systems [49].

Some of the limiting factors for typical MEMS fabrication technologies into a CMOS fabrication process are high fabrication temperatures and introduction of gold. The main reason polymer MEMS was considered, as a post-fabrication process for creating on-chip antennas, was its compatibility with CMOS fabricated chips. All of the fabrications steps are performed at low temperatures, under 200°C and would be compatible for post-CMOS integration. As the developed method would be a post-CMOS fabrication process, gold should not be able to diffuse into active areas of the CMOS wafer with a passivation layer applied on a CMOS wafer.
2. SU-8 in MEMS

2.1. Introduction

SU-8 is an epoxy-based negative photoresist, which can be used to create MEMS structures. SU-8 has many advantages over conventional materials used for fabricating microstructures. First, fabrication of high aspect ratio microstructures from SU-8 is relatively easy and cost effective compared to processes such as lithographie, galvanof ormung und abformug (LIGA). The LIGA process was developed to fabricate high aspect ratio metal microstructures [50]. Typical illumination source for LIGA is synchrotron, which provides collimated monochromatic X-rays. The synchrotron and X-ray masks make the fabrication process expensive. SU-8, on the other hand, only requires typical ultra-violet (UV) aligners, spin coaters, and hotplates available in most university-level cleanrooms to fabricate LIGA like high-aspect-ratio structures. Using standard photolithography, up to 20:1 aspect ratios are achieved [51]. Also, the processing of SU-8 is fast compared to most MEMS structural fabrications. The fabrication process steps include spin-coating, softbake, exposure, post exposure-bake, development, and hardbake, where hardbake can be optional. All these process steps can be completed within an hour although the exact time varies depending on fabrication recipes.

2.2. Physical Properties

SU-8 is made into a photoresist by adding a photo acid generator, which becomes activated when illuminated with light at wavelengths below 400 nm and acts as a catalyst during a thermally driven crosslinking [52]. The crosslinking creates reactions among SU-8 monomers to change into a polymer. The degree of crosslinking depends on the exposure dose, and time and temperature used for the post exposure-bake.
Different approaches have been used to determine Young’s modulus of SU-8, which is a measure of the stiffness of an elastic material. Larsson et al. used a cantilever profilometry method and the measured Young’s modulus was 3.7 GPa, assuming that the Young’s modulus is isotropic [53]. On the other hand, Hopcroft et al. used their fabricated cantilevers and reported Young’s modulus of 2.7 GPa [54].

Lorenz et al. determined the bi-axial modulus of elasticity (E/(1-ν)) and the coefficient of thermal expansion with a wafer bowing experiment with an SU-8 film on top [55]. Feng et al. reported that the Young’s modulus of SU-8 is transversely isotropic with different values for in-plane and out-of-plane directions [56]. Table 2. and Table summarize the reported mechanical properties.

**Table 2.1. Mechanical properties of SU-8 reported by Lorenz et al.**

<table>
<thead>
<tr>
<th>Property</th>
<th>Mean</th>
<th>Standard deviation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coefficient of thermal expansion</td>
<td>52.0 ppm/°C</td>
<td>5.1 ppm/°C</td>
</tr>
<tr>
<td>E/(1-ν)</td>
<td>5.18E9 Pa</td>
<td>0.089 Pa</td>
</tr>
</tbody>
</table>

**Table 2.2. Mechanical properties of SU-8 reported by Feng et al. 'i' refers to in-plane and 'o' refers to out-of-plane. The range refers to the experimental error.**

<table>
<thead>
<tr>
<th>Constants</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Young’s modulus</td>
<td></td>
</tr>
<tr>
<td>(E_i)</td>
<td>3.2±0.2 GPa</td>
</tr>
<tr>
<td>(E_o)</td>
<td>5.9±0.9 GPa</td>
</tr>
<tr>
<td>Shear modulus</td>
<td></td>
</tr>
<tr>
<td>(G_i)</td>
<td>1.2±0.4 GPa</td>
</tr>
<tr>
<td>(G_o)</td>
<td>0.3 GPa</td>
</tr>
<tr>
<td>Poisson’s ratio</td>
<td></td>
</tr>
<tr>
<td>(\nu_i)</td>
<td>0.33±0.02</td>
</tr>
<tr>
<td>(\nu_o)</td>
<td>0.29±0.02</td>
</tr>
<tr>
<td>Coefficient of thermal expansion</td>
<td></td>
</tr>
<tr>
<td>(\alpha_i)</td>
<td>87.1±2 ppm/°C</td>
</tr>
<tr>
<td>(\alpha_o)</td>
<td>278±31 ppm/°C</td>
</tr>
</tbody>
</table>
3. Fabrication Environment

All the fabrication processing that would be discussed in later chapters were performed in the Simon Fraser University’s School of Engineering Science cleanroom. Most of this fabrication equipment should be available in a university level cleanroom environment. Many of the decisions on the choice of the fabrication process steps were mainly centred on the availability of the cleanroom equipment. After fabrication, structural measurements were performed on a probe station in a mini-cleanroom module [57].

3.1. Class 100 Cleanroom

The Simon Fraser University’s School of Engineering Science cleanroom is divided into two classes: class 1000 and class 100. The number of the cleanroom classification represents the number of permitted particles of size 0.5 µm or greater per cubic foot of air. Most of the fabrication processing was done in the class 100 cleanroom where most of the fabrication equipment was located.

3.1.1. Spin-coater

A spin-coater is used to spread a liquid into a very thin layer on a wafer with highly repeatable thickness control. Depending on the viscosity of the liquid, the speed the liquid was spun at, the duration of the spin, and the surface of the wafer, the resulting thickness changes. The spin-coater was used for application of positive photoresists, polystyrene solution, SU-8 photoresist, and ProLIFT on a wafer. The wafer is held on a spinning chuck by vacuum as the spin starts. As will be discussed later, to ensure the full coverage of the spun layers on a wafer, enough liquid was poured on the wafer before spinning and the spin speed was increased gradually. The duration time of spin was measured when the target spin speed was reached. This method of spinning was quite important especially when the wafer surface was uneven with microstructures
partially fabricated on top. Figure 1 shows the spin-coater and the chuck in the spin-coater tray.

![Spin-coater](image)

**Figure 3.1.** Spin-coater.

### 3.1.2. Ovens

Two ovens located in the class 100 cleanroom are used for softbaking of positive photoresists and dehydration baking of wafers after an RCA cleaning, which is a set of standard wafer cleaning steps. The temperatures for these ovens are always set to 100°C and 120°C, respectively. After positive photoresists were spun on wafers, the wafers were then transferred to the 100°C oven and softbaked for 15 minutes to drive out solvent from the layer for contact mask alignment. The 120°C oven was used for dehydration of wafers after RCA cleaning. The two ovens used for the fabrications are shown in Figure 3.2.
3.1.3. **UV Aligner**

The most commonly used method of exposing features on a photoresist layer in microfabrication is using a ultra-violet (UV) aligner. The UV aligner in the cleanroom requires a mask, which comes into contact with a wafer and the mask would have features, which either block or transmit the UV light. The UV aligner exposes a collimated UV light to ensure features are transferred to a photoresist layer with high accuracy. An i-line light source was used which has peak intensity at 365 nm. The power output of the UV aligner changes over usage. In the early stage of the development, the power output of the exposure was around 8 mW/cm², but the power output changed to 13 mW/cm² during the later stage because the light source was replaced for maintenance. Figure 3.3 shows the UV aligner.

![Ovens in the class 100 cleanroom.](image)
Typically, the masks used for exposure are chrome masks with glass plates. These are held by vacuum on the aligner and a wafer can be firmly pressed onto the masks. During exposure, a good contact with a minimal gap between the mask and the wafer is very important to ensure that the exposed features are same as the features on the mask and not be affected by light diffraction. While chrome masks offer very small feature sizes and a good contact exposure, they are expensive, costing hundreds of dollars per mask; and the process takes significant turnaround time. During the development of the fabrication processes, emulsion masks on Mylar sheets were used instead. The advantages of the emulsion masks are low cost, which is less than $20 per mask, and a quick turnaround time. The minimum feature size of these masks is 5 µm, which is more than enough for fabrication of the self-assembled antenna structures. Because these masks are flexible, a different method of holding these masks is necessary to minimize the gap between the masks and a wafer. Instead of using vacuum to hold the masks in place, these masks were placed under a glass plate of similar size to a chrome mask and both the masks and the glass plate were held by using neodymium rare earth magnets on the UV aligner. Figure 3.4 shows how the emulsion masks were held on the UV aligner.
3.1.4. **Acid and Base Wet Bench**

The acid and base wet bench is located under a fume hood and protects users from dangerous fumes while using organic and reactive solvents. Most of the wet processing steps including RCA cleaning, photoresists developments, and metal etchings are performed in this area. Although fume hood protects users from harmful fumes, proper protective gears need to be worn to protect users from acid and base. Figure 3.5 shows a picture of the acid and base wet bench.
3.1.5. **Solvent Wet Bench**

The solvent wet bench does not have a fume hood but instead it has an open area, which has laminar flow of air to transport solvent fumes away from the user. This is an area where simple fabrications steps such as rinsing and drying can be performed without being obstructed by the fume hood setup. For drying, either spin-dryer or nitrogen airgun is used. Wafers with MEMS structures should not be dried using the spin-dryer. If drying is necessary, nitrogen airgun can be used from very far to speed up the drying process. Figure 3.6 shows the solvent wet bench with the spin-dryer and the nitrogen airgun.
Figure 3.6.  Solvent wet bench with a spin-dryer and a nitrogen airgun on the right.

3.1.6.  Hot-plates

There are five hotplates in the class 100 cleanroom and these are mainly used for the softbake, post exposure-bake, and hardbake of the SU-8 photoresist, and softbaking of the ProLIFT. The target temperatures and the ramping rates of these hotplates can be programmed. Especially for SU-8 photoresists, hotplates are recommended as an SU-8 photoresist layer can develop a skin layer on top if an oven is used instead. If a skin layer is created, it prevents proper drying out of the SU-8 photoresist solvents. Compared to the ovens, the hotplates can reach target temperatures quick enough that whenever temperatures other than the standard set temperatures of the ovens are needed, the hotplates are better choices. The one downside is that only one wafer can be baked per hotplate. Figure 3.7 shows hotplates placed on a rack.
3.1.7. **Sputtering System**

The Corona Vacuum Coaters DC sputtering system is used for all metal depositions required for the fabrications processes. The sputtering systems can have up to five different targets to be deposited on wafers. Metals that were deposited during the fabrications were chromium, gold, aluminum, and copper. When the sputtering chamber is brought down to vacuum, a suggested current value, previously determined by the cleanroom technicians, is used for each metal with a DC power supply. The sputtering system has five wafer stages in the chamber, which can be rotated to deposit metal at once. Figure 3.8 shows the sputtering system with a nitrogen tank in front, which is used for cooling the high vacuum pump.
For etching of the sacrificial layers and activation of SU-8 layers, Axic Benchmark 800 plasma-enhanced chemical vapour deposition (PECVD) and RIE system was used. The system has two separate chambers for PECVD and RIE. Only the RIE, which is the chamber on the right side in Figure 3.9, was used during the fabrications. The system’s vacuum pump is located behind the left window shown in the Figure 3.9. The pressure, power, and flow rates of the gasses are all controlled with the computer system. Etch rates are different for different materials and etching parameters, and tests were done to obtain the etch rates, which were later used to determine the etch times required for desired thicknesses of sacrificial layers.
3.2. Class 1000 Cleanroom

Most of the post-fabrication equipment is located in the class 1000 cleanroom for testing and measurement. Class 100 cleanroom uses lights with yellow filters for lighting of the room for photoresist handling. On the other hand, class 1000 cleanroom has a switch that controls between regular fluorescent lights and yellow lights. Thus, all the photosensitive fabrication processes are performed in the class 100 cleanroom, whereas yellow lights are used for profilometer measurements only while working with photoresists in the class 1000 area. As class 100 cleanroom has limited space, most of the cleanroom supplies are stored in the class 1000 cleanroom.

3.2.1. Profilometer

The profilometer uses a stylus with a diamond tip, which is dragged across a wafer to measure the height profile. This equipment was extensively used to measure feature sizes, layer thickness, and depth of etched holes. The profilometer was
especially important for timed etching of sacrificial layers to create dimple features. By measuring the depth of the dimple features, approximate etching rate was estimated, which can then be used for achieving desired dimple depths. Also, the profilometer measurements can be used to determine how well the mask contacts are with the wafers as poor mask contacts would lead to bloated feature sizes on the wafers. For the same reason, the measurements were undertaken on various locations of the wafers as the quality of contacts might vary over the area of a wafer as thick polymer layers were used for the fabrications. Figure 3.10 shows the profilometer on a vibration isolation table.

![Profilometer on a vibration isolation table.](image)

**Figure 3.10. Profilometer**

### 3.2.2. Wafer Scriber

The wafer scriber is used to cut a fabricated wafer into rectangular blocks called dice. Typically, the size of a die are in the range of millimeter squared, but when the wafer needs to be broken manually after scribing, cutting of dice smaller than 5 mm by 5 mm are quite difficult. For the purpose of creating self-assembled antennas with a ground plane, the size of dice was kept at 10 mm by 10 mm. The scriber has a diamond tip, which cuts a fine line on a silicon wafer. Silicon wafers cleave along the crystallographic planes most easily. When <100> silicon wafers are used, crystallographic planes are parallel and perpendicular to the major flat of the wafers and
dling the wafer into square or rectangular pieces are possible by scribing along those crystallographic planes. Another method to dice a wafer is using a wafer saw. When MEMS structures are already released, a wafer saw cannot be used, as it requires coolant to be sprayed on the wafer while cutting. For fabrication processes, which required sputtering of metals only after microstructures were release, the wafer scriber was used. Figure 3.11 shows the wafer scriber.

![Wafer scriber](image)

**Figure 3.11. Wafer scriber.**

### 3.3. Mini-cleanroom

The mini-cleanroom was developed to do simple measurement and testing tasks outside of the School of Engineering Science cleanroom for MEMS projects, which are fairly insensitive to dusts and does not require class 1000 cleanroom level of air quality. The details of building the mini-cleanroom were discussed in [57]. A probe station microscope with a video camera was used in the mini-cleanroom for characterization of the self-assembly mechanism that would be discussed in later chapters. The video camera is connected to a computer to take screen captures, and the captured images were analysed using National Instruments Vision builder software [58]. To take screen captures of self-assembled structures from the side, the self-assembled structures were
attached to microstructures, which were manually assembled vertical to the substrate using the three-axis manipulators with probe needles. Then, the side of the self-assembled structures were viewed through the microscope and the camera. Figure 3.12 shows the mini-cleanroom and the probe station microscope.

![Figure 3.12. Pictures of the mini-cleanroom and the probe station used for curvature measurements.](image)
4. Polystyrene Process

4.1. Introduction

The proposed research involves fabrication of three-dimensional self-assembled MEMS structures by using stress developed during fabrication processes to control curvatures of structures. Usually, such stress is introduced in microstructures due to metal depositions or thermal stress of two materials with two different CTE. The proposed fabrication process uses a polymer called SU-8 manufactured by MicroChem as its structural material. As described in the previous work [59], SU-8 changes in volume during its curing process. When fully crosslinked, volumes of SU-8 decrease by about 3% compared to its softbaked state [60]. Therefore, when SU-8 crosslinks on top of another rigid structure, it introduces tensile stress on it. When this stress is applied to an overhanging SU-8 structure, the overhanging structure would deform to relieve the stress. This deformation can be used to self-assemble overhanging SU-8 structures. Therefore, self-assembly can be achieved with just two layer of SU-8 and a sacrificial layer needed make SU-8 structures freestanding.

4.2. Self-assembly Using Polystyrene as a Sacrificial Material

Different sizes of repeating SU-8 structures are used to tailor direction and magnitude of curvatures on specified parts of structures with the given amount of stress developed (Figure 4.1). In the previous work [59], bars of different length and width were used for the repeating top structures. The sizes of the repeating structures can be same throughout to create an even curvature or can be changed to have a varying curvature on a single structure. Also, the self-assembly would occur only on the area where the top SU-8 structures are placed. Other areas without the top SU-8 structures would not be affected by stress and remain planar.
Because of typical sizes of fabricated structures, these structures can be effectively used for making millimeter-wave antennas. Typical length for quarter-wavelength antennas at 60 GHz would be 1.25 mm. For creating a self-assembled 60 GHz monopole antennas, overhanging SU-8 cantilevers were raised by placing the stress-inducing structures on top of the cantilevers, making the cantilevers to curl to an upright position. Width and length of the cantilevers used for making the antennas were 200 µm and 1.25 mm, respectively. Figure 4.2 shows the curvature measurement performed only using the repeating bar structures for self-assembly from the previous work. Ideally, the 60 GHz antennas need to be self-assembled to a vertical position to raise the antennas as far as possible from the silicon substrate and achieve highest efficiency possible with the described self-assembly. However, in order for the tip of a 1.25 mm long antenna to be raised vertical at the tip, curvature required from the self-assembly is $1257 \text{ m}^{-1}$. The described self-assembly method does not provide enough curvature to be able to raise the 1.25 mm long antennas to the vertical.

*Figure 4.1. The (a) layout and (b) cross-sectional view of the self-assembly mechanism. The dotted illustration of (b) indicates the final shape.*
4.3. Enhanced Self-assembly

4.3.1. Theory

For the proposed research, a method of creating a higher range of curvatures was needed to accommodate fabrication of 60 GHz antennas. As can be seen in Figure 4.1, unused spaces exist between the stress-inducing bar structures. If these spaces can be used to introduce another set of stress, a higher range of curvatures can be fabricated than those shown in Figure 4.2. In the previous study where only the stress-inducing bar structures were used, the effect of increasing the size of the bar structures decreased due to added stiffness of the overall structure. An efficient way to apply stress on the underlying SU-8 structure is to apply stress on it with minimal physical connections to prevent from the increased stiffness of the overall structure.

A new self-assembly method was proposed where overhanging structures would be applied between the stress-inducing bar structures to further enhance resulting self-

Figure 4.2. Curvature responses to increasing bar length to pitch length ratios for a constant pitch length of 100 µm [59].
assembled curvatures. As previously discussed, softbaked SU-8 crosslinks where it is exposed with a required dosage of UV light and heated to the post-exposure-baking temperature. A short exposure step is used to crosslink only the top portion of a thick softbaked SU-8 layer and create overhanging bridge structures between the bar structures. The short exposure step is done right after the bar structures are defined with a much longer exposure time. The definition of bridge structures would overlap the bar structures to ensure connectivity to the bar structures. Another short exposure over the bar structures would not affect the definitions of the bar structures as they were overexposed previously.

The addition of these bridge structures increases the resulting curvatures significantly since these bridge structures make use of the free spaces between the bar structures with only slight increase in the stiffness of overall structure. Figure 4.3 shows the cross-sectional view of a cantilever with the self-assembly mechanism.

![Figure 4.3](image)

**Figure 4.3.** Cross-sectional view of a cantilever with the self-assembly mechanism with bridge structures.
4.3.2.  **Process Description**

The following describes the fabrication process steps in detail along with a figure for each step. Captions for the figures are omitted to reduce redundancy.

(a) 50 nm of chrome and 50 nm of gold are sputtered on a RCA cleaned wafer to serve as a base for the ground plane and alignment markers during SU-8 exposures.

(b) 20% weight percentage polystyrene solution is spun on the wafer at 1500 rpm for 30 seconds and a 6 µm thick polystyrene layer is made. The polystyrene layer dries immediately, and Shipley 1827 photoresist is spun at 1500 rpm for 30 seconds for thickness of around 6 µm. The wafer is then softbaked in an oven at 100°C for 15 minutes.

(c) The wafer is exposed through the anchor mask for 80 seconds to define anchors of microstructures. The photoresist layer is then developed in Microposit MF-319 developer for 3 minutes with agitation. The wafer is rinsed in deionized (DI) water and dried for another exposure step.
(d) The wafer is exposed through the dimple mask for 14 seconds to expose the photoresist to only about 2 µm deep for dimple features. Dimple features are used to reduce stiction of overhanging microstructures to the substrate. The photoresist layer is again developed in Microposit MF-319 developer for 3 minutes with agitation. The wafer is then rinsed DI water and dried.

(e) The anchor and dimple features are transferred to the polystyrene layer through RIE for 38 minutes with O₂ plasma at 40 sccm of O₂ flow rate, 100 mtorr of pressure, and 150 W of power. The etching process is complete when the metal layer is revealed through the anchor features. An anchor depth of around 5.5 µm and a dimple depth of around 2 µm are achieved.

(f) Gold is etched from the anchor features after 30 seconds of agitation in aqueous potassium iodide (KI). Alignment markers are made with
chrome to overcome similar indices of refraction of polystyrene and SU-8 during subsequent exposure alignments.

(g) MicroChem SU-8 2010 is spun on to a 10 µm thickness at 3500 rpm for 30 seconds. The wafer is softbaked on a hotplate with ramping from room temperature (20°C) to 95°C at 300°C/hour ramping rate and then the temperature is kept at 95°C for another 30 minutes.

(h) The wafer is exposed for 45 seconds through the first structural layer mask. The first SU-8 layer features are overexposed for complete crosslinking before the second SU-8 layer is applied. The SU-8 layer is then post-exposure-baked on a hotplate with ramping from room temperature (20°C) to 95°C at 300°C/hour and then the temperature is kept at 95°C for another 15 minutes.
(i) The second SU-8 layer is spun on to a 21 µm thickness at 1000 rpm for 30 seconds. A thicker layer is used to increase relative stiffness with defined support bar structures and leave enough room for bridge structures to be defined with a brief exposure. The wafer is softbaked on a hotplate at 95°C for 30 minutes.

(j) The wafer is exposed for 60 seconds through the mask for support structures. Overexposure is desired to fully crosslink the support bar structures and to ensure good adhesion to the first structural layer.

(k) The wafer is exposed for 8.5 seconds through the mask for bridge structures. Generally, the bridge features on the mask cover both support bars and areas between support bars to ensure continuity of the bridge structures.
(l) The SU-8 layers are developed in MicroChem SU-8 developer. Then, the sacrificial polystyrene layer is stripped in toluene and the structures are released for self-assembly. Isopropyl alcohol (IPA) is used to rinse the wafer and enhance drying process. As solvents are released from the structures, the self-assembly completes.

4.3.3. Metallization of PS Process for Electrical conductivity

As shown in previous work [61], freestanding SU-8 microstructures can be coated with metal in order to make them electrically conductive and use them as actuators. As a final step of the fabrication process, the whole wafer can be coated with chromium and gold metal bi-layer to provide good electrical conductivity. The coating process of metals can be performed with either sputtering or evaporation methods. Due to lack of access to an evaporator in the cleanroom, only the sputtering method was used for this work. Metal deposition using the sputtering is fairly directional and the degree of directionality is slightly different depending on the metal. Sputtering of both chromium and gold would result in the metals being coated on top and on side of polymer microstructures.

Sometimes, fabricated microstructures need to be electrically isolated from rest of the wafer. As polymer microstructures are themselves electrically insulating, the metal depositions on the microstructures need to be separated from rest of the wafer in order to make the metal-coated microstructures being electrically isolated. Since the sputtering of the metals would coat sides of microstructures, the sides need to be designed in such a way that there would be discontinuity of the metal coverage. Overhanging structures as shown in Figure 4.4 are created to accomplish the discontinuity of the metal coverage. The metals would only land on the top surface and
the sides of the overhanging features during the sputtering process. No metal is deposited underneath the overhanging features due to the directionality of the sputtering deposition.

Figure 4.4. Representation of how electrical isolation is achieved using overhanging features.

The sacrificial layer is necessary for creating the overhanging features, as it is needed for creating freestanding microstructures. The transmission lines were patterned by blocking sputtered metals with overhanging structures, separating metals on signal lines from ground plane. Three factors determine the accuracy of fabricating transmission lines. They are sacrificial layer thickness, first structural layer thickness and accuracy of the exposed features. The accuracy of thickness of the sacrificial layer is critical as it determines the distance of the transmission line from the ground plane. As the metal layers are deposited on the transmission line structures, the sides of the overhanging features of the transmission lines are also coated. Thus, the thickness of the transmission line structures is added to the width of the transmission line, making the thickness of the transmission line structure critical.

As uncrosslinked SU-8 may be affected by sputtering, having a patterned metal layer on top of an SU-8 layer is difficult unless the structure are already crosslinked and developed. During the development process of the fabrication, the polystyrene sacrificial layer also gets partially etched away releasing some of the structures. Thus, spinning of photoresist for the purpose of patterning deposited metal layers on top of developed SU-8 structures is not possible. In order to integrate a patterned metal layer on top of the SU-8 structures, the sacrificial layer should be inert to the SU-8 developer.

In what follows, we show the process steps used for fabricating transmission lines. Depending on the presence of the overhanging features, the process steps can
be used for fabricating anchors for freestanding polymer MEMS structures, which are either electrically connected or isolated from the substrate. The fabrication process is based on the fabrication process discussed previously. For fabrication of the transmission lines, three masks for anchors, dimples, and first structural layer features are used.

(a) 300 nm of Cr and 100 nm of Au are sputtered on a 500 µm thick Si wafer to create the ground plane. These also serve as the alignment markers during the SU-8 exposure.

(b) Polystyrene solution is spun on the wafer and a 6 µm thick polystyrene layer is created. The polystyrene layer dries immediately, and Shipley 1827 photoresist is spun on to a thickness of around 6 µm. The wafer is then softbaked in an oven at 100°C.

(c) The wafer is exposed through the anchor mask to define anchors of the microstructures. The photoresist layer is then developed in Microposit MF-319 developer with agitation. The wafer is rinsed and dried for another exposure step.
(d) The wafer is exposed briefly through the dimple mask to expose the photoresist layer to only about 2 µm deep for dimple features. Dimple features are also used around anchors to create overhanging features for electrical isolation. The photoresist layer is again developed in the Microposit MF-319 developer with agitation. The wafer is then rinsed and dried.

(e) The anchor and dimple features are transferred to the polystyrene sacrificial layer through RIE with O\textsubscript{2}. The etching process is complete when the Au layer is revealed through the anchor features. An anchor depth of around 5.5 µm and a dimple depth of around 2 µm are achieved.

(f) Au is etched from the anchor features in aqueous potassium iodide (KI). Alignment markers are created with the Cr layer to overcome the
similar indices of refraction of polystyrene and SU-8 during the subsequent exposure alignment.

(g) MicroChem SU-8 2010 is spun on to a thickness of 10 µm. The wafer is softbaked on a hotplate with ramping from room temperature (20°C) to 95°C at 300°C/hour ramping rate, the temperature is then kept at 95°C for another 30 minutes.

(h) The wafer is exposed through the first structural layer mask. The SU-8 layer is then post-exposure-baked on a hotplate with ramping from room temperature (20°C) to 95°C at 300°C/hour. The temperature is then kept at 95°C for another 15 minutes.
(i) The SU-8 layers are developed in MicroChem SU-8 developer. Then the sacrificial polystyrene layer is stripped in toluene and the structures are released. Isopropyl alcohol (IPA) is used to rinse the wafer and enhance the drying process.

(j) At the end of the fabrication process, 30 nm of Cr and 270 nm of Au are sputtered to coat the microstructures.

In order to test how large the overhanging features need to be, rectangular test structures with various sizes of overhanging features were fabricated and sputtered with 10 nm of chromium and 200 nm of gold. Since the metals were blanket deposited, the wafer would also be coated with chromium and gold. Figure 4.5 and Figure 4.6 show a layout and a photomicrograph of the test structures. The extension of the overhanging features from the anchor vary from 0 µm to 50 µm with (a) 2.5 µm increment. The effectiveness of the overhanging features of different sizes was measured by testing the electrical conductivity between the test structures and the wafer surface. The accuracy of the size of the overhanging features on each side of the rectangles is only as accurate as the alignment is. However, it was founded that all the test structures except the ones without overhanging features showed electrical isolation. First, the result showed that
the alignment was good enough to be within 2.5 μm. If the alignment were off by more than 2.5 μm, one side of the test structure would make electrical connection to the wafer. Also, the overhanging feature size of 2.5 μm, which would be much smaller than what would be recommended for creating overhanging features on top of anchors, was sufficient for achieving electrical isolation.

Figure 4.5. Layout of the test structures with increasing size of overhanging features.

Figure 4.6. Photomicrograph of the structures used for the electrical isolation test.
4.3.4. **Curvature measurement**

Test structures with the new self-assembly mechanism were fabricated to determine the ranges of self-assembled curvatures. A test setup was made to capture images of the test structures edge-on, and the images were analyzed for self-assembled curvature calculations and geometrical parameter extractions. Sets of the test structures were fabricated over various locations on a wafer to determine consistency of the self-assembly mechanism and were compared with the previously studied self-assembly mechanism. The test structures were composed of 1.5 mm long and 200 µm wide cantilevers with the stress-inducing features and manually assembled vertical micro-stages. Figure 4.7 and Figure 4.8 show a layout and a photomicrograph of the curvature test structures attached to the manually assembled vertical stages.

*Figure 4.7. Layout of curvature test structures.*
Self-assembled curvatures with different ratios of bar to bridge lengths were measured. The widths of the bar and bridge structures were kept equal to the width of the test cantilever structures. Figure 4.9 shows the transition of geometrical parameters used on the test structures. The length of the bar structures was increased from 10 \( \mu \text{m} \) to 70 \( \mu \text{m} \), while the length of the bridge structures between the bar structures was decreased from 90 \( \mu \text{m} \) to 30 \( \mu \text{m} \) by 10 \( \mu \text{m} \). A set of a bar structure and a bridge structure can be considered as a pitch for the self-assembly mechanism in Figure 4.3, and the length of a such segment was kept constant at 100 \( \mu \text{m} \). Therefore, only the ratio of bridge length to pitch length was changed.

**Figure 4.8.** A curvature test structure on a manually assembled vertical stage.
Figure 4.9. **Diagrams representing initial and final geometrical parameter variations.**

Figure 4.10 shows a graph representing relationship between area percentages covered by the bridge structures per pitch and measured curvatures together with previously reported curvature data of the self-assembly method only with the stress-inducing bar structures. The graph is accompanied with depictions of the test structures at both ends of the horizontal axis. The data was collected from thirteen sets of test structures over various locations on a test wafer. The measurement errors on curvatures are less than 30 m\(^{-1}\). Most of the inconsistencies seen on the curvatures were from variations during fabrication, such as poor mask contacts. Features in SU-8 may swell due to poor contacts of wafer and Mylar exposure masks. The error bars at each data point represent standard deviations of the measurement data. As can be seen in the graph, the actual bridge lengths were different from the design parameters due to the feature swelling of SU-8.
Figure 4.10.  *Self-assembled curvatures to changing bridge or bar length to pitch length ratios for a constant pitch length of 100 µm.*

As can be seen in Figure 4.10, two distinct ranges of self-assembled curvatures can be obtained by using the two different types of self-assembly method. The self-assembly using only the bar structures provides a lower range of curvatures whereas higher curvatures are obtained by integrating the bridge structures. Long bridge structures with length over 70 µm, which resulted in highest curvatures showed mechanical instability in some cases due to their excessive lengths and large amount of stress induced. Since the thin bridge structures are created with a timed exposure, they would not be as mechanically rigid as normally cured SU-8 structures.

4.4. Microwave Measurements

4.4.1.  *Transmission Lines*

Fabricated millimeter-wave structures suffered from large signal loss due to the transmission line designs and thin metal layers. Figure 4.11 shows photomicrograph of fabricated test transmission lines. However, metal sidewall coverage created due to usage of overhanging structures for electrical isolation increased field intensity around
the transmission lines and resulted in increased loss. The calibration transmission lines of length 3000 µm were fabricated in order to characterize the feed line effect. Figure 4.12 shows the insertion and the return loss of the interconnect, and a maximum insertion loss of 10.5 dB was measured at 65 GHz. For the next iteration of development, lift-off patterning of metal layers was investigated instead of using overhanging structures to pattern transmission lines on a flat substrate and remove the problem of having sidewall metal coverage.

*Figure 4.11. Photomicrograph of transmission line test structures.*
4.4.2. Monopole Antennas

The lower structural layer defines the overall shape of the monopole before assembly. Using the upper structural layer, support bar structures and bridge structures are defined and they are used to curl the overall structure vertical to the substrate. A long exposure is used for defining the support bar structures and a short exposure is used to crosslink only the top portion of the top SU-8 layer between the support bar structures to create the bridge structures. The widths of the tested monopoles were all 200 µm and the lengths were 1250 µm and 1677 µm for monopoles which corresponds to a quarter free-space wavelength at 60 GHz and and 1327 µm for oblique monopoles with a 45° tilt angle. Using the result of the calibration transmission lines and the actual length of the feed lines to the antennas, which is 675 µm, a maximum insertion loss of 3 dB was estimated. Figure 4.13 shows the return and insertion losses of the feed line. Two sets of straight monopoles as shown in Figure 4.14 and one oblique monopole as shown in Figure 4.15 were tested.

Figure 4.12. Insertion and return loss of the 3000 µm transmission lines [62].
Figure 4.13. Transmission characteristics of the 675 µm feedline and the scaled 3000 µm transmission line [63].

Figure 4.14. Photomicrograph of a monopole antenna with a blanket deposited metal layer.
Figure 4.15. **Photomicrograph of an oblique antenna with a blanket deposited metal layer.**

The return loss measurements of six straight and an oblique monopoles are shown in Figure 4.16. Compared to thin monopoles on a finite ground plane reported previously [64], the self-assembled monopoles showed a much larger impedance probably due to the shape of the monopole being strips while the impedance bandwidth increased. The -10 dB impedance bandwidth range was 10-20%. Figure 4.17 shows impedances for some of the straight monopoles and the oblique monopole and the contrast between them.
Figure 4.16. Return loss measurements of tested straight and oblique monopoles. 1-3 are 1677 µm long, the oblique monopole is 1327 µm long and 4-6 are 1250 µm long [63].
Figure 4.17. Measured impedance of the monopole antennas [63].

Due to relatively large size of the probing station and scattering from the intrusive presence of the probing station, radiation pattern measurement of the stand-alone antennas was difficult. A direct measurement of the antenna performance was done by transmitting between a pair of antennas. Two identical 60 GHz straight monopoles on their 1 cm by 1 cm ground planes were separated by 4 cm. Figure 4.18 shows a transmission gain of -50 dB from physical measurement along with simulation obtained from CST (Computer Simulation Technology). The transmission gains are much higher compared to that of planar antennas which is reported to be -55 dB with only an eighth of separation [36].
Figure 4.18. Measured and calculated values for transmission between a pair of 60 GHz vertical monopole antennas [63].

4.5. Summary

Although the fabrication process provides means of building self-assembled on-chip antennas for 60 GHz transmissions, few things need to be improved in the fabrication process to achieve highest possible performance for the antennas. First of all, the exact thickness of the metals on parts of the antennas and quality of the metal coverage under the antenna structures are uncertain. Ideally, the metal layers should be deposited before the self-assembly takes place to control the thickness and the placement of metals with precision. The separate metallization under the antenna structures ensures full coverage of metal and should reduce dielectric loses. Secondly, the transmission lines need to be made from a patterned metal layer to eliminate the sidewall metal coverage and efficiency. Lastly, the distance between the silicon substrate and the antennas along with the transmission lines need to be increased. The sacrificial layer provided the gap between the silicon substrate and the antennas, but the gap should be much greater than a typical sacrificial layer could provide.
5. Modification of Multi-user Polymer MEMS Process for Improved 60 GHz Antennas

5.1. ProLIFT as a Sacrificial Material

5.1.1. Introduction

Previously, thicknesses of deposited metals were kept very low in order to prevent possible contact of the signal lines to the ground plane. If more metal was deposited on the wafer, the distance between the ground plane and the transmission line would decrease as the low point of the metal on the transmission line would stay the same and the height of the ground plane would increase as can be visualized from Figure 4.4. A thicker polystyrene sacrificial layer was attempted for the fabrication, but due to stress build-up of using a much thicker layer, cracks were unavoidable hindering it to be successfully used as a sacrificial layer. When SU-8 features were defined over large enough cracks of the sacrificial layer, the SU-8 in the cracks would effectively become unwanted anchors and prevent self-assembly.

Also, choosing arbitrarily large sizes for the overhanging features is not possible since the width of the transmission lines is determined by the 50-ohms characteristic impedance requirement. The width of the transmission lines and the size of the overhanging features over their anchors were close to fabrication limit due to capability of the mask aligner and mask resolution in the cleanroom. Therefore, only a single skin depth of metals at 60 GHz was deposited, but this resulted in increased loss along transmission lines. Another issue of the previously presented fabrication was that sidewall coverage of metals on the overhanging features of transmission lines was affecting the performance of the transmission lines. The sidewall coverage of metals was unavoidable due to the blanket deposition of the metals with sputtering process. Because the antenna structures were already released, the blanket deposition was the only method for metallization of the antennas. Two features needed to be addressed
were the ability to pattern metal layers and tolerance to thicker metal layers, which would be greater than the skin depth at 60 GHz. A new fabrication method was proposed, which could incorporate patterned metal layers and ability to deposit about 1 µm thick metals all around self-assembled antenna structures.

One of the reasons that initiated the proposal of a new fabrication process was several months of downtime RIE system in the cleanroom. The usage of RIE is critical for the previously used fabrication process for patterning of the polystyrene sacrificial layer. After the anchor and dimple features were patterned on the thick photoresist layer on top of the sacrificial polystyrene layer, the features were transferred to the polystyrene layer with RIE. There were only few options for eliminating the RIE processing from the fabrication, and they were replacing the polystyrene sacrificial layer with either spin-on-glass or ProLIFT. These two materials can be patterned without the usage of RIE and can withstand the application of SU-8 and its developer. Another benefit of these materials is that they have high glass-transition temperatures compared to polystyrene and can safely be sputtered with metal without surface deformation issues. This advantage allows deposition of metals underneath the self-assembled structures by first sputtering metals on the sacrificial layer and then curing the first structural layer. When the sacrificial layer is removed, the metal layer would remain under the released structures providing that the metal has good adhesion to the structural material used.

Honeywell Accuglass 512B spin-on glass was tested for viability of using it as a sacrificial material. One of the issues of using the spin-on glass was that it was not possible to spin thicker than 1 µm. When multiple layers of spin-on glass were used to create a thick sacrificial layer, cracks were formed within the sacrificial layer, which could create unwanted anchors. With such a thin sacrificial layer, patterning of dimple features would become very challenging. Dimples are placed under freestanding structures in many types of microstructures to prevent stiction, which happens when surface adhesion forces are higher than the mechanical restoring forces of microstructures. When dimples are placed underneath microstructures, the contact area of the microstructures to the substrate decreases reducing the surface adhesion force and prevents stiction. For the self-assembled SU-8 microstructures, 2 µm thick dimple features were placed by using partial exposure of dimple features to photoresist and developing the photoresist to
create tiny holes. Then the holes were transferred to the polystyrene sacrificial layer with RIE and when SU-8 photoresist was spun over the sacrificial layer the holes were filled with SU-8, creating dimple features under fabricated SU-8 structures.

If holes for the dimples are to be patterned on the spin-on glass layer, photoresist need to be used as an etch mask and the etching should be timed to make sure the etchant does not go through the whole thickness of the spin-on glass layer. An etching test was performed for the dimple features. After 900 nm of spin-on glass was spun on and cured according to the manufacturer’s recommendations, a thin photoresist layer was spun on using Shipley 1813 and softbaked. After exposing and developing test dimple features on the photoresist layer, the spin-on glass was etched using buffered HF solution. The challenge was finding the right amount of time needed to etch about half the thickness of the spin-on glass layer, which is about 500 nm. The biggest issue with the timed etch was that not all areas of a wafer were etching at the same rate even when a whole wafer was submerged in a bucket of buffered HF with slight agitation. Some areas would have etched all the way through the spin-on glass layer while other areas were etched only slightly. The difference in etch rates at different locations would be probably minimal, but the effect is heightened due to the thinness of the spin-on glass layer.

The second issue was the curing temperature of the spin-on glass layer. Suggested final curing temperature for the spin-on glass is 350°C. Since spin-on glass layer itself is not a thick enough sacrificial layer, transmission lines need to be patterned on a raised dielectric substrate such as a thick SU-8 layer. Thick dielectric layer is necessary to provide enough distance between the low resistivity substrate and the transmission lines. When looking for a dielectric layer with thickness of tens of micrometers, there was no suitable dielectric material, which could withstand the high curing temperature of the spin-on glass within the available fabrication processes.

ProLIFT on the other hand can be spun to a 6 µm thick layer. This allows easier timing for etching holes for creating dimple features. ProLIFT can be etched easily with tetramethyl ammonium hydroxide (TMAH) based developers such as positive photoresist developer Microposit MF-319. Since greater thickness of the sacrificial layer would provide larger margin of error for timing of ProLIFT etching, spinning multiple layers of
ProLIFT was tested. However, if a layer of ProLIFT with a thickness larger than recommended by the manufacturer was deposited, the layer could be cracked during baking and create unwanted anchors. In order to pattern a ProLIFT layer, the positive photoresist Shipley 1813 was used for creating an etch mask on top of the ProLIFT layer. The anchor and dimple patterns were exposed and the photoresist layer was developed in MF-319. Since MF-319 etches the underlying ProLIFT as well, the wafer was left in the developer for longer period time to pattern the ProLIFT layer. The ProLIFT layer goes through isotropic etching and etching should be timed accurately to minimize undercut. When ProLIFT patterning was completed, the photoresist can be removed in a propylene glycol methyl ether acetate (PGMEA) bath which does not affect ProLIFT.

Another benefit of ProLIFT is that curing temperature of ProLIFT is very close to hardbaking temperature of SU-8, which makes ProLIFT compatible with already existing SU-8 layers. When SU-8 is hardbaked before a ProLIFT layer is spun on, SU-8 structure will not be affected by following ProLIFT processes. Thus, ProLIFT can be used as both a sacrificial layer and a layer for metal patterning. Once cured, ProLIFT can withstand temperatures above 300°C and is resistant to SU-8 developers, which is also PGMEA. Both properties combined allow development of the SU-8 layers without releasing structures and hardbaking of SU-8 structures. When metals are sputtered on the wafer without releasing the self-assembled structures, the amount of metal placed on the structures would be even. Thus, the self-assembled antennas would have even thickness of metals throughout the lengths, preventing any unexpected performance degradation. The previous metal deposition method, where metals were applied after releasing structures, did not guarantee that parts of the structures which were vertical to the wafer would have expected thickness of metal as the metals are deposited perpendicular to the wafer surface.

Another benefit of keeping structures on a sacrificial layer is that metal can be deposited and patterned on top of developed SU-8 structures. When the structures are not released, photoresist or ProLIFT can be easily spun on the wafer for patterning metal layers. If the structures are released, photoresist or ProLIFT cannot be spun on without breaking the released structures, and contact alignment would not be possible as well. One might think that deposition of metals on top of undeveloped SU-8 could be used for coating freestanding SU-8 structures, but sputtering may cause crosslinking of SU-8 on
unexposed areas of an SU-8 layer and this method does not allow deposition of metals on sidewalls of self-assembling SU-8 structures connecting the top and bottom metal layers.

One method of patterning metal is using ProLIFT as a lift-off layer. The lift-off process involves patterning of a lift-off layer using a photoresist and a photoresist developer, deposition of metal, and removal of the lift-off layer as shown in Figure 5.1. Patterned metal is left behind when the lift-off layer is removed. The target was to pattern 1 µm thick metal layer, which would be about four times the skin depth at 60 GHz. Therefore, ProLIFT needed to be spun thicker than 1 µm. The positive photoresist used to pattern ProLIFT was also used as an overhanging structure to separate the metal. For the fabrication process, copper was used instead of gold to lower the prototype fabrication cost.
**Figure 5.1.** Lift-off processing with the ProLIFT and a photoresist on top as a mask layer.

Figure 5.2 shows the cross-sectional view of a self-assembling cantilever from the proposed fabrication process. The dashed line indicates the final form of the self-assembly.
5.1.2. **Process Description**

(a) 50 nm of chromium and 1 µm of copper are sputtered on a RCA cleaned wafer to serve as the ground plane.

(b) ProLIFT 100-24 is spun on the wafer at 2000 rpm for 90 seconds and a 6 µm thick layer is made. The wafer is then baked on a hotplate from 20°C to 220°C with ramping at 300°C/hour, baked for another 15 minutes and cooled naturally.
(c) Positive photoresist layer Shipley 1813 is spun at 4000 rpm for 30 seconds. The layer is softbaked in an oven at 100°C for 15 minutes.

(d) The wafer is exposed through the anchor mask for 30 seconds to define anchors of microstructures. The photoresist layer is then developed in Microposit MF-319 developer for 1 minute and 30 seconds with agitation. During the development the ProLIFT layer is also patterned. The wafer is rinsed and dried for another exposure step.

(e) Dimple and metal features under structures are exposed for 30 seconds. The wafer is developed in Microposit MF-319 for 35 seconds etching into half of the ProLIFT layer’s thickness.
(f) 1 µm of copper and then 50 nm of chromium are sputtered.

(g) Photoresist is stripped in an acetone bath.

(h) MicroChem SU-8 2010 is spun on 10 µm thick at 3500 rpm for 30 seconds. The wafer is softbaked on a hotplate with ramping from room temperature (20°C) to 95°C at 300°C/hour ramping rate and then the temperature is kept at 95°C for another 30 minutes.

(i) The wafer is exposed for 50 seconds through the first structural layer mask. The first SU-8 layer features are overexposed for complete
crosslinking before the second SU-8 layer is applied. The SU-8 layer is then post-exposure-baked on a hotplate with ramping from room temperature (20°C) to 95°C at 300°C/hour and then the temperature is kept at 95°C for another 15 minutes.

(j) The second SU-8 layer is spun on 30 µm thick at 1000 rpm for 30 seconds. A thicker layer is used to increase relative stiffness with defined support bar structures and leave enough room for bridge structures to be defined with a brief exposure. The wafer is softbaked on a hotplate at 95°C for 30 minutes.

(k) The wafer is exposed for 60 seconds through the mask for support structures. Overexposure is desired to fully crosslink the support bar structures and to ensure good adhesion to the first structural layer.
(l) The wafer is exposed for 10 seconds through the mask for bridge structures. Generally, the bridge features on the mask cover both support bars and areas between support bars to ensure continuity of the bridge structures.

(m) The SU-8 layers are developed in MicroChem SU-8 developer. SU-8 is hard baked at 200°C for 15 minutes.

(n) ProLIFT 100-24 is spun on the wafer at 3000 rpm for 90 seconds and a 4 µm thick layer is made. The wafer is then baked on a hotplate from 20°C to 220°C with ramping at 300°C/hour, baked for another 15 minutes and cooled naturally.
(o) Positive photoresist layer Shipley 1813 is spun at 4000 rpm for 30 seconds. The layer is softbaked in an oven at 100°C for 15 minutes.

(p) The wafer is exposed through the mask for top metal features for 30 seconds. The photoresist layer is then developed in Microposit MF-319 developer for 1 minute with agitation. During the development the ProLIFT layer is also patterned.

(q) 50 nm of chromium and 1 µm of copper are sputtered.
5.1.3. **Fabrication Result**

Different methods have been attempted to partially develop ProLIFT in MF-319 to create dimple features. With recommended exposure dosage of the positive photoresist, exposed areas of the photoresist layer developed too quickly and MF-319 developed through ProLIFT within 20 seconds. Therefore, partial development of ProLIFT to a desired depth was difficult to achieve with repeatable success. In order to slow down the development, diluted MF-319 with deionized water was attempted. At least 50% dilution was required to achieve significant reduction in development speed. However, the dilution resulted in inconsistent development of photoresist layer. Another method of slowing down the development was exposing the photoresist with lower energy. The exposure time was reduced to a third, and repeatable partial development of ProLIFT was achieved with 30 seconds of development in MF-319.

For the prototype fabrication, the resulting self-assembled structures showed curvature slightly in the opposite direction as would be expected from the fabrication with polystyrene sacrificial layer (Figure 5.3). Instead of curving severely out of the plane, the structures were curly slight into the plane. Which meant that no stress was developed between the crosslinking of the first structural layer and the second structural layer. As SU-8 shrinks in volume after it is crosslinked, the second structural layer must had shrunk in volume together with the first structural layer, which led to a hypothesis that the first structural layer was held taut by the ProLIFT sacrificial layer even after crosslinking.
because of a high glass transition temperature of ProLIFT. Therefore, when the second structural layer was crosslinked and the freestanding structures were released, the first and the second structural layers were free to shrink and relieve built up stress together resulting in small stress differential between the layers both before and after the removal of the sacrificial layer. For the previous fabrication method where polystyrene was used for the sacrificial layer, the first structural layer must have been free of stress before the second structural layer was applied due to its low glass transition temperature of the polystyrene. During the post exposure-baking step of the first structural layer, the polystyrene sacrificial layer must had become soft at the baking temperature and allowed SU-8 to shrink almost at its natural rate and become free of stress. On the other hand, stress was developed between the first and the second SU-8 structural layers, as glass transition temperature of SU-8 is much higher than its baking temperatures.

![Photomicrograph of fabricated cantilevers.](image)

**Figure 5.3. Photomicrograph of fabricated cantilevers.**

In order to prove the hypothesis, another fabrication was performed where only the first structural layer was hardbaked and both structural layers were developed at the end of the process. The first structural layer would shrink more than the second structural layer and the residual stress between the first structural layer and the sacrificial layer would be higher. As the bottom layer would be shrinking at higher rate than the top layer, the structures should curl towards the wafer at a higher rate.
compared to the previous fabrication. The fabrication result showed much higher curvature towards the substrate than before and proved that the issue with the self-assembly was indeed due to the stress build-up between the sacrificial layer and the first structural layer (Figure 5.4). In order to self-assemble structures using the stress build-up between two structural layers, a material with minimal residual stress is needed for the first structural layer.

![Figure 5.4](image)

**Figure 5.4.** Photomicrograph of self-assembled cantilevers fabricated with the hardbaked bottom SU-8 layer.

### 5.2. PI only process

#### 5.2.1. Introduction

In order to remove the stress buildup of the first structural layer, another structural material with low stress was used. Polyimide has been used previously in many MEMS fabrications for structural and for passivation applications. The advantageous properties of polyimide are very high flexural strength and low residual stress after fabrication. The high flexural strength makes polyimide microstructures resistant to breakages. Polyimide solution PI-2610 from HD Microsystems particularly has very low residual stress and it would be a very good candidate for replacing the first
structural layer of the self-assembled structures. The polyimide would also allow patterning of metal layers both above and below structures, as both ProLIFT and the patterned polyimide layer are compatible with high temperature during metal depositions. For patterning of the polyimide layer, a metal layer was deposited on top and patterned to serve as a masking layer during RIE.

For making stress-inducing bridge structures, two different methods could be used to create the bridge structures. One method was to pattern a ProLIFT layer to create the gap between the first and the second structural SU-8 layers. The other method would be similar to previously used fabrication method where a thick second structural layer and a timed exposure were used to create the bridge structures. The first method would be ideal as the thickness of the second structural layer could be minimized and provide much better alignment and exposure for patterning metals on top.

Test fabrications were performed in order to determine the feasibility of using ProLIFT for defining the bar and bridge structures for self-assembly. After the first SU-8 structural layer was exposed and post exposure-baked, it was developed in a SU-8 developer bath for 5 minutes. Then the SU-8 structures were hardbaked at 200°C for 15 minutes. A ProLIFT layer was spun on using ProLIFT 100-20 at 2000 rpm for 90 seconds to achieve 2 µm thickness. With a positive photoresist etch mask was created using the exposure mask for bar structures to pattern via-holes between the first and the second SU-8 structural layers. However, wet etching was found to be not suitable for patterning of the via-holes because accuracy of the self-assembly was affected by the dimensional change of via holes. MF-319 etches ProLIFT isotropically thus the sizes of the via-holes would increase with time. Increased via-holes would translate into reduced length of the bridge structures, which would result in lower self-assembled curvatures. Also, the rate of the isotropic etching was very inconsistent among the via-holes. In order to accurately pattern the via-holes RIE should be used instead of wet etching. Since RIE is very directional vertically, the patterns in the photoresist layer would be accurately transferred to the ProLIFT layer.

5.2.2. **Process Description**

The following processing steps fabricated the bridge structures using partial exposure of thick SU-8 layer. For the first structural layer, low stress PI-2610 was used.
(a) 50 nm of chromium and 1 µm of copper are sputtered on a RCA cleaned wafer to serve as the ground plane.

(b) ProLIFT 100-24 is spun on the wafer at 2000 rpm for 90 seconds and a 6 µm thick layer is made. The wafer is then baked on a hotplate from 20°C to 220°C with ramping at 300°C/hour, baked for another 15 minutes and cooled naturally.

(c) Positive photoresist layer Shipley 1813 is spun at 4000 rpm for 30 seconds. The layer is softbaked in an oven at 100°C for 15 minutes.

(d) The wafer is exposed through the anchor mask for 30 seconds to define anchors of microstructures. The photoresist layer is then developed in Microposit MF-319 developer for 1 minute and 30
seconds with agitation. During the development the ProLIFT layer is also patterned. The wafer is rinsed and dried for another exposure step.

(e) Dimple and metal features under structures are exposed for 30 seconds. The wafer is developed in Microposit MF-319 for 35 seconds etching into half of the ProLIFT layer’s thickness.

(f) 1 µm of copper and 50 nm of chromium are sputtered

(g) Photoresist is stripped in an acetone bath.
(h) Polyimide PI-2611 is spun on at 5000 rpm for 30 seconds and bake on hotplate at 150°C for 3 minutes. Then, the hotplate temperature is raised from 150°C to 300°C at 240°C/hour and held at the final temperature for 30 minutes.

(i) 300 nm of aluminium is sputtered for creating RIE masking layer.

(j) Photoresist Shipley 1813 is spun at 4000 rpm for 30 seconds and softbaked at 100°C for 15 minutes.

(k) RIE masking features are exposed and the photoresist layer is developed in MF-319.
(l) Exposed part of aluminium layer is etched away in aluminium etchant type D from Transene.

(m) Polyimide layer is patterned using RIE with 80 sccm O₂, 20 sccm CF₄, 300 W, and 170 mtorr. The etching takes about 17 minutes.

(n) The second SU-8 layer is spun on 30 µm thick at 1000 rpm for 30 seconds. A thicker layer is used to increase relative stiffness with defined support bar structures and leave enough room for bridge structures to be defined with a brief exposure. The wafer is softbaked on a hotplate at 95°C for 30 minutes.
The wafer is exposed for 60 seconds through the mask for support structures. Overexposure is desired to fully crosslink the support bar structures and to ensure good adhesion to the first structural layer.

The wafer is exposed for 10 seconds through the mask for bridge structures. Generally, the bridge features on the mask cover both support bars and areas between support bars to ensure continuity of the bridge structures.
(q) The SU-8 layers are developed in MicroChem SU-8 developer. SU-8 is hard baked at 200°C for 15 minutes.

(r) ProLIFT 100-24 is spun on the wafer at 3000 rpm for 90 seconds and a 4 µm thick layer is made. The wafer is then baked on a hotplate from 20°C to 220°C with ramping at 300°C/hour, baked for another 15 minutes and cooled naturally.

(s) Positive photoresist layer Shipley 1813 is spun at 4000 rpm for 30 seconds. The layer is softbaked in an oven at 100°C for 15 minutes.
(t) The wafer is exposed through the mask for top metal features for 30 seconds. The photoresist layer is then developed in Microposit MF-319 developer for 1 minute with agitation. During the development the ProLIFT layer is also patterned.

(u) 50 nm of chromium and 1 \( \mu \text{m} \) of copper are sputtered.

(v) Top metal layers are patterned by lift-off process in an acetone bath. The structures are released in Microposit MF-319 developer.
Another processing steps were used concurrently to determine to if ProLIFT can be effectively used for defining bridge structures, which would yield better defined width and thickness for bridge structures. Instead of partial exposure of the thick second SU-8 structural layer, ProLIFT would provide via-holes for bar structures and gap between the first structural layer and the bridge structures.

(a) 50 nm of chromium and 1 µm of copper are sputtered on a RCA cleaned wafer to serve as the ground plane.

(b) ProLIFT 100-24 is spun on the wafer at 2000 rpm for 90 seconds and a 6 µm thick layer is made. The wafer is then baked on a hotplate from 20°C to 220°C with ramping at 300°C/hour, baked for another 15 minutes and cooled naturally.

(c) Positive photoresist layer Shipley 1813 is spun at 4000 rpm for 30 seconds. The layer is softbaked in an oven at 100°C for 15 minutes.

(d) The wafer is exposed through the anchor mask for 30 seconds to define anchors of microstructures. The photoresist layer is then developed in Microposit MF-319 developer for 1 minute and 30 seconds with agitation. During the development the ProLIFT layer is also patterned. The wafer is rinsed and dried for another exposure step.

(e) Dimple and metal features under structures are exposed for 30 seconds. The wafer is developed in Microposit MF-319 for 35 seconds etching into half of the ProLIFT layer's thickness.

(f) 1 µm of copper and 50 nm of chromium are sputtered

(g) Photoresist is stripped in an acetone bath.

(h) Polyimide PI-2611 is spun on at 5000 rpm for 30 seconds and bake on hotplate at 150°C for 3 minutes. Then, the hotplate temperature is raised from 150°C to 300°C at 240°C/hour and held at the final temperature for 30 minutes.

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(i) 300 nm of aluminium is sputtered for creating RIE masking layer.

(j) Photoresist Shipley 1813 is spun at 4000 rpm for 30 seconds and softbaked at 100°C for 15 minutes.

(k) RIE masking features are exposed and the photoresist layer is developed in MF-319.

(l) Exposed part of aluminium layer is etched away in aluminium etchant type D from Transene.

(m) Polyimide layer is patterned using RIE with 80 sccm O₂, 20 sccm CF₄, 300 W, and 170 mTorr. The etching takes about 17 minutes.

(n) ProLIFT 100-20 is spun on the wafer at 2000 rpm for 90 seconds and a 2 µm thick layer is made. The wafer is then baked on a hotplate from 20°C to 220°C with ramping at 300°C/hour, baked for another 15 minutes and cooled naturally.

(o) Positive photoresist layer Shipley 1827 is spun at 1500 rpm for 30 seconds. The layer is softbaked in an oven at 100°C for 15 minutes.

(p) The wafer is exposed through the mask for support bar features for 7 seconds. The photoresist layer is then developed in Microposit MF-319 developer for 15 seconds with agitation. Short exposure is used not to fully expose the photoresist in order to make sure that the ProLIFT layer is not etched by the Microposit MF-319 developer.

(q) The via-hole features are transferred to the ProLIFT layer using RIE with 80 sccm O₂, 20 sccm CF₄, 100 W of power, and 100 mTorr pressure for 18 minutes.

(r) The second SU-8 layer is spun on 10 µm thick at 3500 rpm for 30 seconds. The wafer is softbaked on a hotplate at 95°C for 30 minutes.
(s) The wafer is exposed for 50 seconds through the mask for support and bridge structures. Overexposure is desired to fully crosslink the SU-8 layer to ensure good adhesion to the first structural layer.

(t) The SU-8 layers are developed in MicroChem SU-8 developer. SU-8 is hard baked at 200°C for 15 minutes.

(u) ProLIFT 100-24 is spun on the wafer at 3000 rpm for 90 seconds and a 4 µm thick layer is made. The wafer is then baked on a hotplate from 20°C to 220°C with ramping at 300°C/hour, baked for another 15 minutes and cooled naturally.

(v) Positive photoresist layer Shipley 1813 is spun at 4000 rpm for 30 seconds. The layer is softbaked in an oven at 100°C for 15 minutes.

(w) The wafer is exposed through the mask for top metal features for 30 seconds. The photoresist layer is then developed in Microposit MF-319 developer for 1 minute with agitation. During the development the ProLIFT layer is also patterned.

(x) 50 nm of chromium and 1 µm of copper are sputtered.

(y) Top metal layers are patterned by lift-off process in an acetone bath. The structures are released in Microposit MF-319 developer.

Figure 5.5 shows an example of the fabricated structures using the process with a polyimide structural layer. As can be seen in the figure, the self-assembled structure curled up backing up the hypothesis made previously.
5.2.3. **Fabrication Result**

The usage of the low stress polyimide would allow us to create self-assembling structures surrounded with patterned metal layers. However, the fabricated prototype structures were highly sensitive to surrounding temperatures. The difference in coefficient of thermal expansion (CTE) of the polyimide and SU-8 caused curvature to change depending on the temperature. Figure 5.6 shows changed curvature of the same structure at a slightly higher temperature by placing a fingertip near the structure on the wafer. This high temperature sensitivity would be unsuitable for creating three-dimensionally configured antennas, although the feature can be used effectively for creating tunable antennas and transducers.
Another issue with using the polyimide as the first structural layer was that although the structures were resilient to breakage, the layer was too thin to be useful for fabricating large freestanding structures. Even with the presence of dimple features, the polyimide layer was too flexible and deformed itself to flatten out around the dimple features, causing stiction issues with most of the freestanding structures.

5.3. Usage of ProLIFT for Limiting Blanket Metal Deposited Areas

5.3.1. Introduction

From the previous fabrications, the importance of minimal residual stress in the first structural layer was found for accomplishing the self-assembly of microstructures. Polyimide, which was used for the first structural layer because of its low stress properties, was not found to be suitable for making self-assembled microstructures. Compared to polyimide, SU-8 still is a better choice because of simplicity of fabricating structures with it. Also, for the purpose of creating fixed three-dimensional antennas, usage of a single structural material or two materials with same coefficient of thermal
expansion is important. This can be achieved by using SU-8 for both structural layers as previously done. However, there were two issues that need to be solved, which were patterned metal layers and release of stress of the first structural layer. One way to remove stress of the first structural layer was to use a material for the sacrificial layer with a low glass transition temperature. If the glass transition temperature is low enough that the material becomes soft at SU-8’s curing temperature, minimal stress would develop between the SU-8 and the sacrificial layer. One such material is polystyrene, which was used previously.

During the development of a new fabrication method, a compromise was necessary as sputtering of metals on polystyrene is not ideal due to its low glass transition temperature. The most important goal of the new fabrication process was the ability to pattern transmission lines on a thick substrate. Patterned metal layers were necessary for transmission lines to improve performance by eliminating the sidewall metal coverage on transmission lines. On the other hand, the sputtering of metals on the sacrificial layer was omitted. Metals would be blanket deposited on the wafer to coat the self-assembled structures instead. The separation of metals for transmission lines is achieved with lift-off profile fabricated using ProLIFT. As the electrical isolation of transmission lines is achieved by lift-off profiles, thickness of metal that can deposited is determined by the thickness of ProLIFT layer. With the ability to spin on up to 6 µm thick ProLIFT layers, very thick layer of metal can be blanket deposited which should allow enough thickness of metal to land on most of the surfaces of self-assembled microstructures. To provide the separation of the transmission lines from the silicon substrate, a very thick dielectric layer was created under the transmission lines using an SU-8 photoresist.

Antenna structures would be deposited with a thick layer of metal at the end of fabrication to coat all-around the structures. After releasing the structures, blanket metal deposition over the wafer would coat self-assembled structures and leave transmission lines features with the lift-off profiles. As the last step, the lift-off profiles could be removed in ProLIFT developer such as MF-319 leaving only metal coated self-assembled structures and patterned transmission lines.
A test was performed to determine the compatibility of polystyrene as a sacrificial layer with ProLIFT lift-off layer. The polystyrene solution was prepared with high molecular density polystyrene beads dissolved in toluene. The polystyrene solution dries fast enough that it would interact with underlying layer only minimally. Therefore, a key compatibility test was to see if ProLIFT would be affected by releasing solvent, toluene. ProLIFT was patterned with photoresist and then submerged in toluene solution for 10 minutes. Typical release process takes about 5 minutes, and the compatibility test should indicate if the lift-off profiles would withstand the release process. After the test, features of the ProLIFT layer did not show any change. Positive photoresist is usually used as an etch mask for patterning ProLIFT. For this fabrication process, however, an SU-8 layer is used instead because during the fabrication the ProLIFT etch mask layer need to be exposed to SU-8 developer. SU-8 developer dissolves polystyrene and when all the unexposed areas of SU-8 layers are developed during the development step of the SU-8 structures, the SU-8 developer could etch through the sacrificial layer very fast and also start to etch the ProLIFT mask if the positive photoresist was used instead of SU-8.

5.3.2. Process Description

(a) 50 nm of chromium, 1 µm of copper, and 50 nm of chromium are sputtered in order on a RCA cleaned wafer to serve as the ground plane.

(b) Spin on MicroChem SU-8 3050 at 3000 rpm for 30 seconds to achieve 50 µm thick insulating layer. The wafer is softbaked on a hotplate with ramping from room temperature (20°C) to 95°C at 300°C/hour ramping rate and then the temperature is kept at 95°C for another 30 minutes.
(c) Wafer is exposed through a mask that defines polymer substrates for 60 seconds. The SU-8 layer is then post-exposure-baked on a hotplate with ramping from room temperature (20°C) to 95°C at 300°C/hour and then the temperature is kept at 95°C for another 15 minutes.

(d) The SU-8 layer is developed in MicroChem SU-8 developer for about 3 minutes. SU-8 structures are then hardbaked on a hotplate with ramping from room temperature (20°C) to 200°C at 300°C/hour and then the temperature is kept at 200°C for another 15 minutes.

(e) ProLIFT 100-20 is spun on the wafer at 1500 rpm for 90 seconds and a 3 µm thick layer is made. The wafer is then baked on a hotplate from room temperature (20°C) to 200°C with ramping at 300°C/hour, baked for another 10 minutes and cooled naturally.
(f) Spin on MicroChem SU-8 2002 at 3000 rpm for 30 seconds for 2 µm thick layer. The wafer is softbaked on a hotplate with ramping from room temperature (20°C) to 95°C at 300°C/hour ramping rate and then the temperature is kept at 95°C for another 30 minutes.

(g) Lift-off profiles are defined with 30 seconds exposure. The SU-8 layer is then post-exposure-baked on a hotplate with ramping from room temperature (20°C) to 95°C at 300°C/hour and then the temperature is kept at 95°C for another 15 minutes.

(h) Exposed areas of ProLIFT are etched in MF-319 solution.
(i) 20 wt% polystyrene solution is spun on the wafer at 1500 rpm for 30 seconds and a 6 µm thick polystyrene layer is made. The polystyrene layer dries immediately.

(j) Shipley 1827 photoresist is spun at 1500 rpm for 30 seconds for thickness of around 6 µm. The wafer is then softbaked in an oven at 100°C for 15 minutes.

(k) The wafer is exposed through the anchor mask for 80 seconds to define anchors of microstructures. The photoresist layer is then developed in Microposit MF-319 developer for 3 minutes with agitation. The wafer is rinsed and dried for another exposure step.
The wafer is exposed through the dimple mask for 14 seconds to expose the photoresist to only about 2 µm deep for dimple features. Dimple features are used to reduce stiction of overhanging microstructures to the substrate. The photoresist layer is again developed in Microposit MF-319 developer for 3 minutes with agitation. The wafer is then rinsed and dried.

The anchor and dimple features are transferred to the polystyrene layer through RIE for 38 minutes with O₂ plasma at 40 sccm of O₂ flow rate, 100 mtorr of pressure, and 150 W of power. The etching process is complete when the metal layer is revealed through the anchor features. An anchor depth of around 5.5 µm and a dimple depth of around 2 µm are achieved.
(n) MicroChem SU-8 2010 is spun on to a 10 µm thickness at 3500 rpm for 30 seconds. The wafer is softbaked on a hotplate with ramping from room temperature (20°C) to 95°C at 300°C/hour ramping rate and then the temperature is kept at 95°C for another 30 minutes.

(o) The wafer is exposed for 45 seconds through the first structural layer mask. The first SU-8 layer features are overexposed for complete crosslinking before the second SU-8 layer is applied. The SU-8 layer is then post-exposure-baked on a hotplate with ramping from room temperature (20°C) to 95°C at 300°C/hour and then the temperature is kept at 95°C for another 15 minutes.

(p) The second SU-8 layer is spun on to a 21 µm thickness at 1000 rpm for 30 seconds. A thicker layer is used to increase relative stiffness with defined support bar structures and leave enough room for bridge structures to be defined with a brief exposure. The wafer is softbaked on a hotplate at 95°C for 30 minutes.
(q) The wafer is exposed for 60 seconds through the mask for support structures. Overexposure is desired to fully crosslink the support bar structures and to ensure good adhesion to the first structural layer.

(r) The wafer is exposed for 8.5 seconds through the mask for bridge structures. Generally, the bridge features on the mask cover both support bars and areas between support bars to ensure continuity of the bridge structures.

(s) The SU-8 layers are developed in MicroChem SU-8 developer.
The sacrificial polystyrene layer is stripped in toluene and the structures are release for self-assembly.

Isopropyl alcohol (IPA) is used to rinse the wafer and enhance drying process. As solvents are released from the structures, the self-assembly completes. The released structures self-assemble into predefined shapes.

50 nm of chromium and 1 µm of copper are sputtered.
Metals are removed with lift-off structures when they are released in MF-319.

5.3.3. Fabrication Result

A thick SU-8 layer was spun-on and patterned to be used as a thick dielectric layer for transmission lines. The idea of placing the thick dielectric layer is to place the transmission lines and antennas away from the low resistivity substrate and minimize electromagnetic loss into the substrate. Using a thick dielectric is a better choice for mass fabrication of these antennas compared to automated assembly solution where each antenna and transmission line would be floating over an air gap above the chip surface. If the assembly method was used, each chip has to be assembled serially, while a batch processing of thousands of chips per wafer is possible with the thick dielectric layer. Dielectric property of SU-8 would not be as good as air or vacuum, but the slight disadvantage would be negligible when the self-assembly is used together.
One issue of fabricating thick SU-8 structures is the stress build-up during the crosslinking of the polymer. As expected, thicker SU-8 structures create higher stresses on the surface below, and depending on the type of surface that SU-8 structures are placed on, the stress under the SU-8 structures might lead to delamination of the structures off the substrate. From several test fabrications, it was found that most of the structures were peeling from the edges of the structures where most of the stress would be concentrated. One solution to the delamination problem is to use a thin layer of SU-8 under the thick SU-8 structures, which would provide much higher adhesion to the SU-8 structures compared to either silicon or any types of metal and distribute the stress more evenly throughout the surface. The thin layer of SU-8 would be coated over the whole surface of the wafer and would be able to distribute evenly the small built-up stress from its 5 µm thick layer.

The issue which made this process unsuitable for making self-assembled antennas was the usage of SU-8 as an etch mask which remained stuck on the substrate surface even after the ProLIFT had all been etched away. Because of the fact that the etch mask for lift-off profiles need to withstand the following process steps, a thin SU-8 layer was used. But as ProLIFT was dissolved away, the thin SU-8 structures closed themselves to the substrate surface, requiring ultrasonic agitation to lift the SU-8 structures off. Ultrasonic agitation is too strong for released SU-8 structures and cannot be used at the end of the process. While looking for another method of fabricating self-assembled antennas with patterned transmission lines on a thick dielectric substrate, a test was performed how polystyrene would actually react to sputtering of metals.

The copper layer used as a ground plane was also causing delamination issues due to stress build-up from thick SU-8 layers. While some of the thick SU-8 structures were peeled off from the copper layers, both copper and SU-8 were delaminated together on some other areas. Aluminum was tested to replace copper for the fabrication process, but sputtered aluminum was also found to be incompatible with MF-319 photoresist developer. When the aluminum layer was exposed to MF-319 during ProLIFT removal process steps, the aluminum layer was slowly etched away. MF-319 contains TMAH, which chemically attacks aluminum.
While aluminum oxide layer can be grown on top of the aluminum layer in an ozone asher to prevent the chemical reaction with MF-319 [65], a simpler solution to the problem is using gold at least for the purpose of developing prototype antennas. All the fabrication steps will be performed post to CMOS fabrication processes and a passivation layer such as polyimide can be used to protect CMOS circuitry from gold. Via holes can be placed on the passivation layer in order to make electrical connection between CMOS circuitry and the self-assembled antennas.

5.4. **SU-8 Fabrication with Patterned Metals and Polystyrene as a Sacrificial layer**

5.4.1. **Introduction**

Because of the loss of advantage of using the lift-off profiles for patterning blanket deposited metals, a slightly more elaborate process of patterning metal layers using positive photoresists was incorporated into the fabrication process. The advantage of using this method is even coating of entire surface of SU-8 structures with metals. From an earlier work on the development of the multi-user polymer MEMS process, it was found that the metal sputtering on a spun-on polystyrene layer on top of a wafer would be affected by the lower glass transition temperature of polystyrene. During the sputtering process the polystyrene layer would heat up and the residual stress of the metal layer would cause the metal to wrinkle up on top of the polystyrene layer. The metal layer however would be in good adhesion to the polystyrene layer without void in between. Therefore, the polystyrene layer has softened and its top surface has deformed to relieve the residual stress of the sputtered metal layer. The lower glass transition temperature which assists the self-assembly of the polymer structures in turn affects the surface evenness of the underlying metal layer.

Under visual inspection of 5 nm of chromium and 250 nm of gold sputtered on a polystyrene layer, the surface looks fairly even. However, unlike the reflective metal layer sputtered on a spin-on-glass layer or a ProLIFT layer, the surface of the metal layer was matte. When the metal surface was inspected under a microscope, the surface showed small wrinkles as shown in Figure 5.7. The typical height variation was measured under a profilometer to be around 1 µm. The typical width of the wrinkles was
measured to be around 20 μm and length varied widely ranging from around 40 μm to 100 μm. However, the wrinkles were not large enough to be detrimental for fabrication of monopole antennas with 1.25 mm in length.

**Figure 5.7. Photomicrograph of a sputtered Cr/Au layer on top of a polystyrene layer.**

From the earlier trials, the metal sputtering on the polystyrene layer seemed to show bigger issues than stated above. More chromium and gold sputtering tests were performed to determine how the heat generated during the sputtering process affected polystyrene layer. Three wafers were sputtered with different gold thicknesses and different timing. The first wafer was sputtered with 5 nm of chromium and 250 nm of gold. The second wafer was sputtered with 5 nm of chromium and 500 nm of gold. However, the gold layer was sputtered in two separate steps. Each gold sputtering step deposited 250 nm of gold. Enough time was given between the two gold depositions to make sure that the wafer had cooled down before the second half of gold was deposited. The third wafer was sputtered with 5 nm of chromium and 500 nm of gold as well, but the gold layer was deposited all at once. Therefore, the wafer would be heated for a longer period of time and the effect of sputtering on the polystyrene layer would be greater.
Figure 5.8 shows the two of the three wafers after the sputtering, which were deposited with 500 nm of gold. The left wafer was sputtered in two separate depositions while the right wafer was sputtered all at once. As can be seen from the picture, the Cr/Au layer of the right wafer showed some bubbles after the sputtering. Under a microscope, the first two wafers (250 nm and 500 nm sputtered in two steps) showed almost no differences as shown in Figure 5.7 and Figure 5.9. However, the third wafer showed presence of large bubbles along with the wrinkles as seen in Figure 5.10 and the sizes of the bubbles varied from 150 µm to 1.4 mm. The polystyrene layer was heated up enough to generate the large bubbles under the metal layer. Thus, if the wrinkles resulting from the sputtering are acceptable for a given application, a thick metal layer can be sputtered by separating the deposition into multiple sputtering steps. Different metals would heat up the polystyrene layer differently during the deposition, and the thickness needed for each deposition step to prevent the formation of bubbles need to be determined for each metal. For the case of gold sputtering, if a metal layer thicker than 250 nm is needed, gold can be deposited 250 nm at a time with enough break in between to cool down the wafer enough to avoid the critical deformation of the polystyrene layer.
Figure 5.8. Two wafers deposited with 5 nm of Cr and 500 nm of Au. The left wafer is sputtered with 250 nm of Au at a time, while the right wafer is sputtered with 500 nm of Au at once.

Figure 5.9. Photomicrograph of a metal layer with 5 nm of Cr and two layers of 250 nm of Au.
The primary reason for moving away from polystyrene sacrificial layer was to undercoat the self-assembled polymer structures with metal layers to provide electrical connectivity on both sides of the antenna structures to ensure even radiation pattern on all directions. With the uncertainty of how the uneven metal layer sputtered on polystyrene sacrificial layer would affect on the fabrication, the other sacrificial materials, spin-on-glass and ProLIFT were attempted to replace the polystyrene for the sacrificial layer. As stated before, the low glass transition temperature of polystyrene has an important role allowing the self-assembly of the polymer structures to occur. A fabrication process was developed to build self-assembled SU-8 structures entirely coated with metal having in mind that the wrinkles of underlying metal layer might cause an adverse effect on fabrication.

For the self-assembled structures, SU-8 was used for both top and bottom structural layers. The difference from the initial SU-8 fabrication process with polystyrene sacrificial layer is that there will be metal under the bottom structural layer and above the top structural layer, which would enable coating all around the structures. If gold was used for the metal layer with chromium adhesion layer to the SU-8, gold and then chromium would be sputtered before the bottom structural layer is spun on, and chromium and then gold would be sputtered after both SU-8 structural layers are
developed. Therefore, the chromium adhesion layer would be placed between the SU-8 structures and gold. Metal layers of gold, chromium, and gold would be deposited in order on areas where there are no SU-8 structures as chromium layers are deposited on top of another.

Since the fabrication process is for making self-assembled antennas and the purpose of metallization is make polymer antenna structures electrically conductive by coating them with metals, only the metals on areas where there are no SU-8 structures need to be etched away before releasing the structures. The reason for doing this is to make sure that the sidewalls of the antennas structures are coated with metals to electrically connect both metal layers encapsulating the whole antenna structures with metal. In order to ensure that the metals on sidewalls of self-assembled structures are not etched away, several micrometers of metals extending from the sidewalls would be intentionally left over. The size of the extension would depend on accuracy of alignment and etch times. For patterning of the metal layers, thick positive photoresist Shipley S-1827 was used after the SU-8 structures were developed but not released. After exposing and developing the photoresist mask layer, metals were etched in the order of gold, chromium, and gold. After etching the metal layers, the underlying polystyrene sacrificial layer would be exposed for the release step.

5.4.2. Process Description

(a) 20 nm of chrome and 250 nm of gold are sputtered on a RCA cleaned wafer to serve as a base for the ground plane.

(b) 20 weight percentage polystyrene solution is spun on the wafer at 1500 rpm for 30 seconds and a 6 µm thick polystyrene layer is made. The polystyrene layer dries immediately, and Shipley 1827 photoresist
is spun at 1500 rpm for 30 seconds for thickness of around 6 µm. The wafer is then softbaked in an oven at 100°C for 15 minutes.

(c) The wafer is exposed through the anchor mask for 80 seconds to define anchors of microstructures. The photoresist layer is then developed in Microposit MF-319 developer for 3 minutes with agitation. The wafer is rinsed and dried for another exposure step.

(d) The wafer is exposed through the dimple mask for 14 seconds to expose the photoresist to only about 2 µm deep for dimple features. Dimple features are used to reduce stiction of microstructures to the substrate. The photoresist layer is again developed in Microposit MF-319 developer for 3 minutes with agitation. The wafer is then rinsed and dried.

(e) The anchor and dimple features are transferred to the polystyrene layer through RIE for 38 minutes with O₂ plasma at 40 sccm of O₂ flow rate, 100 mtorr of pressure, and 150 W of power. The etching
process is complete when the metal layer is revealed through the anchor features. An anchor depth of around 5.5 µm and a dimple depth of around 2 µm are achieved.

(f) 250 nm of Au and 20 nm of Cr are sputtered. Cr is sputtered after Au to promote adhesion of the metal layer to the first layer of SU-8.

(g) MicroChem SU-8 2010 is spun on to a 10 µm thickness at 3500 rpm for 30 seconds. The wafer is softbaked on a hotplate with ramping from room temperature (20°C) to 95°C at 300°C/hour ramping rate and then the temperature was kept at 95°C for another 30 minutes.

(h) The wafer is exposed for 45 seconds through the first structural layer mask. The first SU-8 layer features are overexposed for complete crosslinking before the second SU-8 layer is applied. The SU-8 layer is then post-exposure-baked on a hotplate with ramping from room temperature (20°C) to 95°C at 300°C/hour and then the temperature was kept at 95°C for another 15 minutes.
The second SU-8 layer is spun on to a 21 μm thickness at 1000 rpm for 30 seconds. A thicker layer is used to increase relative stiffness with defined support bar structures and leave enough room for bridge structures to be defined with a brief exposure. The wafer is softbaked on a hotplate at 95°C for 30 minutes.

The wafer is exposed for 60 seconds through the mask for support structures. Overexposure is desired to fully crosslink the support bar structures and to ensure good adhesion to the first structural layer.

The wafer is exposed for 8.5 seconds through the mask for bridge structures. Generally, the bridge features on the mask cover both support bars and areas between support bars to ensure continuity of the bridge structures.
(l) The SU-8 layers are developed in MicroChem SU-8 developer and
dried.

(m) 20 nm of Cr and 250 nm of Au are sputtered to complete
encapsulation of structures with metal.

(n) Shipley 1827 photoresist is spun at 1500 rpm for 30 seconds. The
wafer is then softbaked in an oven at 100°C for 15 minutes.
(o) The wafer is exposed through the metal mask for 80 seconds to define anchors of microstructures. The photoresist layer is then developed in Microposit MF-319 developer for 3 minutes with agitation.

(p) Exposed metal layers are etched in order using Au, Cr, and Au etchants.

(q) Photoresist is removed using acetone.

(r) Then, the sacrificial polystyrene layer is stripped in toluene and the structures are released for self-assembly. Isopropyl alcohol (IPA) is used to rinse the wafer and enhance drying process. As solvents are released from the structures, the self-assembly completes.
5.4.3. Fabrication Challenges and Result

Towards the end of the fabrication process, positive photoresist Shipley 1827 needed to be spun on to be used as an etching mask layer for metals around the antenna structures. The challenge of spinning a photoresist on an uneven surface is incomplete coverage of the photoresist on the wafer and streaks. In order to ensure good coverage of photoresist on the entire surface of the wafer, enough photoresist was poured onto the wafer before start of spin coating. Also, the speed, which was used for the spin-coating was ramped up slowly to make sure that the whole surface was covered with photoresist before reaching to the target speed. The time for spin coating was measured after the target speed was reached. Figure 5.11 shows a monopole structure entirely coated with metal layers.
For large antenna structures, release holes need to be added in order to reduce the time for releasing antenna structures from the substrate. For toluene to have short paths to the polystyrene sacrificial layer under large structures, small holes are created evenly over the large structures. Toluene can then dissolve polystyrene not just from the edges the structures but also from the top through the release holes.

5.5. SU-8 Fabrication with Patterned Metals with Polystyrene Scarificial Lyayer on Thick SU-8 Substrate

5.5.1. Introduction

The initial reason for using overhanging structures for fabricating transmission line was to pattern the transmission lines at a distance from the ground plane with the given fabrication process. The blanket deposition of metals at the end of the fabrication process for metallization of antennas disallowed patterned metal layer below the antennas structures for the purpose of fabricating transmission lines. With the ability to pattern metal layers for the antenna structures, incorporation of a thick SU-8 substrate with a patterned metal layer to serve as both transmission lines and ground plane was
possible. Because the blanket deposition of metals was removed at the end of the fabrication process, patterned transmission lines and ground plane could be protected under the polystyrene sacrificial layer during the metallization step of the antenna structures. A very thick SU-8 structure was used to distance the antennas and transmission lines to reduce radiation loss to the silicon substrate. For the new fabrication process, 50 µm thick SU-8 layer was used as a dielectric substrate for the antennas, which seemed to offer a good balance between performance gain and ease of fabrication. With the thick SU-8 dielectric substrates and patterned transmission lines, the effect of metal sidewall coverage of the transmission line using the initial fabrication method was eliminated.

Also, a thicker 500 nm metal layer was used which would be double the skin depth at 60 GHz. As discussed previously, sputtering of thick metal layers affects the sacrificial layer, which is cause mostly by heating up of polystyrene. To minimize the issue with the sacrificial layer, the sputtering process was split up into half and enough time was given between the sputtering steps to ensure that temperature of the sacrificial layer did not increase too high. Before the metals were sputtered on top of the SU-8 substrate, surfaces of the SU-8 structures were activated using RIE with oxygen in order to improve adhesion of the metal layer to the hardbaked SU-8 substrates.

Positive photoresist Shipley S1813 was used to create an etch mask for the metals on the thick SU-8 substrate. Similar to the spin-coating a photoresist over unreleased antenna structures, enough photoresist was poured on top of the wafer and the spin speed was increased slowly to ensure that the photoresist covered the whole wafer before reaching the final spin speed. Without this ramping step, the photoresist might no be able to reach some areas of the wafer, as it would radially move out too fast and might skip over the areas behind the thick SU-8 substrates. The ramping of the spin speed would also be critical for the subsequent spin-coating processing steps of the polystyrene sacrificial layer and the SU-8 structural layers. An example run sheet for this fabrication process is provided in Appendix A.
5.5.2. Process Description

(1) SU-8 2005 is spun on to a 5 µm thickness at 3000 rpm for 30 seconds on a RCA cleaned wafer and the wafer is softbaked at 95°C for 15 minutes with ramp from room temperature at a rate of 300°C/hour on a hotplate. Then, the wafer is blanket exposed for 35 seconds and post-exposure-baked on a hotplate with ramping from room temperature (20°C) to 95°C at 300°C/hour and then the temperature was kept at 95°C for another 15 minutes.

(2) SU-8 2025 is spun on to a 50 µm thick layer at 1700 rpm for 30 second and softbaked on a hotplate with ramping from room temperature (20°C) to 95°C at 300°C/hour and then the temperature was kept at 95°C for another 15 minutes.

(3) The wafer is exposed through the dielectric substrate mask for 100 seconds and post-exposure-baked on a hotplate with ramping from room temperature (20°C) to 95°C at 300°C/hour and then the temperature was kept at 95°C for another 15 minutes.
(4) The SU-8 layers are developed in MicroChem SU-8 developer and dried. The wafer is then hardbaked on a hotplate with ramping from room temperature (20°C) to 200°C at 300°C/hour and then the temperature is kept at 200°C for another 10 minutes. Then, surface of the SU-8 layers is activated through RIE for 3 minutes with O₂ plasma at 40 sccm of O₂ flow rate, 100 mtorr of pressure, and 150 W of power.

(5) 5 nm of Cr and 500 nm of Au are sputtered for creating transmission lines.

(6) In order to pattern the metal layers, positive photoresist Shipley 1813 is spun on at 3000 rpm for 30 seconds and softbaked at 100°C for 15 minutes in an oven.

(7) The photoresist layer is exposed through the transmission line mask for 10 seconds and developed in MF-319 for 30 seconds.
(8) Au and Cr are etched in Au and Cr etchants respectively.

(9) The photoresist etch mask is blanket exposed for 10 seconds and developed in MF-319 for 30 seconds.

(10) 20 weight percentage polystyrene solution is spun on the wafer at 1500 rpm for 30 seconds and a 6 µm thick polystyrene layer is made. The polystyrene layer dries immediately, and Shipley 1827 photoresist is spun at 1500 rpm for 30 seconds for thickness of around 6 µm. The wafer is then softbaked in an oven at 100°C for 15 minutes.
(11) The wafer is exposed through the anchor mask for 80 seconds to define anchors of microstructures. The photoresist layer is then developed in Microposit MF-319 developer for 3 minutes with agitation. The wafer is rinsed and dried for another exposure step.

(12) The wafer is exposed through the dimple mask for 14 seconds to expose the photoresist to only about 2 µm deep for dimple features. Dimple features are used to reduce stiction of microstructures to the substrate. The photoresist layer is again developed in Microposit MF-319 developer for 3 minutes with agitation. The wafer is then rinsed and dried.

(13) The anchor and dimple features are transferred to the polystyrene layer through RIE for 38 minutes with O₂ plasma at 40 sccm of O₂ flow rate, 100 mtorr of pressure, and 150 W of power. The etching process is complete when the metal layer is revealed through the anchor features. An anchor depth of around 5.5 µm and a dimple depth of around 2 µm are achieved.
(14) 500 nm of Au and 5 nm of Cr are sputtered. Cr is sputtered after Au to promote adhesion of the metal layer to the first layer of SU-8.

(15) MicroChem SU-8 2010 is spun on to a 10 µm thickness at 3500 rpm for 30 seconds. The wafer is softbaked on a hotplate with ramping from room temperature (20°C) to 95°C at 300°C/hour ramping rate and then the temperature was kept at 95°C for another 30 minutes.

(16) The wafer is exposed for 45 seconds through the first structural layer mask. The first SU-8 layer features are overexposed for complete crosslinking before the second SU-8 layer is applied. The SU-8 layer is then post-exposure-baked on a hotplate with ramping from room temperature (20°C) to 95°C at 300°C/hour and then the temperature was kept at 95°C for another 15 minutes.
(17) The second SU-8 layer is spun on to a 21 µm thickness at 1000 rpm for 30 seconds. A thicker layer is used to increase relative stiffness with defined support bar structures and leave enough room for bridge structures to be defined with a brief exposure. The wafer is softbaked on a hotplate at 95°C for 30 minutes.

(18) The wafer is exposed for 60 seconds through the mask for support structures. Overexposure is desired to fully crosslink the support bar structures and to ensure good adhesion to the first structural layer.

(19) The wafer is exposed for 8.5 seconds through the mask for bridge structures. Generally, the bridge features on the mask cover both support bars and areas between support bars to ensure continuity of the bridge structures.
(20) The SU-8 layers are developed in MicroChem SU-8 developer and dried.

(21) 5 nm of Cr and 500 nm of Au are sputtered to complete encapsulation of structures with metal.

(22) Shipley 1827 photoresist is spun at 1500 rpm for 30 seconds. The wafer is then softbaked in an oven at 100°C for 15 minutes.
(23) The wafer is exposed through the metal mask for 80 seconds to define anchors of microstructures. The photoresist layer is then developed in Microposit MF-319 developer for 3 minutes with agitation.

(24) Exposed metal layers are etched in order using Au, Cr, and Au etchants.

(25) Photoresist is removed using acetone.
Then, the sacrificial polystyrene layer is stripped in toluene and the structures are released for self-assembly. Isopropyl alcohol (IPA) is used to rinse the wafer and enhance the drying process. As solvents are released from the structures, the self-assembly completes.

5.5.3. Fabrication Challenges

The first major challenge for the fabrication process was spin-coating and patterning of the thick SU-8 substrate. Microposit SU-8 2025 was used to spin a 50-µm thick SU-8 layer on a 4" Si wafer. Ideally, Microposit SU-8 2050 was designed to spin such thick SU-8 layers, but because of difficulty handling such a viscous resist, Microposit SU-8 2025 was used instead. The thinner Microposit SU-8 2025 solution would then be spun at a much lower spin speed to achieve a 50 µm thick layer. Normally, spinning of such a viscous SU-8 resist would lead to bubble problems where bubbles would form while the photoresist is poured onto a wafer for spinning. When the wafer is spun, the formed bubbles would move towards the outer edge of the wafer. Any presence of bubbles would leave some streaks and the streaks might not disappear during the softbake depending on the size of the bubbles.

Also, the bubbles might still remain on the wafer surface after the spin-coating, which create a small gap during a contact alignment and influence the quality of
exposure. Contact alignment has the advantage of sharp resolution during pattern exposure as a mask would be in contact with a wafer minimizing any light diffraction. If a gap exists between a mask and a wafer due to a bubble, exposed features would be slightly larger. The thinner Microposit SU-8 2025 was a better alternative, as there were very little formation of bubbles and streaks from the spin-coating.

The timing RIE was difficult as part of the substrate where the anchors were located was not fully metallized to act as an etch stop. When the RIE reached transmission line features in anchors, the substrate outside the transmission line would continue to etch. Due to lack of a photoresist with right viscosity, the photoresist layer was thicker than the polystyrene sacrificial layer, and etching of the SU-8 substrate was unavoidable past the depth of the transmission line. A thicker polystyrene layer tested for usage to accommodate the thickness of the photoresist. However, due to development of thermal stress during baking polystyrene layer developed cracks with any higher thicknesses. The cracks later lead to partial peeling of the sacrificial layer during the application of SU-8 photoresist.

Due to the thicker photoresist layer, precise timing of RIE was necessary. Since there was a slight possibility that little bit of photoresist might be left behind on the polystyrene sacrificial layer, the wafer was submerged in an acetone bath for 30 seconds during the release step of the structures. The antenna structures did not show any ill effect from the acetone bath. As the wafer was rinsed in an isopropyl alcohol bath with almost no agitation, antenna structures started to self-assemble out of plane. The wafer was then taken out of the rinsing bath very gently and was air-dried.
6. Design Rules

6.1. General Rules

Several design guidelines need to be discussed for designing layout of self-assembled antennas. These guidelines are to be used to maximize the fabrication yield of self-assembled antennas. Some of the guidelines may need to be modified depending on specifications of available cleanroom equipment. Following guidelines will be mostly based on equipment in a university-level cleanroom facility.

For structures that are required to be coated with metal layers, photoresist etch mask should be used which extends at least 10 µm over the outer edges of the structures in order to provide enough room for alignment error and extra etch time for metals. Since the fabrication process requires seven exposure masks with several very thick structural layers, alignment can be challenging. The etching of metals can take more time than expected because of uneven etching of metals over the surfaces of a wafer. Therefore, slightly larger photoresist etch masks are recommended taking into account that some of the metals will etch under the photoresist masks. Another reason for leaving the extra room for error is that since the edges of the photoresist masks are not on the same height as the photoresist on top of antenna structures, the exposed areas are not in full contact with the exposure mask. The gap will cause some light diffraction, which will make dimensions of the photoresist etch masks slightly smaller than intended.

For any freestanding microstructures, stiction is the biggest concern for failure. In order to prevent stiction, area of contacts of microstructures to the substrate needs to be minimized. Placing dimple features under the microstructures can minimize the area. For example, 1 mm by 1 mm square freestanding structure can have 25 of 5 µm by 5 µm dimple features and reduce the area of contact by 1600. 5 µm by 5 µm dimple features can be placed every 200 µm by 200 µm areas to prevent stiction. The occurrence of
dimples can be increased or decreased depending on the structural layer thickness and flexibility. Above recommendation worked well enough that they microstructures were able to detach themselves from the substrate during the drying process of solvents at the end of the fabrication process.

Another thing to consider when designing relatively large microstructures is placing etch holes to assist with development of SU-8 structures and release of the microstructures. If self-assembly of large of microstructures is necessary, very wide bridge structures for the self-assembly might be necessary as shown in Figure 6.1. If that is the case, the time for the SU-8 developer to develop uncrosslinked part of SU-8 under the bridge structures might be too long because of the developer cannot reach easily. Etch holes can be placed along the bridge structures to increase the area for the SU-8 developer to dissolve the uncrosslinked SU-8. These etch holes can be 20 µm by 20 µm squares and can be placed every 200 µm along the bridge structures. Similarly, etch holes need to be placed on large structures to help with the releasing step such that toluene can start etching the polystyrene layer from many directions and reduce the time required. The size of the etch holes can be 20 µm by 20 µm as well can placed every 200 µm by 200 µm square areas. When self-assembling parts of structures span large areas as in Figure 6.1, etch holes need to be placed on both the lower structural layer and the bridge structures such that toluene will have short paths to the polystyrene layer. When metals are placed on top and bottom of microstructures, the metal layers need to be patterned in such a way that the metal layers would not block the etch holes.
Figure 6.1. Example layout of a wide self-assembled structure.

A benefit of using SU-8 as a structural material is the good mechanical property, which allows fabrication of large structures for MEMS. Very large structures with length reaching to 1 cm have been fabricated successfully using the fabrication process. Although the capability might not be useful for most MEMS applications, it represents the advantage of using SU-8 as a structural material. Nevertheless, care need to be taken while handling such large structures during the release step as large movement of solvent might bend the structure too much and break the microstructure as in any other fabrication processes.

In a previous chapter, the method of achieving different curvatures using the self-assembly mechanism was presented which were achieved by using different ratio of dimensions for bridge and support bar structures. As can be seen in Figure 4.10, the rate of self-assembly tapered off as the ratio of the bridge to the bar structure dimensions increased. As the length of the bridge structure increases, magnitude of the induced stress would increase and affect the effectiveness of the bridge structure due to strain. One method of solving this issue would be using a better UV aligner and a mask, which would enable aligning and defining features with greater accuracy and use shorter pitch lengths while keeping the ratio the same. Thus, the size of each bridge structure would decrease respectively and be under less stress per structure with the same ratios.
6.2. Anchor Design

6.2.1. Grounded Anchors

When an anchor is required which is grounded to the ground plane, the following steps need to be performed. After ground plane is defined on top of the thick SU-8 substrate, the polystyrene sacrificial layer would be spun on. The anchor feature needs to be patterned on the sacrificial layer with RIE over where the ground plane is located. After the ground plane is exposed through the hole for the anchor, the metal layers both under and over the intended antenna structure are deposited along with the SU-8 structure. When the metal layers for the antenna structure are patterned, the etch mask for the patterning of the grounded anchor need to be bigger than the size of the anchor to ensure that the metallized sidewalls of the grounded anchor are not etched. Thus, the ground plane, the metal layer under the anchor structure, and the metal layer over the anchor structure are all connected. In addition, making the size of the anchor equal to or larger than the size of the hole on the sacrificial layer is recommended to lower the chance of making errors during the layout process of the grounded anchors. If the size of the photoresist etch mask for the anchor metal patterning and the anchor structures were both smaller than the size of the anchor hole, metal around the anchor would be etched away on the ground plane and make the anchor electrically isolated.
6.2.2. Anchors to Transmission Lines

When anchors need to be connected to transmission lines to feed the antennas, holes for the anchors on the sacrificial layer is made over one end of the transmission lines. At the end of the transmission lines, the width of the lines is gradually widened towards the anchor. The end of the transmission lines does not cover the whole area of the anchor holes. One of the reasons of doing this is to ensure that all the polystyrene is removed from the anchor holes. If any polystyrene were left over, the anchor would detach from the substrate and the antenna structure would not stay on the wafer.

However, the fabrication experiment showed that covering whole area of the anchor holes with metal would actually be better since the thick positive photoresist layer used for transferring anchor and dimple features was much thicker compared to the polystyrene sacrificial layer. If the photoresist needs to be removed completely during transferring the anchor and dimple features using RIE, the difference in height between the polystyrene sacrificial layer and the thick positive photoresist layer would be transferred as holes on the thick SU-8 substrate next to the transmission lines as all three layers etch at a similar rate. The transmission lines would however not be etched as the metal used for the transmission lines acts as an etch mask for RIE. Thus, there

Figure 6.2. Layout of a grounded anchor.
would be some height difference between the transmission lines within the anchors and rest of the area of the anchors. This difference in height can be fixed by covering the whole anchor area with metals. Even with a significant difference between the sacrificial layer and the photoresist layer thicknesses, timing of transferring the anchor and dimple features to the sacrificial layer would not be difficult.

![Image of an anchor connected to a transmission line.](image)

**Figure 6.3. Layout of an anchor connected to a transmission line.**

### 6.3. Monopole Antenna Design

The simplest form of self-assembled 60 GHz antennas is a vertically raised monopole antenna with length of a quarter-wavelength. The self-assembling structures can be placed near anchors of the antennas and use them to raise the monopole structures vertical to the substrate surface. Figure 6.4 shows a typical layout for the monopole antennas. Different curvatures can be used to raise the structures vertical while the structures that yield the highest curvatures would require the shortest length to achieve the same. If tip of the monopole antennas are void of self-assembling structures, a bar structure can be placed along the length of the monopole antenna to ensure that the structures remains very flat at the tip.
6.4. Structures of Different Shapes

Other than the vertical monopole structures, structures of different shapes can be self-assembled vertical to the substrate surface. Irrespective of the shape of the structures, the self-assembling structures can be placed over the surface of the structures to make them self-assemble. If the widths of the structures that apply the stress are the same as the widths of the structures being self-assembled, the rate of curvature would be as expected. Thus, structures can be self-assembled to desired
degrees of assembly by using correct ratios of the bridge and support bar structures and the total length of the self-assembled structures. Figure 6.5 shows layouts for elliptical and triangular self-assembled structures. Depending on the length of the erected structures, the self-assembling structures would span only part of them. As can be seen in the layout of a triangular structure, support bar structures are places along the length to ensure the flatness on that particular area of the structure.

![Figure 6.5. Layouts for elliptical and triangular self-assembled structures.](image)

### 6.5. Half Loop Design

Half loop structures are fabricated by connecting two monopole structures of same degrees of self-assembly with a half loop structure. The two monopole structures are designed to self-assemble vertical to the substrate surface to make the half loop structure stand vertical. Figure 6.6 shows a layout for a self-assembled half loop structure. As shown in the figure, a supporting bar structure is place along the flat part of the structure to ensure flatness.
Figure 6.6. Layout of a half loop antenna.
7. 60 GHz Antennas

7.1. Fabricated Antennas

Figure 7.1 shows an image taken using a scanning electron microscope (SEM) of a monopole antenna fabricated using the final fabrication process. The antenna was fabricated on top of a 40 µm thick SU-8 substrate and was covered with chromium and gold bi-layers on top and bottom. The transmission line was patterned on the SU-8 substrate and was connected to the both metal layers of the antenna. Figure 7.2 shows a top view image of transmission lines fabricated for calibration test. The ground plane covers almost all of the SU-8 substrate except near the transmission lines and the antenna anchors. The ground plane is placed even under the antenna. The advantage of this fabrication is that the thicknesses of the metal layers are all even irrespective to the location.
Figure 7.1.  SEM image of a monopole antenna.
Figure 7.2. **SEM image of transmission lines viewed from top of the chip surface.**

Figure 7.3 shows an SEM image of a half loop antenna. The left anchor of the antenna is connected to a transmission line, while the other anchor is connected to the ground plane. The design of the transmission line, left anchor, and the connection between the transmission line and the metal layers of the anchor are exactly same as the monopole antenna. However, the right anchor is intentionally grounded by placing the bottom metal layer of the anchor directly on top of the ground plane to make an electrical connection. Since the top and bottom metal layers are patterned to be larger than the self-assembled antenna structure they are placed on, the bottom and the top
metal layers make an electrical connection with each other covering the structure all around.

Figure 7.3. SEM image of a half loop antenna.

7.2. Antenna Measurements

Currently, measurement facilities, which are capable of characterizing the antennas, are not available in British Columbia. All industrial and academic organizations in British Columbia are limited to measurements in low gigahertz frequencies. Two sets of parameters were of interest: network parameters (impedance,
return Loss, for example) and over-the-air (OTA) performance. Network parameter measurements for antennas built with the initial fabrication process, where metals were blanket deposited, were carried out in CMC facility located in the University of Manitoba.

The major challenge is determining the antenna radiation efficiency, radiation pattern, and polarization. The fabricated antennas are currently shipped for performance measurements to Orange Labs in La Turbie, France, which is one of only few facilities in the world with the measurement capability.

Figure 7.4 shows the setup used for OTA measurement at the Orange Labs. Preliminary measurements were performed on a monopole antenna, which was 1250 µm long and 200 µm wide. The measurement showed about -5 dBi gain at 60 GHz and maximum gain was measured at 66 GHz. Figure 7.5 shows the radiation pattern on horizontal (XY plane) and vertical (XZ plane) planes.

![Figure 7.4. Measurement setup at the Orange Labs in La Turbie.](image)
Figure 7.5. Radiation pattern measurement on horizontal and vertical planes.
8. Contributions

The development of a fabrication process for building self-assembled 60 GHz on-chip antennas and the testing of the fabricated antennas and transmission lines have led to two journal articles and two conference papers and a US patent. The fabrication process is the first to allow full control of curvature and direction of curvature for self-assembly of millimeter-wave antennas. A cost-effective, fast, and very flexible fabrication process has been developed which could be used for the next generation 60 GHz SOC solutions. Several journal publications are in preparation based on a conference paper and measurement updates of antennas fabricated with the most recent process. A short summary of the academic articles is as following:


This was the first article which explained how self-assembled structures could be fabricated using the multi-user polymer MEMS process [66]. The article was submitted after achieving the self-assembly using the stress-inducing SU-8 bar structures on top of planar SU-8 structures. This work was the first to explain how stress developed during the crosslinking of SU-8 could be used to apply with specific amounts of stress to control the resulting curvatures. Also, the directions of curvatures were controlled independently of the shape the structures which were being self-assembled as the stress-inducing bar structures were acting as mechanical reinforcements perpendicular to the direction of curvatures. Different ratio of stress-inducing bar structures were shown for designing of self-assembled structures with predetermined curvatures. Vertically self-assembled straight and triangular cantilevers, a vertically self-assembled half-loop structure, and a cantilever self-assembled into a helix were presented.


Vertically self-assembled straight and oblique monopole antennas were fabricated based on the earlier publication and the antenna measurements and simulations were performed to determine the antenna radiation efficiency. The enhanced self-assembly method was used to provide higher self-assembled curvatures for fabrication of 60 GHz antennas. The fabrication process included blanket deposited metal layers to provide an electrically conductive layer on the polymer antenna structures and anchors were designed to electrically isolate the antennas from the ground plane with the overhanging structures. With the ability to control the direction of curvatures, oblique antennas were fabricated along with the straight monopole antennas. The work was the first CMOS compatible on-chip antennas, which were self-assembled with the control of the magnitude and the direction of curvatures for individual antennas. The estimated antenna efficiency was 25%, which is considered very high performing at 60 GHz.


This conference paper described the fabrication method of the transmission lines using the fabrication process with polystyrene sacrificial layer together with the blanket metal depositions. The transmission lines were fabricated by separating the metals on the transmission line structures from the ground plane using overhanging structures on raised anchor structures, which determined the geometry of the transmission lines. The transmission lines were characterized and the issues of having sidewall metal coverage on the overhanging structures were discussed.

This conference paper investigated a new fabrication process, which would provide more control on the thickness of the metal layers deposited on both above and under the self-assembled structures by individually depositing the both metal layers during the fabrication process and patterning the metal layers in the shape of the antennas before releasing the antenna structures from the substrate. Previously, the antenna structures were metallized after they were released from the substrate and self-assembled. Therefore, it was previously uncertain exactly how thick of metal layers were deposited on parts of the structures which were not lying parallel to the substrate and under the structures. Also these patterned metal layers could be deposited thicker than with the blanket deposition as there was no risk of shorting the antennas and the transmission lines to the ground plane. As the patterning of the metal layers was not limited to just the shapes of the antenna structures, the fabrication process showed a possibility of integrating other electrical devices on self-assembled stages. Journal publications are in preparation, which would discuss the integration of patterned transmission lines on very thick dielectric substrates along with the discussed fabrication process for antennas, and the performances of the fabricated self-assembled 60 GHz antennas.
9. Conclusions

In this work, fabrication processes were developed for building self-assembled antennas and transmission lines. The requirements for the new fabrication processes were tailored to build highly efficient millimeter-wave antennas. Several fabrication processes were developed to address these requirements to address issues such as uncertainty of thickness of deposited metal layers on self-assembled structures and non-planar transmission lines. During the search of a fabrication process that would meet all the requirements, the usage of polystyrene as a sacrificial layer for the self-assembled structures was found to be crucial for generating the stress mismatch between the two structural SU-8 layers and allowing the self-assembly to happen. Polystyrene has a low glass transition temperature and minimizes the stress developed between the sacrificial layer and the first structural layer and the stress developed between the first and the second structural layers is not negated.

For reliable self-assembly, the first structural layer should be free of stress while the second structural layer should apply enough stress to curl the structures out of plane and be made of a material with very similar or the same coefficient of thermal expansion. With dissimilar coefficients of thermal expansions, the shape of the self-assembled structures would be sensitive to temperatures. The final fabrication process uses SU-8 for both structural layers and thus the fabricated freestanding structures are not sensitive to change of temperatures. The volume shrinkage of SU-8 is used to create the stress between the layers, as they are crosslinked separately. In addition, the photopatternable second layer simplifies the design and fabrication of the self-assembled structures. The magnitude of the stress and the direction to which the stress is applied can be easily controlled using photolithography. The ability to easily control these variables over every part of the self-assembled structures gives a great flexibility to create various types of three-dimensional structures.
The thick dielectric substrates were fabricated using a very thick SU-8 photoresist formula to distance the antennas and transmission lines from the silicon substrate. On top of the thick dielectric substrates and around the antenna structures, patterned metal layers were used to achieve accurate transmission line geometries and consistent thickness of metals over the antennas. Design guidelines were discussed to help antenna designers create layouts, which would produce three-dimensional self-assembled structures with desired antenna geometries. The fabrication process is compatible with CMOS integrated circuits as all the fabrication steps were performed at very low temperature and the contamination from deposited metals can be prevented with a passivation layer between the CMOS chip and the antenna structures. In conclusion, a fast and cost-effective CMOS compatible fabrication process was developed for building highly efficient millimeter-wave antennas, which would be excellent for prototyping as well as industrial scale manufacturing.
References


Appendix A.

Run Sheet for SU-8 Fabrication with Patterned Metals and Polystyrene as a Sacrificial Layer

<table>
<thead>
<tr>
<th>Completed</th>
<th>Fabrication Step</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Spin SU-8 2005 @ 3000 rpm</td>
</tr>
<tr>
<td></td>
<td>Softbake @ 95°C for 15 min with ramp @ 300°C/hour</td>
</tr>
<tr>
<td></td>
<td>Expose wafer for 35 sec</td>
</tr>
<tr>
<td></td>
<td>Post-exposure-bake @ 95°C for 15 min with ramp @ 300°C/hour</td>
</tr>
<tr>
<td></td>
<td>Spin SU-8 2025 @ 1700 rpm</td>
</tr>
<tr>
<td></td>
<td>Softbake @ 95°C for 15 min with ramp @ 300°C/hour</td>
</tr>
<tr>
<td></td>
<td>Expose SUBSTRATE MASK for 100 sec</td>
</tr>
<tr>
<td></td>
<td>Post-exposure-bake @ 95°C for 15 min with ramp @ 300°C/hour</td>
</tr>
<tr>
<td></td>
<td>Develop in SU-8 developer</td>
</tr>
<tr>
<td></td>
<td>Hardbake @ 200°C for 10 min with ramp @ 300°C/hour</td>
</tr>
<tr>
<td></td>
<td>Activate SU-8 surface with O₂ plasma for 3 minutes</td>
</tr>
<tr>
<td></td>
<td>Sputter 5 nm Cr and 500 nm Au</td>
</tr>
<tr>
<td></td>
<td>Spin S1813 @ 3000 rpm</td>
</tr>
<tr>
<td></td>
<td>Softbake @ 100°C for 15 min in oven</td>
</tr>
<tr>
<td></td>
<td>Expose TRANSMISSION LINE MASK for 10 sec</td>
</tr>
<tr>
<td></td>
<td>Develop in MF-319 for 30 sec</td>
</tr>
<tr>
<td></td>
<td>Etch Au and Cr</td>
</tr>
<tr>
<td></td>
<td>Expose wafer for 10 sec</td>
</tr>
<tr>
<td></td>
<td>Develop in MF-319 for 30 sec</td>
</tr>
<tr>
<td></td>
<td>Spin 20% wt polystyrene solution @ 1500 rpm</td>
</tr>
<tr>
<td>Step</td>
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<tr>
<td>----------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>Spin S1827 @ 1500 rpm</td>
<td></td>
</tr>
<tr>
<td>Softbake @ 100°C for 15 min in oven</td>
<td></td>
</tr>
<tr>
<td>Expose ANCHOR MASK for 80 sec</td>
<td></td>
</tr>
<tr>
<td>Develop in MF-319 for 3 min</td>
<td></td>
</tr>
<tr>
<td>Expose DIMPLE MASK for 14 sec</td>
<td></td>
</tr>
<tr>
<td>Develop in MF-319 for 3 min</td>
<td></td>
</tr>
<tr>
<td>RIE with O₂ plasma for 38 min</td>
<td></td>
</tr>
<tr>
<td>Sputter 500 nm Au and 5 nm Cr</td>
<td></td>
</tr>
<tr>
<td>Spin SU-8 2010 @ 3500 rpm</td>
<td></td>
</tr>
<tr>
<td>Softbake @ 95°C for 30 min with ramp @ 300°C/hour</td>
<td></td>
</tr>
<tr>
<td>Expose FIRST LAYER MASK for 45 sec</td>
<td></td>
</tr>
<tr>
<td>Post-exposure-bake @ 95°C for 15 min with ramp @ 300°C/hour</td>
<td></td>
</tr>
<tr>
<td>Spin SU-8 2010 @ 1000 rpm</td>
<td></td>
</tr>
<tr>
<td>Softbake @ 95°C for 30 min with ramp @ 300°C/hour</td>
<td></td>
</tr>
<tr>
<td>Expose SUPPORT STRUCTURE MASK for 60 sec</td>
<td></td>
</tr>
<tr>
<td>Expose BRIDGE MASK for 8.5 sec</td>
<td></td>
</tr>
<tr>
<td>Post-exposure-bake @ 95°C for 15 min with ramp @ 300°C/hour</td>
<td></td>
</tr>
<tr>
<td>Develop in SU-8 developer</td>
<td></td>
</tr>
<tr>
<td>Sputter 5 nm Cr and 500 nm Au</td>
<td></td>
</tr>
<tr>
<td>Spin S1827 @ 1500 rpm</td>
<td></td>
</tr>
<tr>
<td>Softbake @ 100°C for 15 min in oven</td>
<td></td>
</tr>
<tr>
<td>Expose METAL MASK for 80 sec</td>
<td></td>
</tr>
<tr>
<td>Develop in MF-319 for 3 min</td>
<td></td>
</tr>
<tr>
<td>Etch Au, Cr, and Au</td>
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<td></td>
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<tr>
<td>☐</td>
<td>Remove photoresist in acetone</td>
</tr>
<tr>
<td>☐</td>
<td>Remove polystyrene layer in toluene</td>
</tr>
<tr>
<td>☐</td>
<td>Rinse with IPA</td>
</tr>
</tbody>
</table>