FPGA IMPLEMENTATION OF SOFTWARE DEFINED RADIO MAC LAYER

by

Sameer Khushal

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Name: Sameer Khushal

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Examining Committee:

Chair: Dr. Marek Syrzycki
Professor
School of Engineering Science

Dr. Stephen Hardy
Senior Supervisor
Professor
School of Engineering Science

Dr. Tejinder Randhawa
Adjunct Professor
School of Engineering Science

Dr. Paul Ho
Professor
School of Engineering Science

Date approved: April 11, 2003

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Title of Thesis/Project/Extended Essay

FPGA Implementation of Software Defined Radio MAC Layer

Author:

(signature) _____

(name) Sameer Khushal

(date) April 14 2003

Abstract

In order to converge the large number of wireless standards onto a Software Defined Radio (SDR) system a configurable approach to the various signal processing and process mechanisms is needed. This work will focus on the configuration of Medium Access Control (MAC). The configuration to be explored will be between Aloha and CSMA, two common protocols. This ability to dynamically configure between the two channel access methods, during the transfer from one network to another, is termed vertical handoff.

The configuration will be achieved through the use of the Field Programmable Gate Array (FPGA) semiconductor device. This device allows its configuration and algorithms to be altered at any time. In this implementation, our design flow will involve a high level description using a state machine followed by hardware description language then verification and final preparation for future implementation in the semiconductor.

The implementation of MAC layer configuration is shown through the implementation of two access schemes using the same hardware. In addition it is shown that the time required to handoff between the two is manageable.

This method of implementing the MAC makes the use of the FPGA invaluable in SDR, especially when it is considered that the underlying

hardware implementation can be upgraded or changed while the device it is installed in the field, which is the original intent of SDR.

Dedication

To all those who made reaching this point possible.

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Table of Contents

List of Tables

List of Figures

Chapter 1
Introduction

In order to converge the large number of wireless standards onto a Software Defined Radio (SDR) system a configurable approach to the various components is needed. This work will focus on the configurability of Medium Access Control (MAC). The configurability to be explored will be between Aloha and CSMA. This ability to dynamically configure between the two channel access methods, during the transfer from one network to another, is termed vertical handoff.

Due to the emergence of non-regulated wireless services, eg. 802.11b, and their subsequent popularity, the interface with regulated services, eg. GSM/GPRS, becomes an issue when seamless roaming between wide area and local area networks is considered. A major part of this interface is the MAC layer. So this vertical handoff mechanism can be used when transitioning from a non-regulated to regulated service and vice versa. An extension of the seamless roaming principle is between regulated services, eg GPRS to CDMA, which will not be considered here.

The configurability will be achieved through the use of the Field Programmable Gate Array (FPGA) semiconductor device. This device allows its configuration and algorithms to be altered at any time.

Software Defined Radio

In order to keep radio hardware and software from becoming obsolete, due to emerging and changing standards, a new paradigm is needed. The concept of the Software Defined Radio (SDR) provides that as much as possible of the radio system is configurable. The hardware design of a radio system is a very complicated and time consuming process. Once a standard hardware design is implemented, based on SDR concepts, it's configuration can be modified by implementing software changes, thus avoiding costly, from time and monetary perspectives, hardware changes.

In the context of this work, the aspects of SDR that are to be investigated relate to multifunctionality between short-range networks and cellular networks. This is desirable so that a device can achieve uninterrupted and high quality service wherever it may be. Current wireless standards typically dictate lower data rates for cellular transmission and higher rates for local area networks, for example GPRS vs 802.11. Hence, it is advantageous to operate within local area networks when physical possible, i.e. in radio frequency range.

Within the Software Radio System the majority of the signal processing can be implemented with an Application Specific Integrated Circuit (ASIC) or Field Programmable Gate Array (FPGA). The ASIC is highly optimized for a particular application and cannot be modified once

it is manufactured. In addition the time to remanufacture and revision the product is considerable, on the order of months. The FPGA is configurable at any time, with tradeoffs in speed, power and size. Modern FPGA's contain Digital Signal Processors (DSPs) as well as high speed interfaces, and tradeoffs are better managed through algorithmic and other, usually proprietary, innovations.

FPGA Overview

In this work we will use the FPGA due to its configurability and the positive implications of this with regards to SDR. The FPGA allows the user to design circuit level hardware, program the device and make changes at any time during the life of the design. There are two major types of FPGAs: SRAM Based, and One Time Programmable. For SDR we will use the SRAM Based FPGAs. This will allow us to reprogram the device when it is in the field.

The FPGA is an Integrated Circuit (IC), usually based on silicon, that is packaged in a protective case. An example of an FPGA is shown in Figure 1, the packaged device is in the foreground and the IC is shown in the background.

Figure 1 Packaged FPGA & Silicon [2]

When the FPGA is assembled as part of a system it will be included on a Printed Circuit Board (PCB) that connects it to other components in the system. An example PCB is shown in Figure 2, the FPGA is the device in the middle.

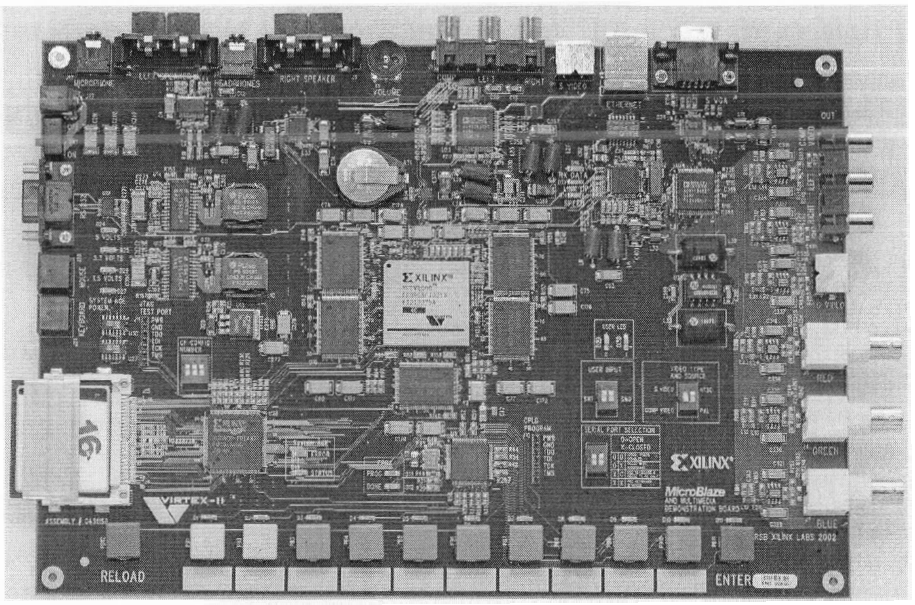

Figure 2 FPGA on PCB [2]

The configurability and speed gains achievable with an FPGA make it a vital part of the SDR system. Once in the system it can even be reprogrammed while the system is operationally active.

The other major part of the FPGA system is the software with which the system is programmed. A Hardware Description Language (HDL) is used to describe the operations that the FPGA must perform. Unlike software programming languages, HDL can describe concurrent operations. This allows speed and functionality gains when compared to implementations done purely in software. The general flow for

implementation of functionality in an FPGA is shown in Figure 3. During Specification HDL is generated, or a schematic is created, that is then transformed into a netlist. In Verification, the functionality of the described hardware is tested, including timing and semantics. During Implementation most of the work is done by the software design tools, where they determine the most efficient way to fit the described functionality onto the hardware. During System Debug, the FPGA is tested in the system and if modifications need to be made it can be programmed in there. This reprogramming is almost instantaneous, because hardware manufacture is not necessary with the FPGA. With other IC devices several months and many dollars later a new device would emerge.

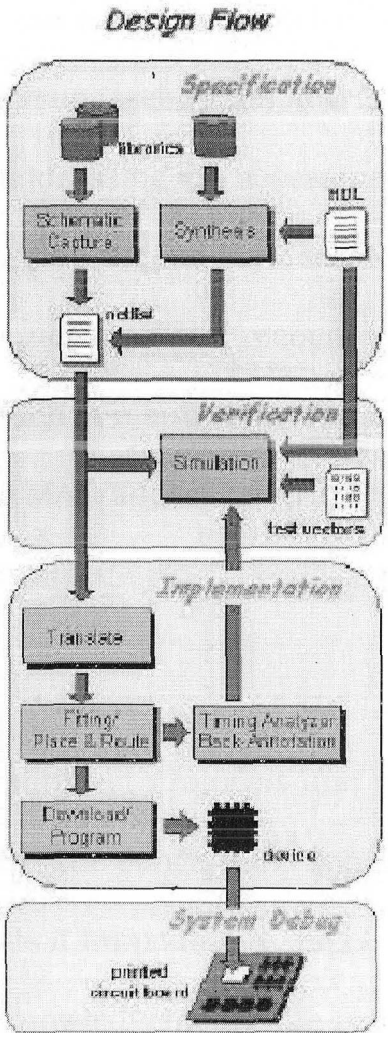

Figure 3 FPGA Design Flow [2]

MAC Layer Description

In a typical protocol stack the Medium Access Control (MAC) functionality is part of the Data Link Layer (DLL). The DLL is responsible for error control & synchronization. The MAC sublayer is responsible for determining priority and allocation to access the channel. The MAC can implement protocols based on random access, ordered access,

deterministic access, or some combination. Here we will investigate Random Access which encompasses Aloha and CSMA.

The MAC provides addressing via accessing the wireless medium, access coordination via joining the network session, authentication and privacy. It also provides addressing and recognition frames in support of the Logical Link Layer, which is a sub layer above the MAC. Typically each station has a unique MAC address which defines whether or not it should receive the transmitted data.

Aloha

Aloha is one of the simplest protocols and was the earliest to be developed and analyzed [3]. The concept in Aloha is that when a station wants to send data it sends it immediately, no checking of the channel is done, then it waits for acknowledgement. The main use in Aloha is when the propagation time is much larger than the time to transmit the packet. The peak throughput of Aloha is approximately 18% [3].

A variant, Slotted Aloha, maintains that all stations synchronize on a time base and transmit only at specified intervals. In this way the collision time is reduced since the collisions can only occur for single transmission intervals. Whereas in Aloha they could easily occur across multiple transmission boundaries. This doubles the throughput to approximately 36% [3].

CSMA

Carrier Sense Multiple Access (CSMA) refers to schemes that detect when the medium is in use. In CSMA schemes it is generally assumed that the maximum propagation delay is small. The CSMA/CD (Collision Detection) scheme is used in wired networks because they allow for instantaneous detection of the physical medium. In our case we will be looking at the CSMA/CA (Collision Avoidance) scheme since it is used in the wireless arena, due to the inconsistencies of radio communications. CSMA/CA makes use of p-persistence, which states that the station must wait for the medium to be idle and p is 0<p<=1. With CSMA/CA this means that once the medium is idle an additional time must be waited out. This additional time is varies from station to station. The peak throughput of 1-persistent CSMA is 53% [3].

Chapter 2
Design

The hardware design of the MAC layer was done using Xilinx FPGA design software [4]. This software is considered industry standard and allows a great deal of flexibility as to how the initial design is done, before the physical implementation is decided. The nature of the software guarantees that once the design is complete the necessary timing and performance will be met in the physical implementation. The various characteristics of the generic FPGA have been included in the software to speed the hardware design. Hence, it was only necessary to ensure that the design functioned properly in the software. The final hardware implementation would be better defined when the system is designed.

The main interface to controlling the software is shown in Figure 4. From that interface the hierarchy of the design may be defined including, state machines, schematics, and HDL code. Implementation of the design may also be defined, including chip level mapping, pin mappings, and target device specification.

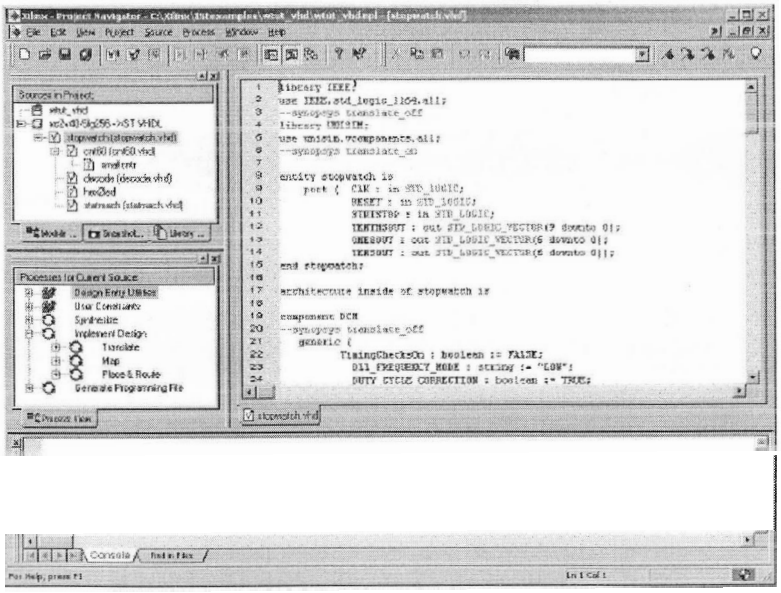

Figure 4 Xilinx FPGA Design Software

For our purposes we start of with the state machine design as show in Figure 5. The methodology at deriving such a state machine is beyond the work here but is well defined in [3] and [5]. The important parts of this state machine are that it allow for places at which conditions are set and checked and counters are incremented and checked. These are necessary and important parts of MAC layer design. In particular for the Aloha and CSMA methods considered here, these are the main functional parts.

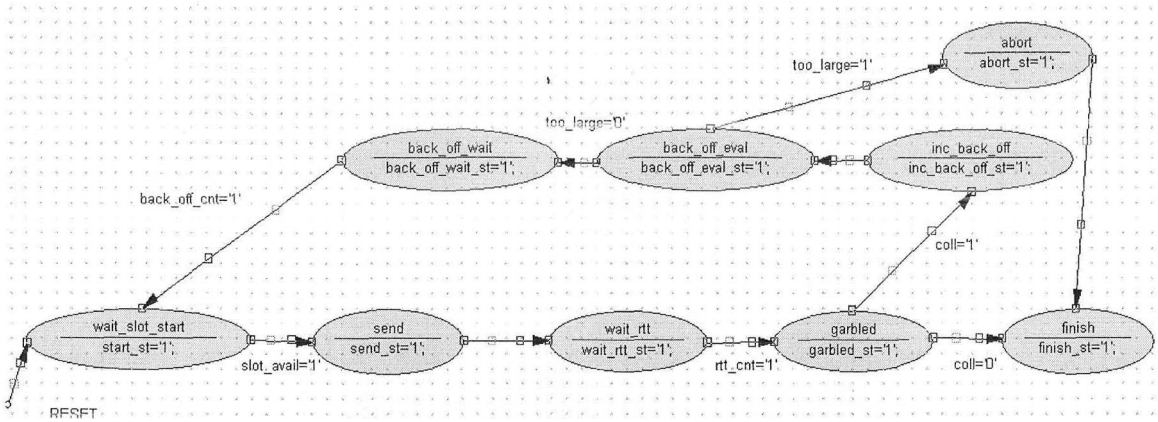

Figure 5 Reconfigurable State Machine

The high level state machine description is configured into a HDL description which can be hardware implemented. The HDL description is shown in Figure 6. This HDL description is verified against the state machine description and functional checks are done.

```
1
2   LIBRARY ieee;
3   USE ieee.std_logic_1164.all;
4
5   ENTITY ALOHA_TX IS
6      PORT (CLK,back_off_cnt,coll,RESET,rtt_cnt,slot_avail,too_large: IN std_logic
7         ;
8         abort_st,back_off_eval_st,back_off_wait_st,finish_st,garbled_st,
9            inc_back_off_st,send_st,start_st,wait_rtt_st : OUT std_logic);
10  END;
11
12  ARCHITECTURE BEHAVIOR OF ALOHA_TX IS
13  -- State variables for machine sreg
14     SIGNAL abort, next_abort, back_off_eval, next_back_off_eval, back_off_wait,
15        next_back_off_wait, finish, next_finish, garbled, next_garbled, inc_back_off,
16         next_inc_back_off, send, next_send, wait_rtt, next_wait_rtt, wait_slot_start
17         , next_wait_slot_start : std_logic;
18  BEGIN
19     PROCESS (CLK, RESET, next_abort, next_back_off_eval, next_back_off_wait,
20        next_finish, next_garbled, next_inc_back_off, next_send, next_wait_rtt,
21        next_wait_slot_start)
22     BEGIN
23        IF ( RESET='1' ) THEN
24           abort <= '0';
25           back_off_eval <= '0';
26           back_off_wait <= '0';
27           finish <= '0';
28           garbled <= '0';
29           inc_back_off <= '0';
30           send <= '0';
31           wait_rtt <= '0';
32           wait_slot_start <= '1';
33        ELSIF CLK='1' AND CLK'event THEN
```

Figure 6 HDL Implementation

Following the functional checks the testing of the MAC layers of several nodes is conducted. The nodes are arranged in a schematic as shown in Figure 7. This schematic arrangement allows the testing of the

nodes as well as the gathering of statistics. As can be noted, the power of the software in speeding the design of not only single nodes, but several nodes, is beneficial.

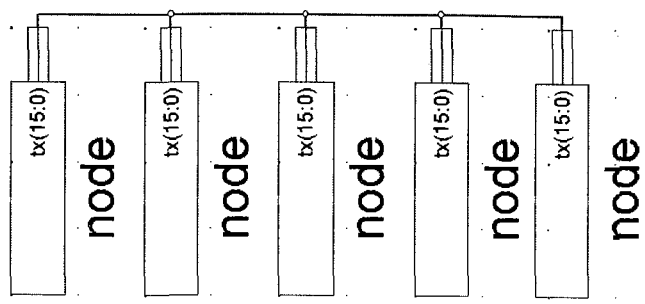

Figure 7 MAC Layer Node Arrangement

To verify the operation of the nodes within themselves and with each other the principal method of verification is the timing diagram, shown in Figure 8. The timing diagram is derived from a HDL testbench. This diagram enables one to visualize the input and output characteristics of the system. Statistics gathered from the timing verification also aid in determining that the system is operating as expected. Using Figure 5 and Figure 8, we can describe that they can be used as an example of the various parameters that can be set and monitored. Referring to Figure 8, The first two lines set the back off size, next is the collision indicator, the next two lines set the maximum times to back off before the node aborts. Reset is used to start the operation of the node, and to pull it out of operation as issued through an interrupt. The rtt delay is an optional parameter that allows for cases where the

round trip time is so large that it has to be waited out, typical of satellite Aloha-based systems. The slot available parameter indicates that a slot is available, this parameter is used in throughput analysis.

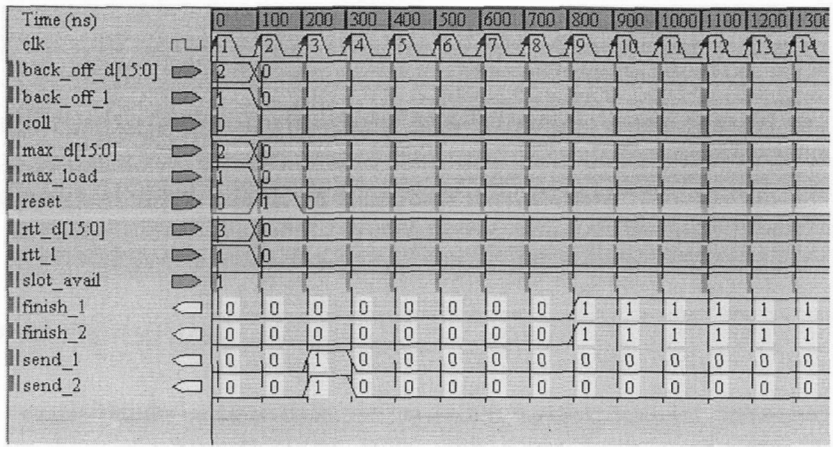

Figure 8 MAC Timing Diagram From HDL Testbench

During the design of the MAC layers for this project the main difficulties were successfully transferring the defined state diagrams into the software HDL code. In cases there are subtleties that are not easily handled in hardware. (This is a challenge for SDR using DSP, although modern FPGAs include DSP functionality.) Although solving these in hardware clearly gives a large speed advantage, which ultimately leads to bandwidth gains for the protocol and system.

This chapter gives an overview of the design implementation. The HDL code to implement the Aloha and CSMA protocols is extensive and is not included due to a non-disclosure agreement.

Chapter 3
Results

Here we will discuss the results of the simulations. Using randomized stimulus the individual MAC layers were tested as well as the overall system with vertical handoff capability.

Randomized Stimulus

The randomized stimulus used here was used to simulate data that would naturally occur randomly to the various MAC nodes involved in the simulation. The stimulus for each node was kept the same when different MAC nodes were evaluated, and when the handoff case was evaluated. This stimulus is based on Pseudo Random Bit Stream (PRBS) data, a commonly used random stimulus.

Measurement Apparatus

As discussed previously, the timing diagram obtained from the HDL testbench was able to indicate the throughput statistics. This was the primary objective measurement apparatus. During the design, subjective means were used to determine if the MAC nodes were behaving correctly. Later in the design these objective means were used

to determine the performance and any enhancements that could be made.

Aloha & CSMA Results

Here the results of both the Aloha and CSMA sections will be presented together since it facilitates easier comparison.

In Figure 9 we see the theoretical maximums of the various protocols [3]. It is important to note that these are based mainly on formulae and would not take into account non-idealities encountered in the real world. For example, processing and signaling time is finite and serves to degrade these statistics. What is shown is the througput, S, versus the offered load, G.

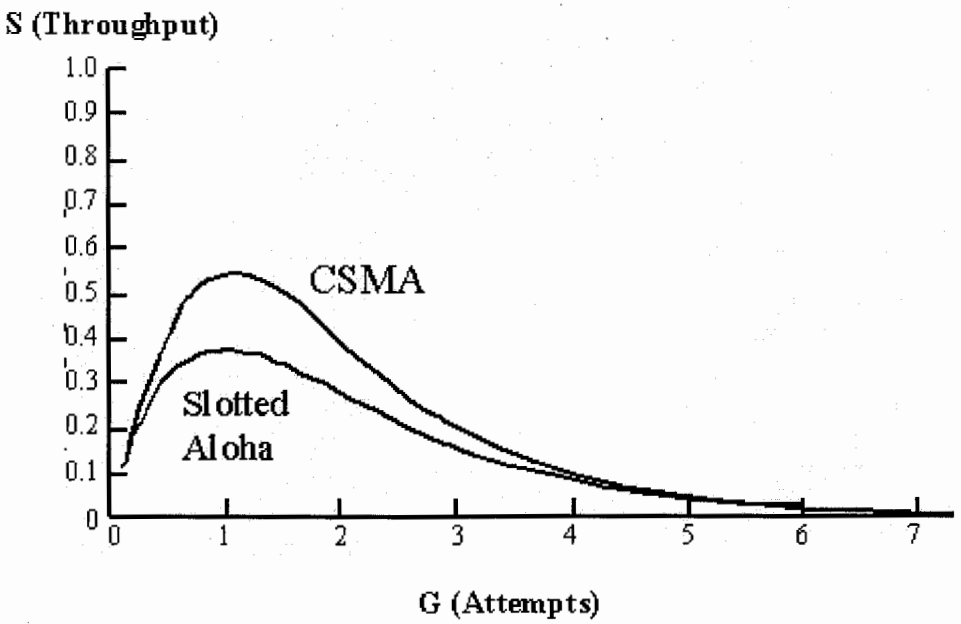

Figure 9 Slotted Aloha & CSMA Analytical Maximums

In Figure 10 we see the results obtained from the work done here. As can be noted the maximal values are very similar to the analytical maximums predicted by Figure 9. In order to obtain this desired performance, tuning of the HDL and FPGA implementation was necessary. With a different or more advanced FPGA or SDR systems better results may be obtained.

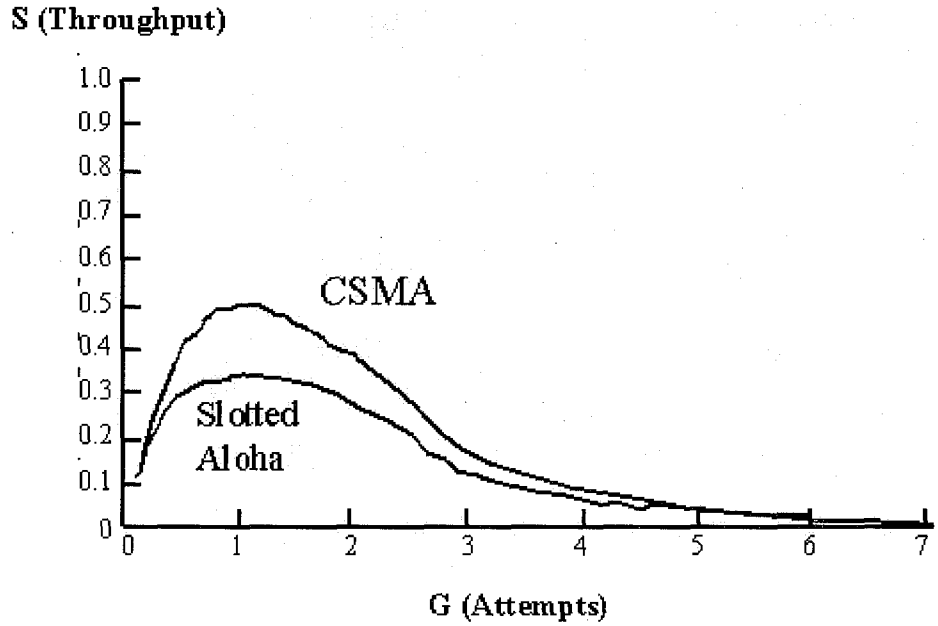

Figure 10 Slotted Aloha & CSMA Measured Results

Vertical Handoff Results

Here the results of the speed at which the vertical handoff can proceed will be presented. In order to determine the frequency at which a switchover can be made a special node containing both Aloha & CSMA MAC protocols was created. It was further assumed that an external

signal would trigger the event, such as a weak radio frequency signal indicator. The results are summarized in Table 1.

Table 1 Results for Vertical Handoff Operation

FPGA Freq. of Operation (MHz)	MAC Layer Switching Time (ns)
100	2.3
200	2
300	1.8
400	1.5

These results show that there is a linear decrease in switching time with increase in operational frequency of the FPGA, symbolized by clk, in the timing diagrams. Hence, as faster hardware becomes available the vertical handoff capabilities of SDR systems will be much greater.

Conclusion

The implementation of MAC layer configurability is shown through the implementation of two access schemes, Aloha & CSMA, using the same hardware. In addition it was shown that the time required to handoff between the two is inline with quality of service and processing capabilities. This makes the use of the FPGA invaluable in SDR, especially when it is considered that the underlying hardware implementation can be upgraded or changed while the device it is installed in the field.

Future work involves integrating the FPGA in a SDR system, as well as finding other efficiencies, and hardware capabilities that can increase throughput.

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