Robust Micromachining of Compliant Mechanisms for Out-of-plane Microsensors

by

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Abstract

Micro-Electro-Mechanical-Systems (MEMS) take advantage of a wide range of very reliable, and well established existing microelectronics fabrication techniques. Due to the planar nature of these techniques, out-of-plane MEMS devices must be fabricated in-plane and assembled afterwards in order to create out-of-plane three-dimensional structures. Out-of-plane microstructures extend the design space of the MEMS based devices and overcome many limitations of the in-plane processing. Nevertheless, several issues have to be addressed in order to integrate an out-of-plane structure into an existing process. These include robustness, yield, reliability, assembly technique, packaging and so forth. In this thesis we introduce an inorganic based post-CMOS compatible process upon which the mechanical structure for out-of-plane micro sensors and actuators can be fabricated. The hinge-less out-of-plane microstructures (compliant mechanisms) are mechanically robust structures that provide reliable electrical connection to the devices that are rotated out-of-plane. Fabrication of these structures by inorganic materials introduces several challenges to the process that have to be addressed.

Fabrication of micromechanical structures by silicon micromachining could significantly modify the topography of the substrate, which results in non-planarity and degradation of the mechanical performance of the structures. On the other hand, the residual stress of the structural layer has profound effect on the final shape of the out-of-plane microstructures. In particular, stress non-uniformity can cause severe structural deformation which deteriorates the device performance (e.g. linearity, sensitivity, and dynamic range), or can make the device assembly difficult or sometimes impossible.

To overcome the topography issue related to the freestanding structures and to control the stress profile of their structural layer, we have developed two novel techniques. The first technique is an unconventional planarization process that is achieved by modifying the etch property of the sacrificial layer. The second technique compensates the stress non-uniformity across the thickness of the sputter-deposited films by in-situ control of the film property during the deposition process. The practicality and versatility of these techniques has been illustrated through the fabrication of a functional out-of-plane three-axis thermal accelerometer, which has a significant and growing share in the consumer electronics market.

Keywords: Planarization; Stress Anisotropy; 3-axis Thermal Accelerometer; Nickel Silicide; Out-of-plane; Micromachining

To my loved ones

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Table of Contents

List of Figures

List of Tables

1. Introduction

Micro-Electro-Mechanical-Systems (MEMS) take advantage of a wide range of very reliable and well established microelectronics fabrication techniques. Due to the planar nature of these techniques, most out-of-plane MEMS devices are first fabricated in-plane and then assembled in order to create high aspect ratio three-dimensional structures. Out-of-plane micro structures extend the design space of the MEMS based devices and overcome many limitations of the in-plane processing. Nevertheless, several issues have to be addressed in order to integrate an out-of-plane structure into an existing process. These include robustness, yield, reliability, assembly technique, packaging and so forth.

In this thesis we introduce a post-CMOS compatible process, based on inorganic thin films, upon which the mechanical structure for out-of-plane micro sensors and actuators can be fabricated. The hinge-less out-of-plane microstructures are mechanically more robust than the hinged structures and provide reliable electrical connection to the devices that are rotated out-of-plane. These microstructures, also known as compliant mechanisms, gain the necessary mobility for their assembly process through deformation of their elastic component. Fabrication of these structures from inorganic materials introduces several challenges to the process that have to be addressed.

Fabrication of micromechanical structures for sensors and actuators by silicon micromachining could significantly modify the topography of the substrate, which results in non-planar surfaces and therefore, degradation of the mechanical performance of the structures. On the other hand, the residual stress of thin films, which form the structural layer of the out-of-plane microstructures, has profound effect on the final shape of the freestanding and out-of-plane microstructures. In particular, stress non-uniformity can cause severe structural deformation which deteriorates the device performance (e.g.

linearity, sensitivity, and dynamic range), or it makes the device assembly difficult or sometimes impossible.

To overcome the topography issue related to the freestanding structures and to control the stress profile of their structural layer, we have developed two novel techniques. The first technique is an unconventional planarization process that is achieved by modifying the etch property of the sacrificial layer. The second technique compensates the stress non-uniformity across the film thickness by in-situ control of the film property during the deposition process. The practicality and versatility of these techniques will be illustrated through the fabrication of a functional out-of-plane three-axis thermal accelerometer, which has a significant and growing share in the consumer market. These processes are both low temperature and post-CMOS compatible.

1.1. Significance of out-of-plane structures

The limits of traditional lithographic microfabrication processes have constrained microelectronics and microelectromechanical systems to the substrate plane. While the commercially available surface micromachining, bulk micromachining and CMOS-based processes are able to create freestanding structures, the majority of these devices operate in the same plane as the substrate plane. Out-of-plane microstructures offer a completely new design space to create devices with advantages and capabilities previously not possible in ordinary planar structures. Out-of-plane microstructures have numerous applications in micro optical, thermal, and RF systems [1], [2], [3]. They can provide thermal isolation from the substrate that is necessary for many transducers, and can also add extra axes of sensitivity to the in-plane devices. The thermal accelerometer and gyroscope are prime examples of the potentials of these structures [3], [4].

1.2. Inorganic versus organic

Many researchers [5], [6] have demonstrated the possibility of fabricating out-of-plane structures using organic materials such as SU8, PMGI (Polymethylglutarimide), Polyimide, etc. Polymers in general have much lower Young's modulus to yield strength

ratio than most silicon based materials and metals, and hence are mechanically more suitable materials to create compliant mechanisms; structures which are expected to undergo large deformation. However, practical difficulties in integrating a polymer-based fabrication technology into existing silicon-based processes have hindered the industry from adopting such processes. The most important and inherent drawbacks of using an organic material in a silicon based microfabrication foundry are deformation of the structures under long-term stress and contamination. Many polymers still out-gas even when they are cured. The out-gassing makes working with these materials very difficult in vacuum systems. Organic material easily re-sputtered in many common processes such as Reactive Ion Etching (RIE) and sputtering. The re-sputtered material covers the equipment chamber and cause cross-contamination. Sputtered non-organic films easily lose their adhesion to the bottom layers due to this contamination. Furthermore, the re-sputtered organic material becomes trapped in the coating material and changes the mechanical and chemical property of the film. Using the non-organic material such as metals or silicon-based materials (oxide, nitride, etc) eliminates these problems.

1.3. Motivation

The needs of the MEMS industry are the driving force behind this research. A low-cost, low temperature and reliable process for fabricating out-of-plane structures broadens envisioning for new devices that can thrive in today's highly competitive market. The work presented in this thesis introduces an inorganic based post-CMOS compatible method upon which out-of-plane transducers can be created. While in this thesis we do not insist on fabrication of a particular transducer, but the three-axis thermal accelerometer was chosen to demonstrate a real-world application because of its market potential, ease of design and characterization, and well-studied operating principles [3].

1.4. Chapters outline

The planarization technique for eliminating the step between a structure and its anchor is presented in chapter 2. In chapter 3 we introduce a compensation technique to overcome the effect of stress anisotropy across the thickness of the sputter-deposited films. A generic application for these two techniques is illustrated in chapter 3, where the fabrication process for a 3-axis thermal accelerometer is explained, and the test result is presented. A detailed run-sheet of the fabrication steps for the thermal accelerometer is included in Appendix A.

2. Planarization

Fabrication of micromechanical freestanding structures for sensors and actuators by silicon micromachining could modify the topography of the substrate significantly [7]. In conventional surface micromachining (e.g. POLYMUMPS), 0.5-2 μm phosphosilicate glass (PSG) is often used as a sacrificial layer. The patterning of the PSG layer creates surface non-planarity. This surface non-planarity will result in a structure with a step, as shown in Figure 1. Local stress concentration may take place at the corners of these steps, which degrades the mechanical performance of the structure. During the actuation or assembly of an out-of-plane structure, stress accumulation at the structure's step can easily exceed the yield strength of the material and lead to the structure failure. Furthermore, the non-planarity results in complications in subsequent processing associated with lithography and step coverage, as in the case of multilayer interconnection of modem integrated circuit fabrication [7]. These difficulties include: variations in resolution and line width near the steps due to the limited depth of focus of exposure systems, and possible discontinuous metal or dielectric coverage of features with vertical sidewalls [7]. Therefore, planarization is important to increase the mechanical robustness of the structures, and the fabrication process yield.

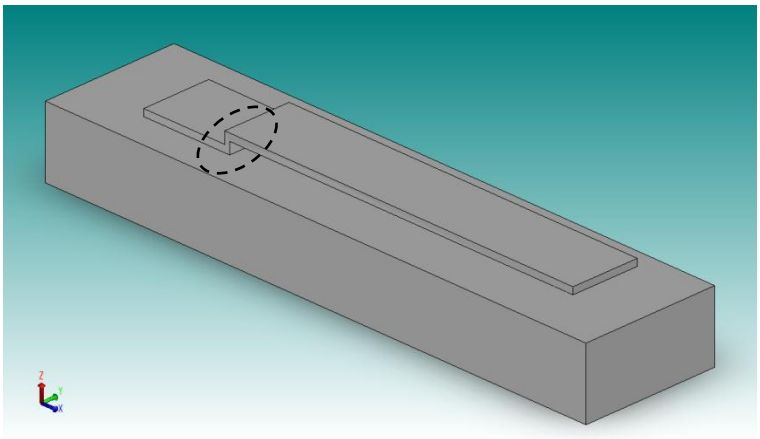


Figure 1: A freestanding microstructure fabricated using conventional sacrificial surface micromachining.

The planarization technique presented in this chapter takes advantage of the nickel silicide technology to enhance the reliability of the freestanding structures and the compliant mechanisms by:

- Increasing the stiffness and mechanical robustness of the structures by eliminating the step between the structure and its anchor, and achieving planarization without using Chemical Mechanical Polishing (CMP).
- Eliminating the step coverage issue related to the deposition processes.

We use a layer of amorphous silicon (a-Si) as a sacrificial layer, which is locally converted to nickel silicide to form the anchors. High etch selectivity between silicon and nickel silicide in the Xenon Difluoride (sacrificial layer etchant) enables us to use the silicide to anchor the structures to the substrate. The formed silicide has the same thickness as the sacrificial layer; therefore, the structure is practically flat.

2.1. Planarization techniques

Different planarization techniques of the substrate surface for IC fabrication have been developed. The level of planarization varies significantly from one method to the other. It could be as little as tapering the sharp corners of the formed structures without change in the surface level across the wafer due to the substrate topography, and as far as a completely planar surface across the wafer. Followings are the most common planarization techniques:

- Reflow of doped silicon dioxide
- Reflow of metals (aluminum alloys)
- Re-sputter deposition
- Selective deposition of Chemical Vapour Deposition (CVD) tungsten
- Spin-on glass
- Plasma etch back of sacrificial layer
- Chemical Mechanical Polishing (CMP)

Low Pressure Chemical Vapour Deposition (LPCVD) deposited silicon dioxide requires high annealing temperatures to gain sufficient reflow for reducing substrate topography. A PhosphoSilicate Glass (PSG) requires temperatures in excess of 1000ºC

to reflow significantly [8]. However, BoroPhosphoSilicate Glass, BPSG, yields a better performance as it reflows at temperatures below 900 ºC; nevertheless, the reflow temperature of the film strongly depends on its phosphorous and Boron content [8]. Due to its extremely high thermal budget, this technique has limited application.

Metal reflow can also be used as planarization technique in processes that involve aluminum or aluminum alloy (aluminum-copper) as a contact or via material. In this process, the wafer is heated to 450-500ºC to help fill the vias and planarize the surface. Introducing germanium to the film can reduce the reflow temperature to below 400ºC [9]. Aluminum-Copper deposition with conventional techniques results in voids, gaps and poor via filling. By reacting Germane (GeH_4) with the as deposited Al-Cu film, high aspect ratios vias can be filled without leaving any voids [9]. However, all reflow techniques result in local and partial surface planarization and the wafer's overall topography remains the same.

In the biased sputter deposition process, due to the energetic ions that bombard the growing film, deposition and sputter-etching (re-sputtering) can take place at the same time. The relative rate of each process depends on the ion flux, angular distribution and the ion energy. The re-sputtering rate (yield per incoming ion) is relatively low when the incoming ions arrive at shallow angles, and it reaches its maximum when the angle of incident is around 60° [10]. This rate rapidly declines and becomes very low again when the ions hit the surface at right angle. In biased sputtering, different facets can be formed, or removed because re-sputtering yield is different at different angles. During sputter-deposition of a film on a structured substrate, surface features can be eliminated by properly controlling the bombarding ions angle of incident. If re-sputtering rate on the side walls of the surface features is higher than the deposition rate, as the film becomes thicker, the size of these features become smaller and they will eventually disappear [10]. The angle of incident can be controlled by the bias voltage which defines the ion energy. The same technique can be used to planarize thick films using Ion Milling. Figure 2 illustrates the effect of faster milling rate on the sidewalls of a thick non-planar film and its subsequent planarizing outcome. Although surface planarization can be achieved by tuning the deposition and re-sputtering rate, at high re-sputtering rates surface damage and void formation can occur in narrow spaces (e.g. via bottom) [11].

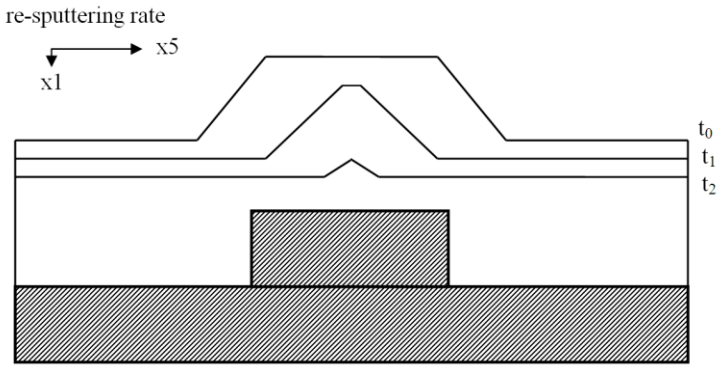


Figure 2: Planarization by re-sputtering (ion-milling).

Tungsten selective deposition on silicon substrate by Chemical Vapour Deposition (CVD) is a practical technique to fill in small via holes in multilevel metal integrated circuits [12]. When silicon dioxide is used as the dielectric and insulation layer on silicon, via holes can be filled by tungsten plugs by a two phase CVD process. Initially, tungsten hexafluoride gas (WF_6) reacts with the silicon surface and a thin layer of tungsten is deposits on the bottom of the vias. The thickness of this layer is limited because when the exposed silicon is covered by the tungsten layer, the reaction stops. For the second phase of the deposition, hydrogen is introduced. Tungsten hexafluoride reacts with the atomic hydrogen (hydrogen reduction) and tungsten is deposited. The disassociation of the H_2 to atomic hydrogen easily takes place at the metal surface but not on the dielectric surface; therefore the overall deposition process is selective. Although this process has demonstrated the ability to fill via holes, there are many problems that have hindered the adoption of technology by the industry (lateral growth, tunnelling).

Spin-on Glass (SOG) is either a mixture of silicon dioxide in a solvent with zero organic content, or a Siloxane (Si-O-Si linkage) polymer chain. The properties and functionality of spin-on glass materials is largely controlled by the various components of the polymer structure. Spin-on glass can be spun like a photoresist layer but it turns to SiO_2 when it is baked and cured. Due to its low viscosity, the spin-on glass can fill in the holes and planarize the substrate surface. The major problems with the spin-on glass are the organic content of the film even after proper curing of the film and the poor quality of the oxide (compare to the CVD or thermal oxide). Spin-on glass can also be used in the plasma etch back planarization process as the sacrificial layer [13]. The

advantage of using spin-on glass instead of other polymers in etch back planarization process is that the spin-on glass can be spun into much thinner layers (less and 100 nm).

In plasma planarization [7], a low viscosity sacrificial layer (usually photoresist, polyimide or spin-on glass) is used to coat the uneven substrate surface to obtain a practically flat surface. Subsequently, plasma etching is used to etch-back the sacrificial coating layer, during which the etch rate of substrate and sacrificial layer should be equal to form a planar surface after the etching. Coating of a structured substrate even with a low viscosity polymer could result in an uneven surface. This issue is more significant when the surface feature density varies (micro-loading) and could result in local planarization.

Once considered a technique too crude and dirty for IC fabrication, CMP emerged as a new method of achieving complete planarization for submicron ULSI applications [14], [15]. With the correct polishing pad, slurry, and planarizing machine tool, thin layers of insulating material and even metals can be removed and brought down to the point where eventually the layer is a plane surface. However, this method suffers from difficulties in planarity control (feature size dependency, hollow formation in wide features, over-polishing of large array areas), and residual contaminations [7].

2.2. Nickel silicide

Silicides have been extensively used in the CMOS technology to reduce the series and the contact resistance to the gate, source and drain regions [16]. Nickel silicide's lower thermal budget, lower resistivity, reduced silicon consumption, and nickel-diffusion-controlled formation have overcome the limitations of the cobalt silicide ($CoSi_2$), and made the nickel silicide the first choice for CMOS technologies below 65nm [17], [18]. The fact that formation of nickel silicide is controlled by nickel diffusion is a significant advantage which results in silicide films with much smoother surfaces and interfaces [18].

Nickel silicide has different phases, but numerous reports agree that the predominant phases are Ni_2Si, NiSi, and $NiSi_2$ [17]. The Ni_2Si forms at the temperature

range of 250-300°C, but above 300°C it transitions rapidly to NiSi. At higher temperatures (above 600°C) the mono-silicide transforms to $NiSi_2$ [18]. Figure 3 illustrates the correlation between nickel initial thickness, t_n, the formed silicide thickness, t_s, and the consumed silicon thickness, t_c, for nickel mono-silicide phase (NiSi). The formed silicide is 2.2 times as thick as the initial nickel, and consumed silicon thickness is 1.83 times as much. As it is shown in the figure, the formed silicide grows slightly above the initial silicon interface. The protrusion is only 16.8% of the total silicide thickness, t_s [18].

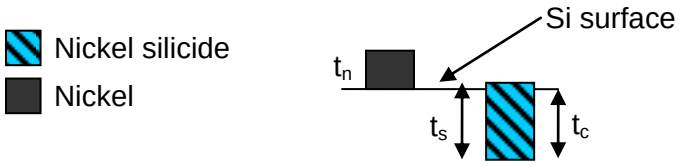


Figure 3: The thickness ratio between nickel, nickel silicide, and silicon consumption in the nickel mono-silicide (NiSi).

Table 1 compares the crystalline properties of nickel silicide at its different phases [18]. Silicon rich nickel silicide ($NiSi_2$) has the largest silicon consumption ratio to the nickel initial thickness among the predominant phases. This high ratio is an advantage when thick layer of silicon has to be converted to silicide. However, the formation temperature of this phase (above 600°C) is too high to be adopted by our process. Above 350°C, the nickel silicide film mostly consists of NiSi. This temperature is low enough for a post-CMOS compatible process, and amorphous silicon (the sacrificial layer) can also be deposited at these temperatures by taking advantage of PECVD technique.

Table 1: The thickness ratio between nickel, nickel silicide, and silicon consumption in the nickel mono-silicide (NiSi).

Phase	**t_n**	**t_s**	**t_c**
Ni_2Si	1	1.47	0.91
NiSi	1	2.2	1.83
$NiSi_2$	1	3.61	3.66

Nickel silicide etch rate is very low or almost zero in most acids and chemicals [19]. The close-to-zero etch rate of the nickel silicide in XeF_2 gas makes it a good candidate for selectively etching the sacrificial layer in our process. The diffusion rate of nickel into silicon dioxide and nitride is extremely low. Therefore, these films can be used as a masking material to selectively diffuse nickel into silicon.

Mechanical properties and possible applications of the nickel silicide in MEMS have been studied by a few researchers [19], [20], [21]. Qin et al [19], [20], have measured electrical and mechanical properties (resistivity, surface roughness, Young's modulus, and stress) of the nickel silicide formed on polysilicon and crystalline silicon substrate. They even managed to fabricate simple mechanical structures like micro-bridges and micro-cantilevers using silicon dioxide as diffusion mask. Bhaskaran et al [21], took advantage of high etch resistivity of nickel silicide, and used it as etch mask in silicon bulk micromachining in potassium hydroxide. We were the first group that introduced a planar surface micromachining process using nickel silicide [22]. This process enabled us to improve the performance of a Pirani pressure sensor in atmospheric pressures by reducing the device gap size to 50nm. To extend the application of our process to the other micro sensors and actuators, we had to enhance and modify the original method [23], [24].

Conventionally, the fabrication of a freestanding structure starts with deposition and patterning of a sacrificial layer. The structural layer is deposited afterwards. The structure is anchored to the substrate through the opening of the sacrificial layer. This process results in a non-planar structure with a step between the structure and its anchors, which is equal to the thickness of the sacrificial layer (Figure 1). Besides the mechanical degradation due to this height difference, deposition process of the structural layer has to be conformal, otherwise poor step coverage will further deteriorate the structure robustness. Instead of opening windows in the sacrificial layer to anchor the structure to the substrate, we locally modify the property of the sacrificial layer by converting it to silicide. The modified sacrificial layer is highly etch-resistant to the sacrificial layer etchant (XeF_2). This process creates patches of highly etch resistant silicide in the sacrificial layer. During the release step (etching the sacrificial layer), the structure remains anchored to the substrate through these patches (Figure 5). The

formed silicide has the same thickness as the original layer which results in a planar structure.

2.3. Design considerations

Before describing the planarization process in detail, we have to emphasize on several criteria and principles upon which a particular material or an implementation strategy was chosen. During the development phase of the process, we sometimes had to replace a material for another to overcome an undesirable outcome, or completely substitute a process with a difference technique to meet our requirements. The materials and the processes selection criteria are discussed here.

2.3.1. Nickel deposition (evaporation versus sputtering)

Nickel thin films can be deposited through several techniques such as, electroplating, electroless plating, sputtering and evaporation. The chemical based deposition techniques tend to leave some traces of other elements and compounds in the film which can hinder the silicide formation. On the other hand, pure elemental nickel can be deposited by sputtering or evaporation techniques. Sputtering is easy and convenient way of nickel deposition with good uniformity, and relatively fast deposition rates at moderate powers (up to 8 Å/s at 5.5 W/cm^2). Nickel is a magnetic material with high magnetic permeability, and in order to sputter nickel from a magnetron (sputtering source with a magnet), one has to use very thin targets or use specially designed sputtering sources (with stronger or unbalanced magnets).

Alternatively, nickel can be deposited by thermal or e-beam evaporation. Nickel forms alloys with most of the common materials that are used as heater in the thermal evaporation; therefore, it has to be thermally evaporated from an alumina coated heater or basket. The melted nickel does not wet alumina and it forms a sphere with very large contact angle. The small contact area between the melt and the heater reduces the nickel evaporation rate. To compensate for the lower evaporation rate, the heater power rating has to be increased significantly which shortens the heater's life time and causes substrate heating the same time. Using e-beam evaporation alleviates the nickel thermal

evaporation challenges considerably but the evaporation rate is much lower than that of the sputtering. Nickel deposition rate using the e-beam technique is only a few angstroms per second (1-2 Á/s).

Nickel silicide films formed by annealing an evaporated nickel are known to be mono-silicide (NiSi), with the composition being very close to 50% nickel and 50% silicon. Sputtered nickel, unlike the evaporated nickel, requires more thermal effort to form NiSi. Sputtered nickel has to be annealed at temperatures as high as 600°C to form the mono-silicide [25], which is too high and incompatible for a post CMOS process.

We initially used a thin foil of nickel as the target to sputter-deposit nickel on silicon and to form silicide. We tried different deposition conditions but the sputtered film did not react with silicon after we annealed the film at 400°C. The analysis of the as deposited film (before annealing) by Electron Dispersive Spectroscopy (EDS) showed significant concentration of oxygen in the film (up to 14%). The high oxygen content of the film could be one of the main reasons that no silicide was formed at those conditions. The primary source of the oxygen in the sputtered film was from the exposure to the atmosphere and the microcrystalline structure of the film (high oxidation rate). This phenomenon could also be attributed to variations in the diffusivity of metals in silicon, based on the metal thin film deposition technique [25]. Repeating the same experiment with thermal or e-beam evaporated nickel resulted in formation of nickel silicide at temperatures as low as 350°C; therefore, we chose evaporation to deposit nickel in our process. Table 2 shows the difference in the oxygen concentration of a sputter deposited and an evaporated nickel film after exposure to the atmosphere.

Table 2: Comparison of oxygen concentration in sputtered and evaporated nickel films.

Deposition method	O_2 (atomic %)	Ni (atomic %)
Sputtering	14	86
Evaporation	5	95

2.3.2. The etch-stop layer

Before the sacrificial layer deposition and formation of the anchors, an etch-stop layer has to be deposited (formed) on the silicon substrate. This layer has to have a very low etch rate in Xenon Difluoride (XeF_2) in order to protect the silicon substrate during the release step, otherwise the XeF_2 attacks the substrate. In addition to having a low etch rate in XeF_2, this layer has to have another important characteristic; the sacrificial layer (a-Si) and the nickel silicide have to adhere very well to this layer. Without enough adhesion, the stress induced by the nickel, and the formed silicide during the annealing step could cause the film to delaminate from the substrate and form stress-humps (blisters) [26], [27]. Figure 4 shows the formed stress-humps on a sample with poor adhesion between the sacrificial and the etch stop layer (on silicon dioxide).The stress-hump formation becomes a major issue with relatively thick a-Si layers (a few hundreds of nanometres) [23].

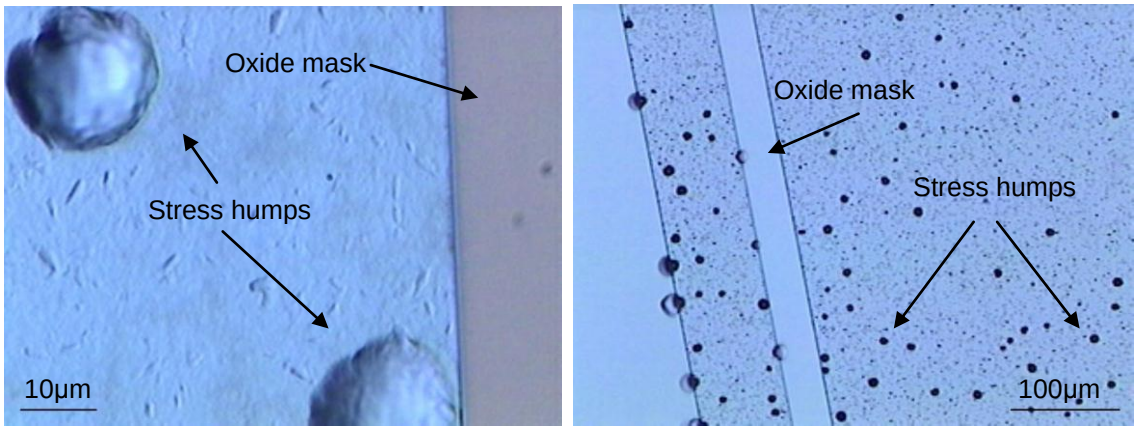


Figure 4: Stress induced humps on silicide sample after annealing at 350°C. There is no stress-hump over the areas covered by the oxide diffusion mask.

In order to apply our process to large structures (a few hundreds of microns across) and to facilitate the structure release process, we had to increase the sacrificial layer thickness to hundreds of nanometres. Even with etch holes in the structure, releasing a large structure with a very thin sacrificial layer (e.g. 100 nm) could be very

time consuming, and sometimes impossible. Lack of sufficient adhesion between the etch-stop and the top silicide layer limits the maximum thickness of the sacrificial layer.

The nickel-silicide based surface micromachining process that we initially introduced in [22] used thermal oxide as the etch-stop layer on the silicon substrate. The adhesion of the sacrificial layer and the formed nickel silicide to the bottom oxide layer was very poor, which had limited the process to the applications with extremely thin sacrificial layers (up to 100 nm). For thicker a-Si layers, nickel film thickness had to be increased to provide enough supply of nickel to completely consume the silicon and form the silicide (anchor). We noticed that as we increase the nickel thickness the stress-hump formation becomes more significant and with nickel layers thicker than 100 nm the annealed film was covered with blisters. Obviously the expansion of the film during silicide formation results in high stress values and the force exerted by the film exceeds the film adhesion to the etch-stop layer which causes the film to delaminate from the bottom layer and form the stress humps.

Increasing the a-Si deposition temperature (up to 350ºC) slightly improved the adhesion but we still observed major stress-hump formation with nickel layers thicker than 100 nm. We later attempted to replace the thermal oxide with another etch-stop layer. PECVD silicon nitride showed much better adhesion but unfortunately the etch rate of nitride is relatively high in XeF_2 and it is also a strong function of deposition parameters. PECVD silicon dioxide on the other hand stands to XeF_2 very well, but it did not show enough adhesion to the sacrificial layer and the formed nickel silicide to be considered for our process.

We came up with the idea of replacing the dielectric etch-stop with a thin layer of silicide in order to solve the adhesion problem. We thought that this layer diffuses both into the substrate and the a-Si layer and would become a bonding layer between the sacrificial layer and the substrate. Experiment with silicide revealed that the a-Si and the top silicide layer adhere much better to a thin layer of silicide compare to the other films such as oxide or nitride. In [23], we introduced a modified process which used a thin layer of nickel silicide as the bottom etch-stop layer. To form the silicide etch-stop layer we deposited a very thin layer of nickel (10 nm) by e-beam evaporation on the substrate

and deposited the PECVD a-Si on top of it. A short annealing step was required to from the bottom etch-stop layer.

With the available equipment (separate e-beam evaporator and PECVD machines), it was impossible for us to evaporate the bottom nickel and deposit the PECVD a-Si without breaking the vacuum (exposing the nickel film to atmosphere). Exposure to atmosphere partially oxidizes the nickel which deteriorates its adhesion to the a-Si and the top silicide layer after silicidation. Although replacing the bottom oxide layer with a layer of nickel silicide improved the film adhesion and reduced the stress hump formation significantly, nickel oxidation was still an issue which rendered the process hard to control and reproduce.

To avoid the exposure of nickel to atmosphere, we had to deposit the nickel in our Cluster Tool and then transfer the wafer to the PECVD chamber for the a-Si deposition without breaking the vacuum. In a Cluster Tool machine, different process chambers are connected to each other via an Ultra High Vacuum (UHV) Isolation and Transferring Zone (ITZ), and a robotic manipulator moves the sample between different chambers. However, the only available technique for nickel deposition in our system was sputtering. As we mentioned earlier, the sputtered nickel needs much higher thermal budget to react with silicon and to form silicide; therefore, we could not use the nickel to further improve the adhesion. It had to be replaced with another material.

Our experience with Nichrome (80% Nickel, 20% Chromium) had shown that it forms a very thin layer of silicide even when it is sputtered at room temperature. Biased sputtering followed by high temperature annealing (350°C) further enhances the silicide formation. The formed silicide at this temperature has excellent etch resistivity to XeF_2 and excellent adhesion to a-Si and nickel silicide. However, silicide formation is very sensitive to presence of oxygen during metal deposition and requires base pressures below 10^{-7} Torr. Furthermore, film exposure to atmosphere after deposition hinders the silicide formation as well (similar to nickel). To avoid the Nichrome film exposure to the atmosphere before sacrificial layer deposition, the entire process was carried out in our Cluster Tool machine equipped with UHV processes and transfer chambers.

The experimental results with Nichrome were very promising and the formed Ni-Cr silicide showed excellent adhesion to the top layers. By monitoring the base pressure of the chamber before deposition and long enough pump-down period, the process was very well controlled and reproducible. We monitored the partial pressure of the different gas species in the chamber using a quadrupole Residual Gas Analyzer (RGA). This was a crucial step in our process since most pressure gauges are calibrated for nitrogen and partial pressure of other gas species in the chamber could be much higher (up to an order of magnitude) than the measured pressure by the gauge. Difference in the gas species partial pressure can significantly affect critical processes which are sensitive to the presence of certain gas types (water vapour in our case).

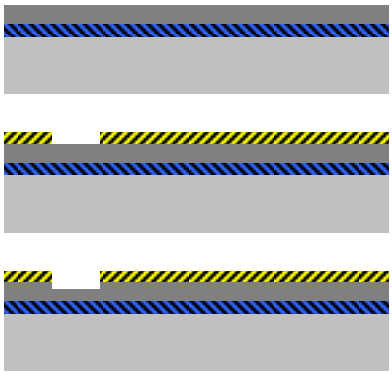
Turbomolecular pumps are the most common pumps in high vacuum systems. They provide high pumping speed (*l/s*) and sufficient compression ratio for different gas species. The compression ratio could be as high as 10^9 for nitrogen and as low as 1000 for lighter species like hydrogen. The pumping speed is also much lower for the lighter gases. Water vapour has the highest partial pressure among the other gas species in the chambers equipped with a turbomolecular pump due to its low compression ratio and pumping speed and its relatively high concentration at the pump outlet (atmosphere). Although the average pressure of the chamber can be brought down into the 10^{-7} Torr range relatively fast (as can be verified by the gauge) the water vapour pressure in the chamber usually requires much longer pumping cycles and must be verified by RGA readout. In our sputtering chamber the base pressure drops below $5x10^{-7}$ Torr in less than 5 minutes (after loading the sample), but the chamber has to be pumped down for more than an hour to reduce the water vapour pressure below $5x10^{-7}$ Torr which is necessary to prevent the Nichrome oxidation and to promote the silicide formation.

2.4. Planarization process

Different steps of the planarization process is illustrated Figure 5. The thin etch-stop silicide layer is formed by sputtering 20 nm NiCr (Nichrome; 80% Nickel, 20% Chromium) on the silicon substrate. We used the MVSystem Cluster Tool for sputtering NiCr and for PECVD amorphous silicon deposition. Our Cluster Tool is equipped with two UHV sputtering chambers, two UHV PECVD chambers, and a UHV Isolation and

Transferring Zone (ITZ). For NiCr sputtering the chamber base pressure was below 10^{-7} Torr, and during transferring the sample from the sputtering to the PECVD chamber the ITZ pressure was kept below 10^{-6} Torr. After DC sputtering of 20 nm thick NiCr (Argon pressure 1 mTorr, 3" target at 150 Watts power rating, substrate bias -50 V) and transferring the sample into the PECVD chamber, 300 nm thick a-Si was deposited on the NiCr film. Amorphous silicon was deposited using pure Silane chemistry (chamber pressure 350 mTorr, substrate temperature 350°C, RF power 2 watts). The Nichrome:a-Si stack was annealed in a convection furnace at 350°C in forming gas atmosphere (5% hydrogen, balance in nitrogen) for 10 minutes to form the etch stop layer (bottom silicide). The forming gas prevents the a-Si from oxidation during the annealing process. Nichrome reacts with the silicon substrate and the a-Si layer at the same time, and it is totally consumed by the silicon to form the bottom silicide. Diffusion into both the substrate and the a-Si layer significantly improves the a-Si layer adhesion to the substrate and prevents the stress-hump appearance during the top silicide layer formation.

We used the FEI Nova NanoSEM 430 EDAX analyzer to study the formed silicide composition utilizing the Energy Dispersive Spectroscopy (EDS) technique. The analysis result showed that the nickel and chromium concentration of the silicide layer is very close to that of the sputtering target (nickel 80%, chromium 20%). The slight discrepancy in the film composition is perhaps due to the sputtering yield difference between nickel and chromium. The measured composition of the formed silicide film on the substrate was Si-60.92%, Ni-30.80%, Cr-8.28%.



a) Sacrificial layer with bottom silicide layer

b) Patterned diffusion mask (oxide)

c) Partially etched a-Si layer in RIE with diffusion mask

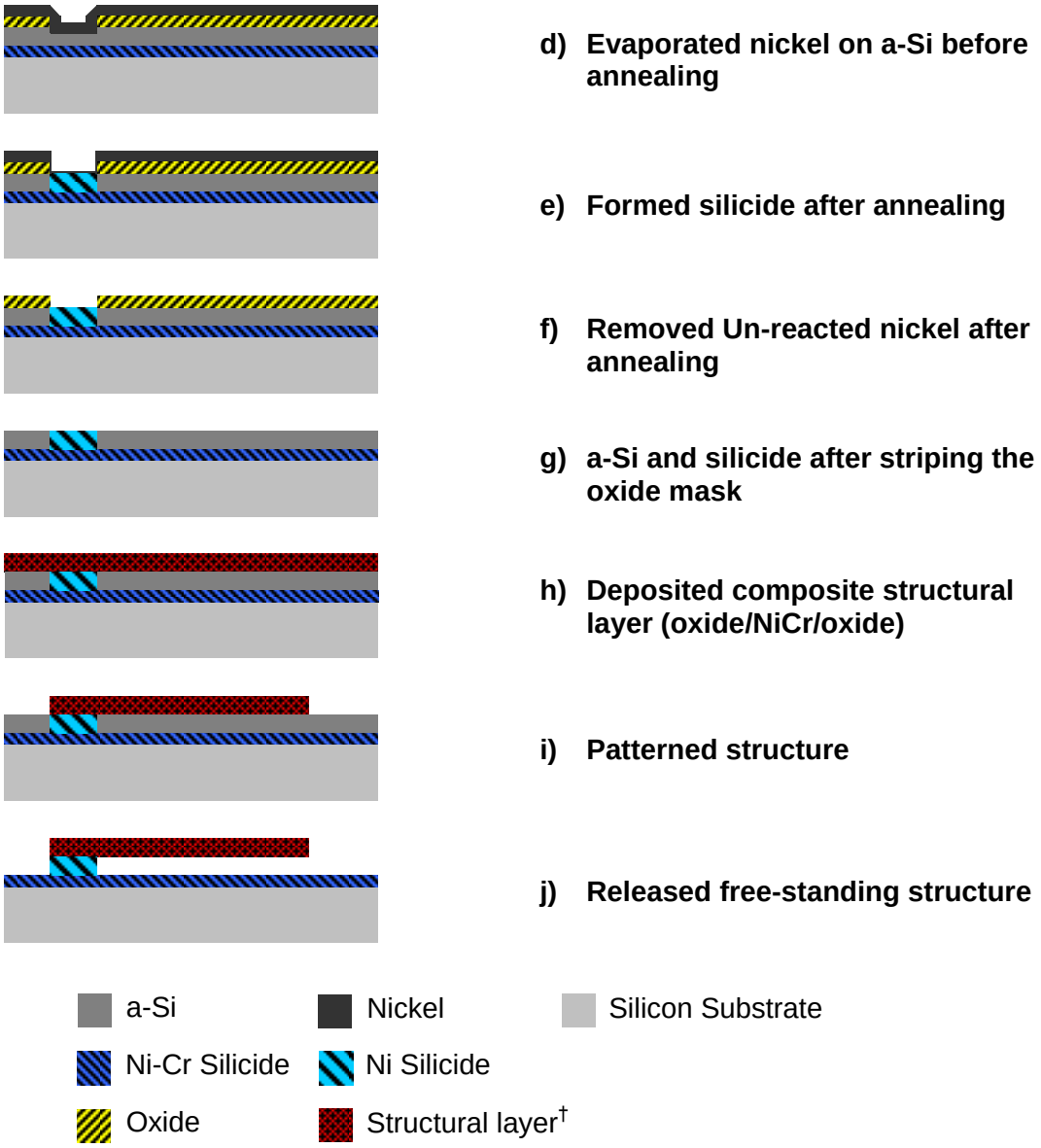


Figure 5: ***Fabrication steps of the planarization process. †For illustration clarity, the composite oxide/NiCr/oxide layer is shown as a single structural layer.***

After the sacrificial layer deposition and the bottom silicide layer formation, a 200 nm thick layer of PECVD oxide was deposited to act as a diffusion mask for the silicidation process. The first mask was used to open the anchor windows into the oxide layer. To compensate the growth of the nickel silicide above the original a-Si surface, part of the a-Si was etched by RIE using a mixture of CF_4 and oxygen (10:1). The a-Si etch depth was equal to the amount that the silicide grows above the surface. This

guarantees that the silicide layer has the same thickness as the a-Si layer. To form the silicide and make the anchors, a 200 nm thick nickel film was evaporated and annealed. We annealed the film in the forming gas atmosphere at 350°C for 45 minutes. We deposit enough nickel on silicon so that after annealing the a-Si is entirely consumed by the nickel to form the anchors (the top and bottom silicides actually merge). We used the Bestec e-beam evaporation system to deposit nickel. During evaporation the chamber pressure was about $5x10^{-7}$ Torr and the deposition rate was about 1 Å/s. After annealing, the non-reacted nickel was etched by a mixture of H_2SO_4 and H_2O_2 (1:1) at 70°C for 5 minutes and the oxide layer was etched by Buffered Oxide Etchant (BOE). PECVD oxide etch rate in BOE was about 250 nm/min.

After the anchors were formed, we deposited and patterned the structural layer on the substrate to fabricate the desired mechanical structures. The mechanical structures were released and assembled manually using a mechanical probe to form an out-of-plane configuration.

The structural layer is a symmetrical tri-layer film consisting of two layers of PECVD oxide (250 nm thick each), on top and bottom of a Nichrome film (300 nm thick). The bottom oxide, Nichrome, and top oxide layers are deposited first and then patterned using a single mask with self-alignment technique. The top and bottom oxide layers were etched in RIE, and the Transene 1020AC Chromium etchant was used to wet etch the Nichrome film. The composite film minimizes the overall stress level of the structural layer, and the symmetry of the structure eliminates its deformation due to the stress mismatch between different layers [28]. We used XeF_2 gas to etch the sacrificial layer and release the structure. XeF_2 is a white crystal that sublimes with a vapor pressure around 4 Torr at room temperature. The XeF_2 gas is an isotropic etchant for silicon. The etch rate of silicon in XeF_2 is a strong function of exposed silicon, but it can reach as high as 4 μm/min. The etch selectivity between silicon and silicon dioxide in XeF_2 gas is better than 1:2000. The etch selectivity is much higher for most of the metals and the silicides [29], [30].

2.5. Planarization process results

Figure 6.a shows the SEM image of an assembled 3D compliant mechanism fabricated using our process. The close up view of the structure's anchor is shown in Figure 6.b. Although there is no height difference between the structure and its anchor, the anchor (the silicide) has a rougher surface compared to that of the structural layer which creates the illusion of having a discontinuous film. The structure is the sensor-plate of a 3-axis thermal accelerometer [3], which provides thermal insulation from the substrate for the sensor, and adds the third sensing axis (z-aixs) to the device. The structure has been buckled out of plane and locked in place [31], [32], [33]. To assemble the structure to the out-of-plane configuration, tip of the T-shape cantilever (main cantilever) is pushed back using a probe. When tip of the main cantilever passes the locking cantilever, the probe is retracted and the mechanism is locked in placed as it is shown in the image. To assemble the structure, tip of the main cantilever has to be slid back slightly more than 25% of the cantilever's original length and then released. During this process, stress is accumulated at the cantilever's anchor and the structural layer is most likely to fail.

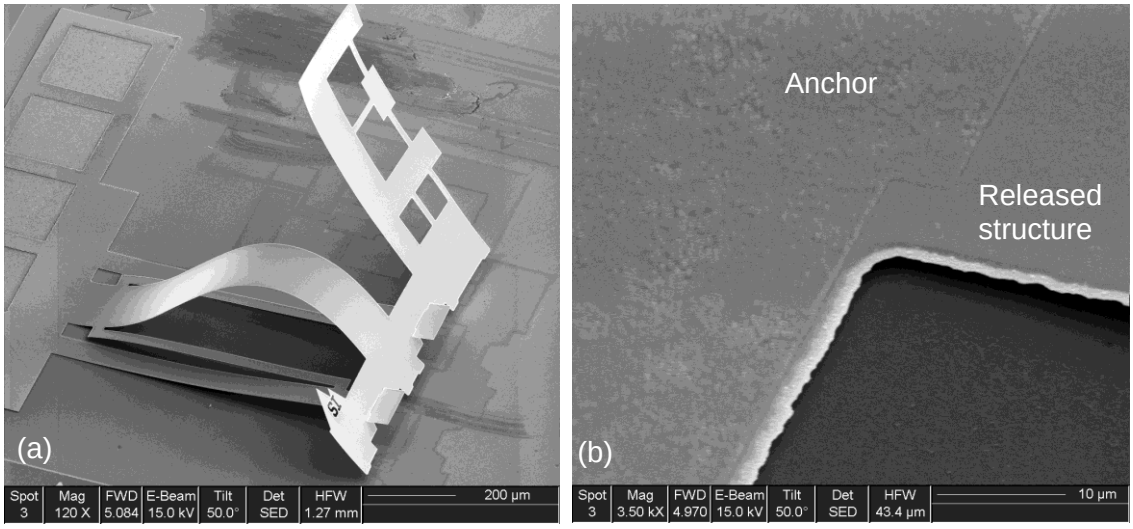


Figure 6: a) SEM image of a compliant mechanism fabricated by our process. The structure has been pushed out of plane and locked in place. b) Structure's anchor.

Figure 7 shows a SEM image of the structure cross section (before the release step). To expose the structure cross section we milled a trench into the substrate using

Focused Ion Beam (FIB). It can be observed that the anchor and the sacrificial layer have the same thickness, and that the structural layers are practically planar. The bottom silicide layer (etch stop) is also clearly visible in the image. We used a surface profiler to examine the structure topography. The measured height difference between the anchor and the original a-Si surface was about 10 nm on a 300 nm thick sacrificial layer (Figure 6.b). This step could be a result of processes variation during a-Si etching, or inconsistency in the nickel silicide composition.

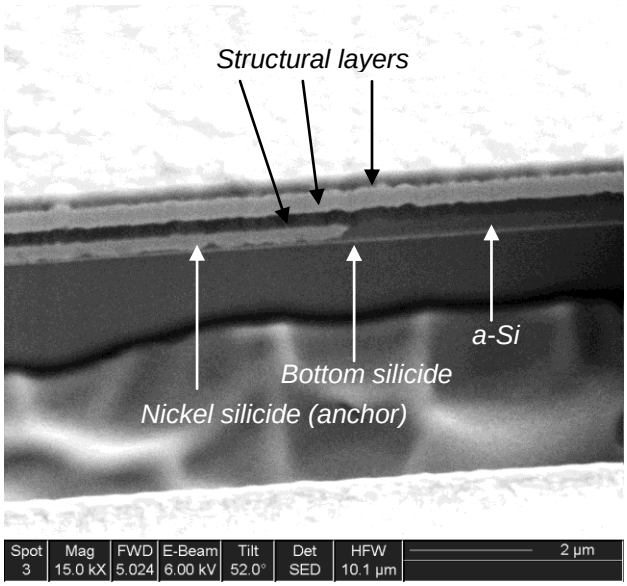


Figure 7: ***A milled trench into the substrate using FIB reveals the cross section of different layers. Notice that the anchor and sacrificial layer have the same thickness, and the structural layers are virtually planar. Please refer to the figure 5.h for the schematic of the structure.***

The a-Si thickness governs the final thickness of the anchors, because nickel completely consumes the amorphous silicon to form the silicide regions. If the etch depth of the a-Si by RIE is not equal to the desired calculated depth, the final surface of the silicide could be lower or higher compare to the original a-Si surface. The other reason for this discrepancy could be the actual composition of the silicide layer. Our process calculations are based on the formation of a perfectly mono-silicide film after annealing. If the annealed film partially contains the other phases of the silicide, the final silicide thickness and the amount that it grows above the initial a-Si surface will be different. However, the actual thickness of the silicide layer and its growth rate can be measured and used to compensate the processes variations.

To study how much our process has improved the mechanical robustness and the assembly yield of the fabricated compliant mechanism, we compared the assembly yield of two sets of identical structures (Figure 6.a), fabricated with and without the proposed planarization technique. The fabricated structures without using our process were made by conventional surface sacrificial micromachining as was explained earlier in this chapter. We released and assembled forty structures from each sets of the fabricated mechanisms. All forty structures that were fabricated by our planarization technique were successfully assembled and locked in place. The assembly success rate for the devices fabricated by the conventional technique was less than 20%, and most of the cantilevers failed and snapped at their anchor when they were pushed backed to be assembled. Figure 8 shows the images of a failed mechanism and the broken structural layer at its anchor. The structure failure happens right at the step that was resulted from the substrate topography.

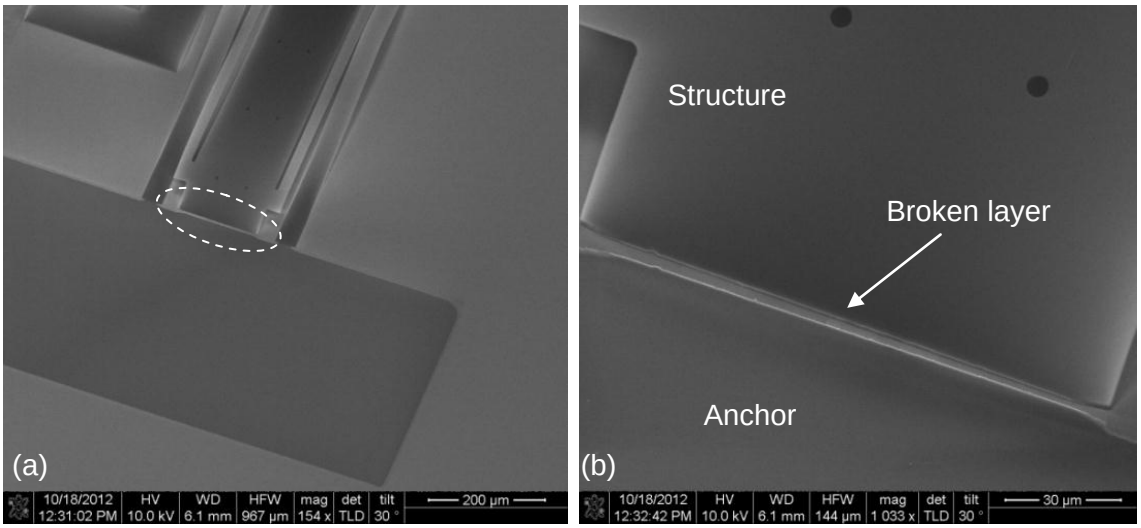


Figure 8: a) A failed structure at its anchor during the assembly process (structure anchor is marked with an oval). b) The close-up image of the structure's anchor (marked area in Figure 8.a)

We introduced an innovative sacrificial surface micromachining process that enhances the mechanical robustness of freestanding microstructures and compliant mechanisms. This process facilitates the fabrication, and improves the assembly yield of the out-of-plane micro sensors and actuators. Our process overcomes the topography issue related to the free-standing structures by eliminating the step between the structure and its anchor, and achieves planarization without using Chemical Mechanical

Polishing (CMP). The experimental results showed a significant improvement in the assembly yield of the compliant mechanisms that were fabricated by our proposed planarization technique.

3. Stress anisotropy

In freestanding structures, structural layer stress variation in different directions, or stress anisotropy, can severely distort the final shape of the released structure. Structural deformation can deteriorate the device performance (e.g. linearity, sensitivity, and dynamic range), or make the device assembly difficult or sometimes impossible. Therefore minimizing the stress anisotropy is a key issue in many applications that incorporate a free-standing or an out-of-plane structure. In many applications the released structure must remain flat and in-plane with the substrate; nevertheless, stress anisotropy or stress mismatch between different layers is a key element in the design of mechanisms such as self-assembly of out-of-plane structures, or 3D RF antennas [34].

Micromachining using polysilicon has a high thermal budget that limits its applications. Polysilicon is usually deposited at temperatures around 600ºC [35], and further annealing for controlling the stress, grain size or dopant activation requires even higher temperatures. Such thermal processes cannot be performed on all substrates, especially on ones with active devices. Because of the high thermal budget as well as other practical constraints [36], polysilicon based micromachining is not a post-CMOS compatible process and new materials have to be explored for low temperature micromachining on such substrates. On the other hand, thin metal films can be sputter-deposited at room temperature; they are attractive materials for micromachining and potential substitute for polysilicon. However, thin films prepared by physical vapour deposition are usually polycrystalline, and they often develop large residual stresses that can have a strong effect on film properties and functional performances [37]. These films experience large stress variations within the substrate plane (biaxial), and across their thickness. It is generally believed that columnar crystallite formation in the film's microstructure causes this anisotropy [37]. These films are not completely amorphous, and they are distinguished by their unique morphology and long-range atomic order in their structure. The microcrystalline structure and morphology of these films are a strong function of the sputtering parameters and geometry.

To successfully fabricate an out-of-plane sensor plate, to make a thermal accelerometer for instance, controlling the stress of the structural layer is as important as controlling the structural layer's stress anisotropy. The stress mismatch between the electrical layers that are deposited on top of the structural layer could significantly deform the sensor plate, if the structural layer stress is not controlled. By controlling the net (overall) stress level of the structural layer the mechanical effect of the electrical layers on the sensor plate could be minimized.

The overall stress level of the structural layer could be controlled by using a symmetrical tri-layer structure [38]. Two different materials with opposite intrinsic stress polarity (tensile and compressive) are used to form the structure. The structural layer is formed by sandwiching a layer of the first material between two symmetrical layers of the second material. The symmetry in the structure prevents the structural deformation due to stress mismatch, and the overall stress level of the layers is controlled by the thickness and the stress level of the each layer. The overall stress level of a tri-layer film is given by [38],

$$\sigma = \frac{2d_1\sigma_1 + d_2\sigma_2}{2d_1 + d_2} \tag{3-1}$$

where d_1, d_2, σ_1, and σ_2 are the thickness and intrinsic mechanical stress of the two outer and the sandwiched layers respectively.

Elemental metal and alloy thin films usually develop tensile intrinsic stress when they are sputter deposited, and their stress level is a function of the film material and the deposition parameters [37]. To fabricate a composite layer with controlled net stress level, these films can be encapsulated by two layers of a dielectric film, which usually have compressive intrinsic stress level. PECVD deposited dielectric films (silicon dioxide, silicon nitride) are completely amorphous materials with zero stress gradient across their thickness that makes them perfect choices for the fabrication of composite structures. Unfortunately, sputter deposited metal films have substantial stress gradient across their thickness that could cause major deformation in these composite structures. Figure 9 shows drastically deformed array of cantilevers fabricated out of sputter-deposited Nichrome after being released from substrate. The released cantilevers have

curled up severely due the non-uniform stress across the film thickness (perpendicular to substrate plane).

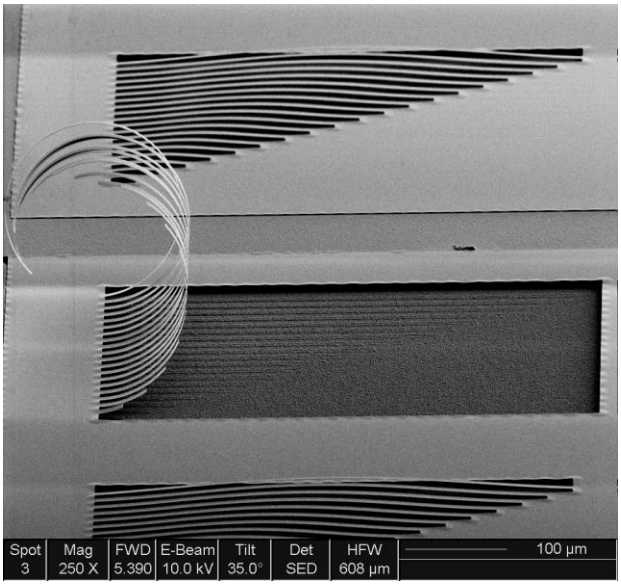


Figure 9: Effect of stress anisotropy across the thickness of a sputter-deposited Nichrome film.

To fabricate a flat out-of-plane sensor plate we use a composite structural layer consisting of two layers of PECVD silicon dioxide on top and bottom of a layer of a Nichrome film. We developed a novel technique to compensate for the stress anisotropy across the thickness of sputter-deposited metal films (Nichrome) which guarantees that the tri-layer structure remains flat when it is released from the substrate. The technique that we introduce in this chapter balances the stress variation across the thickness of the sputtered metal films by controlling the charged particles that bombard the film during the deposition process. By controlling the flux and energy of the bombarding ions during the film growth, stress level and stress polarity of the film can be modified. Ion flux and energy can be easily controlled by changing the substrate bias voltage. In a film with a net tensile stress, the forced exerted by the stress gradient across the film thickness can be compensated by changing the stress level of a very thin layer of the film to compressive. The moment caused by this stress mismatch prevents the freestanding structures from bending upwards due to the stress anisotropy.

3.1. Related compensation techniques

Magnetron-sputtered metal films that are deposited with dynamic deposition geometry (i.e., a moving substrate) were shown to develop in-plane crystallographic textures, elongated grain structures, and anisotropic residual stresses [37]. In order to obtain a homogenous thickness distribution, it is very common that the substrate is moved with respect to the sputtering source during deposition. During film deposition, the crystallites have the tendency to grow in the direction of in incoming atoms (atom flux) [39]. The periodic motion of the substrate leads to a periodical change of the deposition angle and growth direction of the crystallites. In this case, the anisotropic growth of the crystallites leads also to anisotropic film properties (e.g. magnetic properties), and in particular anisotropic intrinsic stress. However, films deposited in a static geometry generally develop isotropic in-plane residual stress (bi-axially balanced). Regardless of the deposition geometry, these films experience a large stress gradient across their thickness.

Many techniques have been developed to overcome the stress anisotropy of the sputtered metal films. Some of these methods were able to only reduce the film in-plane stress gradient, without eliminating the gradient across the film thickness. The inhomogeneous nature of the deposited film's microcrystalline structure is believed to be the main cause of this anisotropy. H. Kattelus *et al.* [36] tried to remove the long-range atomic order in the deposited films and to improve the film's microcrystalline uniformity by reactive sputtering. They have tried to deposit a completely amorphous film by introducing nitrogen in the film composition through reactive sputtering. They were highly successful with eliminating the lateral stress variation in the film, but the vertical gradient remained unchanged.

F. Hubenthal *et al.* [39] managed to control the in-plane stress anisotropy of a sputter deposited TiN film by controlling the period of a linearly moving substrate (with respect to the sputtering source). They characterized the film structure by the undulation period, $\lambda = {}^{t}/_{n}$, where t is the total thickness of the film and n is the number of the cycles. They noticed a distinct microstructure with a preferential growth direction, combined with high in-plane stress anisotropy for large undulation periods, whereas an almost isotropic structure with a poor crystalline order and almost isotropic biaxial

stresses for small undulation periods. Nevertheless, they observed strong stress anisotropy across the film thickness regardless of the undulation period.

W. Wu *et al.* [40] studied the effect of the deposition pressure and post-sputter annealing on the bi-axial stress. They examined the stress anisotropy of the films deposited below and above the transition pressure of their material of interest (molybdenum). The transition pressure [41] for a given material is a pressure above which the sputtered film develops tensile stress, which is a function of the target material and sputtering gas atomic masses. Their experimental results revealed that the stress gradient is higher when the deposition pressure is above the transition pressure (when film develops tensile intrinsic stress). In contrary, the effect of post-sputter annealing on the stress gradient is more profound when the film has tensile stress. The biaxial stress anisotropy of the film was minimized by controlling the deposition pressure and the post-annealing period and temperature

R. Cuthrell *et al.* [42] managed to deposit an almost stress free film by developing a pressure cycling technique. They deposited alternate layer of films with tensile and compressive stresses by switching the deposition pressure above and below the transition pressure. Despite their success in controlling the film stress and preventing the film from cracking or blistering, they could not control the vertical stress gradient build-up.

Saturating the stress level of a film is another technique that introduced by another group to control the stress anisotropy [43]. In this method, stress saturation is achieved by controlling the deposition parameters (i.e., temperature, pressure, and substrate bias). Stress saturation causes the film to become essentially isotropic (uniform) because further applied stress pushes the material beyond its yield point, relaxing the material that relieves the additional stress and causes the internal stress to remain at the saturated level.

Although the in-plane stress of the film can be significantly controlled by the aforementioned methods, the stress gradient across the film thickness remains almost the same regardless of the compensation method. Our technique compensates for the stress anisotropy across the film thickness by controlling the positive ion flux and energy

that bombard the growing film. We alter the substrate bias voltage during sputtering to control the intrinsic residual stress of the film and to balance the film's vertical stress gradient.

3.2. Background

Thin film properties, such as intrinsic stress, refractive index, surface roughness, and electrical resistivity, can be modified by controlling the film's microstructure [44]. The film's microstructure is determined primarily by the surface and near-surface conditions during film growth; more specifically, by the adatom (adsorbed atom) mobility. An adatom is an atom that lies on a crystal surface, and it can be thought of as the opposite of a surface vacancy [45]. This term is used in surface chemistry, when describing single atoms lying on surfaces and surface roughness. The word is a contraction of "adsorbed atom" [45].The main parameters for controlling the adatom mobility are substrate temperature and particle bombardment.

The microstructure of sputtered films is usually classified into four zones: 1,2,3, and T, or Transition. Zone 1 structure, consists of tapered columns and significant voids between columns, which is a common formation when the growth temperature, T (in degree Kelvin), is much lower than the melting point, T_m, of the deposited material (i.e., T/T_m ratio is less than 0.3). In this range of growth temperatures, adatom diffusion is negligible, and because of the shadowing effect, most of the sputtered flux is deposited on high points of the film with little material reaching the valleys. The under-dense Zone 1 structure causes tensile stress, lower reflectance, higher resistivity, and more impurity contamination. Zone 2 and zone 3 are usually formed when the T/T_m ratio is greater than 0.3 and close to the melting point of the material. The details about these zones and their applications are found in [44].

The fourth zone, Zone T (Transition), is the result of bombardment induced surface mobility. Films that would have been expected to have a Zone 1 structure based on the T/T_m ratio can be grown with a very smooth surface and high density by bombarding the growing film with energetic particles during film growth. In the case of magnetron sources, the main bombarding species are ions and energetic neutrals. The

surface mobility and, consequently, Zone T structures, can be promoted by controlling the positive ion bombardment. The ion bombardment flux and energy can be controlled by applying a negative bias voltage to the substrate, which is inevitably the easiest parameter to control in a sputtering system. Alternatively, bombardment can be accomplished with the use of an ion source. Nevertheless, bombardment effects can also be influenced by the pressure, angle of incidence, magnetic field configuration, discharge current, and working gas species [46].

Ion bombardment of the growing film usually causes transition from Zone 1 to Zone T, and is associated with a change in the film's intrinsic stress from tensile to compressive. Both the energy and the ion per atom arrival rate are important factors determining the effects of bombardment. This transition is attributed to rearrangement of the condensing layers (adsorbing) due to recoil implantation (forward sputtering) [47].

In planar magnetron sputtering system if a negative DC bias is applied to the substrate, ions can be extracted from the plasma and relatively large ion current can be produced [46]. For a given substrate bias, increasing the pressure reduces the ion current, and the maximum current usually occurs at pressures around 1 mTorr. At a constant pressure, by increasing the substrate bias the substrate current initially increases but at higher voltages it saturates and becomes independent of the bias potential. One can conclude that at a given pressure, the energy of the bombarding ions could therefore be adjusted without significantly altering the total ion current, or the ratio of ions to sputtered atoms at the substrate. Figure 10 shows how the substrate current changes versus substrate potential at 1 mTorr in our sputtering chamber. In our system, the cathode-substrate separation is 4 inches and the substrate holder area is about 5 square inches.

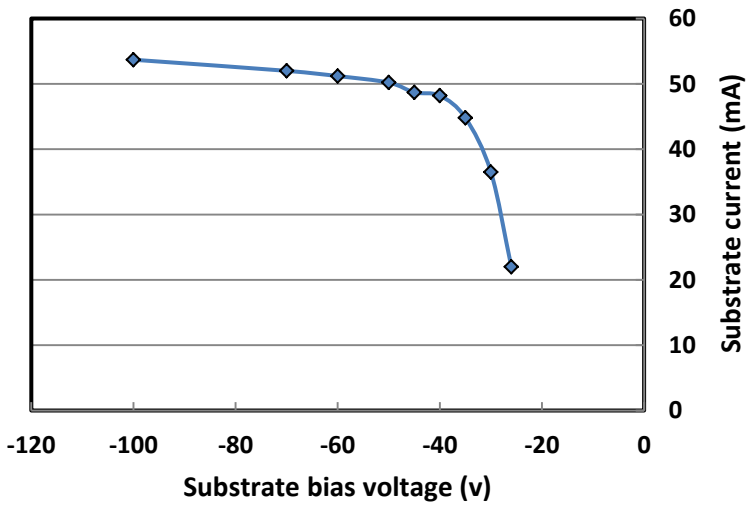


Figure 10: Substrate current versus substrate potential.

Although the bombarding ions energy could be adjusted to control the film properties (e.g., resistivity, reflectivity, stress), increasing the ion energy has another effect on the substrate and the growing film that has to be monitored. Basically, with high enough ion energy, substrate can indeed be treated as sputtering target and considerable re-sputtering of the depositing film can occur. The re-sputtering could become significant at voltages comparable to the cathode voltage and the deposition rate can drastically decrease. In this regime, deposited films develop very high compressive stress along with extremely large stress gradient across their thickness. Figure 11 shows how the deposition rate drops in our sputtering systems due to re-sputtering of the growing film by energetic ions at high substrate potentials.

The intrinsic stress of magnetron sputtered thin films varies by thickness, and it has a tendency to reach a definite value as the film becomes thicker [48]. Although the film's intrinsic stress level and polarity can be tailored by adjusting the deposition parameters such as pressure, temperature, and substrate voltage, controlling the vertical stress gradient across the film thickness is very hard, if not completely impossible, to control. In general the elongated and tapered columnar microcrystalline structure of the deposited film is the source of this anisotropy [36], [48]. The bottom section of the film is more compressed than the top part because of the film morphology; therefore, a fabricated and released cantilever from these films will curl up regardless of whether the film's net stress is compressive or tensile [36].

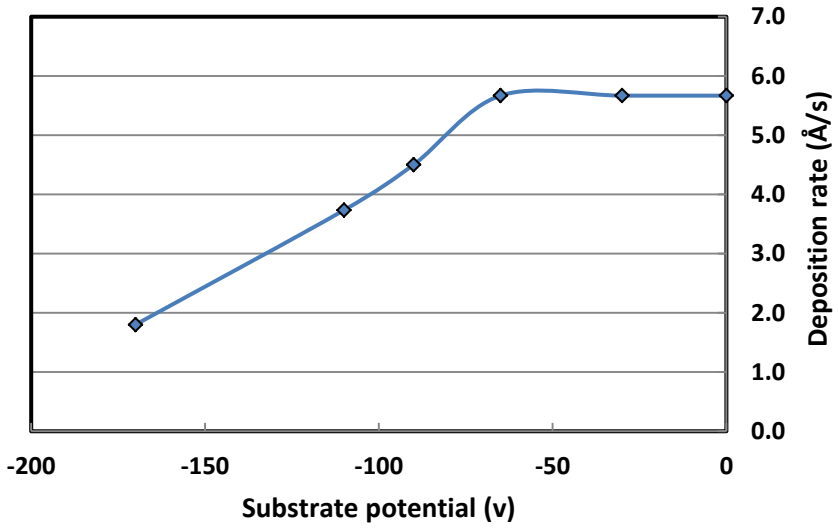


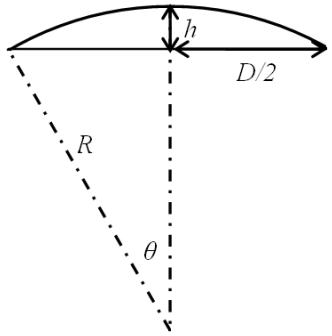
Figure 11: Drop in the deposition rate due to the re-sputtering at high bias voltages.

3.3. Compensation technique

The effect of the stress gradient across the thickness of a sputtered metal film can be compensated or balanced by embedding a layer in the film that has the opposite stress polarity compared to the bulk of the film. The force imposed by the stress mismatch between this layer and the bulk of the film could overcome the effect caused by the film's vertical stress gradient. This compensating force guarantees that the released freestanding structures remain flat. This layer is introduced to the growing film by altering the substrate bias voltage during the sputtering process. The substrate bias voltage controls the ion flux and energy that bombards the film and it enables tailoring the stress parameters of the film. The stress level and thickness of this balancing layer can be determined experimentally. The necessary thickness and stress level of this layer is governed by the bulk of the film's thickness, the overall stress level, and the magnitude of the vertical stress gradient.

For most refractory metals, at zero substrate bias voltage and at a fixed thickness, the net intrinsic stress is usually tensile. By increasing the bias voltage (a negative value), the tensile stress tends to increase, and it reaches a maximum. By further increasing the voltage, the tensile stress decreases and then becomes

compressive; the compressive stress usually saturates at higher voltages. To embed the balancing layer into the film, the bias voltage at which the film stress changes from tensile to compressive (the transition voltage) has to be measured experimentally. This voltage is a function of the deposition parameters, especially the deposition temperature, pressure, and the target material. To measure the transition voltage, we deposited several films with the same thickness on 4 inch silicon wafers, gradually increased the magnitude of the negative bias voltage, and measured the film stress after each deposition. To measure the deposited film stress, we used the "Ionic Systems" stress gauge to measure the change in the curvature of the wafer after each deposition. Our stress gauge has a 9.5 centimetres circular knife edge, and it optically measures how much the center of a wafer bows in or out after the film deposition. For a small angle θ, the deflection of the center of the wafer is related to the wafer's radius of curvature by:



$$R \cong \frac{(\frac{D}{2})^2}{2h} \qquad (3\text{-}2)$$

With known radius of curvature, the film stress was calculated using the Stoney's equation [49]. The Stoney's equation calculates the average stress of the deposited film on a substrate without having the elastic parameters of the film. The Stoney's equation assumes that the film thickness is negligible compare to the substrate thickness, and it is defined as:

$$\sigma = \frac{E_s d_s^2}{6(1-\vartheta)} \cdot \frac{1}{d_f} \cdot \frac{1}{R} \qquad (3\text{-}3)$$

In which σ is the film stress, E_s is the biaxial modulus, d_s is the substrate thickness, ϑ is the Poisson's ratio, d_f is the film thickness and R is the wafer's radius of curvature.

The measured intrinsic stress variation in a 300 nm thick Nichrome film as a function of the substrate bias voltage is summarized in the Figure 12. We DC-sputtered

the Nichrome films from a 3-inch target at 150 watts power rating in argon atmosphere for 10 minutes. The chamber pressure was kept constant at 1 mTorr during the sputtering process. The substrate was not heated, but its temperature usually raised a few tens of degrees during the deposition process.

The experiments showed that the tensile stress of the sputtered Nichrome film maximizes at around -25 volts. The film tensile stress reduces as the bias voltage increases and it becomes slightly compressive at -40 volts; therefore, the transition voltage lies between these two values. Hence, in order to compensate for the stress gradient of a film deposited at room temperature with zero bias voltage, the bias voltage could be switched to values close -40 volts (the transition voltage) during the film deposition. The measured transition voltage in this experiment is only an average value for the deposited NiCr film with fix thickness (300 nm) and can vary if the film's total thickness changes. Similar to the intrinsic stress of magnetron sputtered thin films which tends to vary by thickness, the transition voltage for different portion of the film and across its thickness can vary as well. The transition voltage for the compensating layer in our process could be different and has to be measured for the given thickness. Our experiments have shown that this value is slightly higher for our thin compensating layer (top portion of 300 nm thick NiCr film).

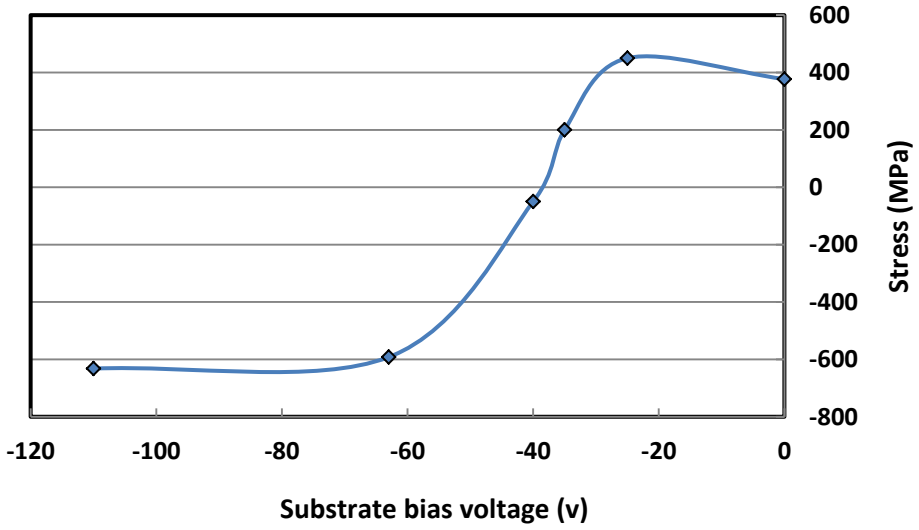


Figure 12: Variation in the average stress of a 300 nm thick Nichrome film with respect to the substrate potential.

3.4. Compensation process and results

We used a (100) n-type silicon wafer as a substrate and NiCr (Nichrome: 80% Nickel and 20% Chromium) for our experiments. Our early experiments with Nichrome had shown that it forms a very thin layer of silicide even when it is sputtered directly onto the silicon wafer at room temperature. Sputtering on a heated or biased substrate further enhances the silicide formation. We avoided silicide formation, which could have altered our experimental results, by depositing a very thin layer of PEVCD oxide (40 nm) on the silicon substrate. The oxide acts as a diffusion barrier and stops the silicide formation. However, the oxide layer prevents the directed DC biasing of the film through the substrate; therefore, we needed to use an RF source to bias the growing film. Our sputtering chamber was not equipped with an RF source; therefore, we had to use a metal grid on the oxide layer to bias the film.

Using an RF power source is the easiest way to bias the substrate when sputtering a non-conducting film or a conducting film on a non-conductive substrate. An alternative way is to use a DC power supply and a metal grid on the substrate to establish electrical contact to the film; in our case, a conducting film on a non-conducting substrate. In the last scenario, because of the directional nature of the sputtering process and the shadowing effect, establishing electrical contact to a growing film simply through the substrate holder is impossible. Fortunately, sputter-deposited metal films start to conduct when their thickness passes a few nanometres. Therefore, by introducing a pre-deposited and patterned metal grid on the substrate, it is possible to apply the bias voltage to a growing film and have a uniform ion flux across the substrate. The electrical contact is accomplished through the metal grid and the substrate holder, and the film will be biased when it is only a few nanometres thick. The metal grid runs around the perimeter of each individual die, and it does not interfere with the chip design.

The metal grid was made out of a 300 nm thick aluminum film. The aluminum was DC-sputtered and patterned by wet etching (Transene type A Aluminium etchant) to form the grid around each die boundary. The maximum resistance of the grid (the farthest point to the substrate holder) was about a few ohms. The Nichrome was DC-sputtered from a 3-inch target in a UHV sputtering system with a stationary substrate

holder at 1 mTorr in argon atmosphere. The deposition time was ten minutes at 150 watts power rating. To study the stress gradient and polarity, the Nichrome film was patterned using standard photolithography and wet etching (Transene 1020AC Chromium etchant) to form arrays of cantilevers and beams with different lengths. After patterning the Nichrome film, the formed structures were released from the substrate by etching away the oxide film with hydrofluoric acid vapour at 40°C (Idonus VPE). We used Xenon Difluoride (XeF_2) to etch a cavity a few micrometers deep in the substrate and under the arrays to make sure that cantilevers and beams were not over compensated (bending downward), which could make them to touch the substrate. The gas phase etching prevents the structures from sticking to the substrate; therefore practice of the Critical Point Drying (CPD) process is not necessary.

Figure 13 shows an array of released cantilevers fabricated out of a 300 nm thick Nichrome film that was deposited at room temperature with zero bias voltage. The image clearly reveals the effect of the stress anisotropy across the film thickness. The cantilevers are curled up as a result of the bending moment produced by the stress gradient. No noticeable bi-axial stress gradient can be observed from the test results, because the film was sputtered on a stationary substrate holder.

To measure the exact value of the transition voltage for the compensating layer, the thickness of this layer has to be predetermined but at the same time kept as thin as possible to reduce the process sensitivity. Therefore, we decided to limit this layer's thickness to only 10% of the film's total thickness. With the given thickness and in order to measure the transition voltage for this layer, several films with constant total thicknesses were deposited. Each film was deposited in two cycles during which a different bias voltage was applied to the film. The first 9 minutes of the deposition was carried out with zero substrate bias voltage, but during the last minute we applied voltage to the growing film. The effect of this layer on the film stress gradient was investigated by measuring the radius of curvature of the released cantilevers. The change in the curvature of the released cantilevers with respect to the different bias voltages is shown in Figure 14.

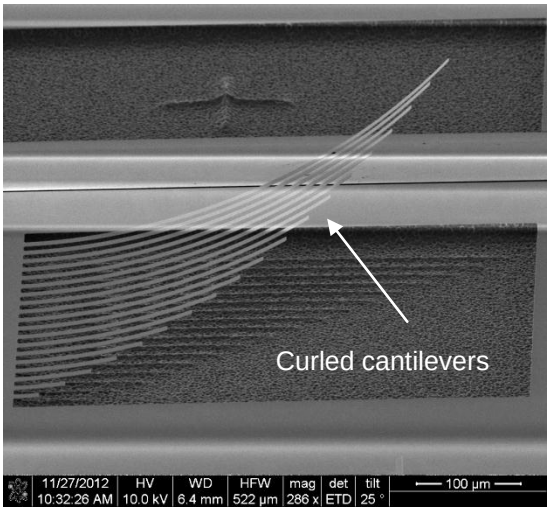


Figure 13: **Array of 300 nm thick Nichrome cantilevers deposited at room temperature with zero bias voltage.**

As we speculated, the transition voltage has slightly changed and shifted to values between -40 to -50 volts (the curvature graphs crosses zero at values between -40 to -50 volts). To compensate for the effect of the stress anisotropy across the film thickness (300 nm in total), the compensating layer has to be deposited at voltages around -50 volts. To study the effect of the deposition temperature on the transition voltage, we repeated the same experiment at elevated temperatures. We noticed that the stress versus substrate bias voltage curve tends to shift upwards at higher substrate temperatures. This shift means that elevated temperatures result in a higher tensile stress (at zero bias voltage) and a higher transition voltage. For instance, the measured transition voltage for the film deposited at 150°C was about -110 volts, which is significantly higher than that of the film deposited and room temperature.

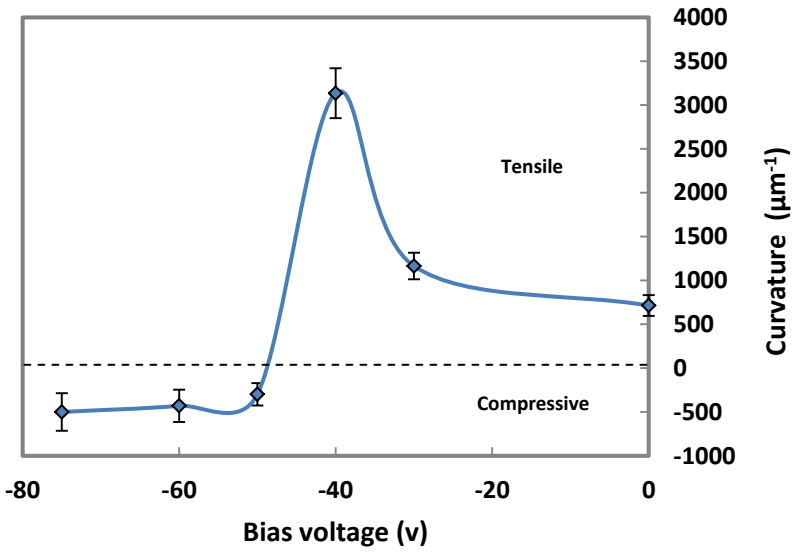


Figure 14: Curvature of released cantilevers at different bias voltages with a fixed compensating layer thickness. The transition voltage for the compensating layer lies between -40 to -50 volts.

The radius of curvature of a cantilever was calculated based on measuring the coordinates of three separate points on the cantilever. The perpendicular bisectors of the two chords that are formed by these three points intersect each other at the center of the curvature. Figure 15 represents the geometry for the measurement technique. The radius of curvature is calculated as follow:

The first perpendicular bisector is defined by its slope, m_1, and the coordinates of the midpoint of the first chord, (x_{m1}, y_{m1}). The slope of the bisector and its intersection coordinates with the first chord are calculated as follow;

$$m_1 = \frac{(x_1 - x_2)}{y_2 - y_1};\ \ x_{m1} = \frac{x_1 + x_2}{2};\ \ y_{m1} = \frac{y_1 + y_2}{2}$$

For the second perpendicular bisector we have;

$$m2 = \frac{(x_1 - x_3)}{y_3 - y_1};\ \ x_{m2} = \frac{x_1 + x_3}{2};\ \ y_{m2} = \frac{y_1 + y_3}{2}$$

The coordinates of the center of curvature, (x_o, y_o), where two perpendicular bisectors intersect can be calculated as;

$$x_o = \frac{y_{m2} - y_{m1} - m_2 * x_{m2} + m_1 * x_{m1}}{m_1 - m_2} \; ; \; yo = m_1 * (x_o - x_{m1}) + y_{m1}$$

The radius of curvature can be calculated from the above parameters as follow;

$$R = \sqrt{(x_1 - x_o)^2 + (y_1 - y_o)^2}$$

We used optical microscope and eyepiece micrometer to optically measure the coordinates of the three points. We used an objective lens with x80 magnification to measure the height of the desire points on the cantilever which limits the depth of field of the image to 0.3 μm. With this small depth of field, and with experienced pair of eyes, ±1 μm resolution in height measurement is achievable. The achievable horizontal resolution at the maximum magnification of our microscope (x800) and with the eyepiece micrometer was about ±1 μm as well.

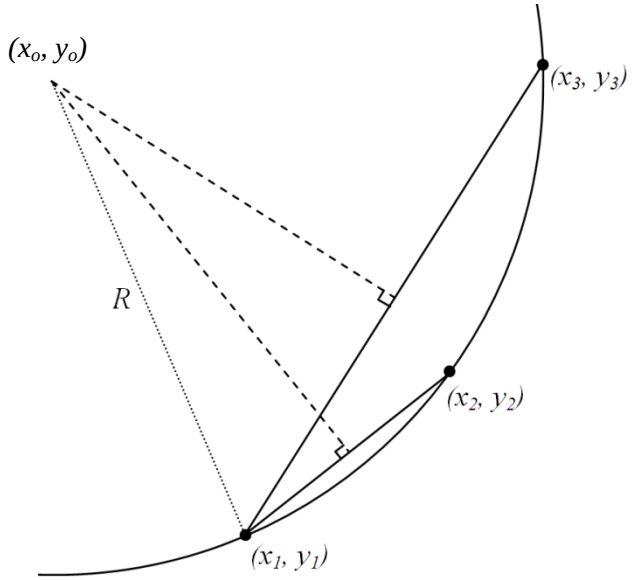


Figure 15: The center of curvature is where the centerlines of the two chords intersect.

To determine the exact thickness that is necessary to fully compensate the stress gradient effect in the NiCr film, we kept the bias voltage constant at -50 volts and varied the compensating layer deposition period. During these experiments, the first cycle of the film deposition, with zero bias voltage, was 9 minutes and was kept constant. The effect of the period of the second deposition cycle (at fixed bias voltage) on cantilever's curvature is illustrated in Figure 16. The cantilever curvature has almost a linear relation

to the thickness of the compensating layer and the necessary thickness to fully compensation the stress gradient can easily be extracted from the curve.

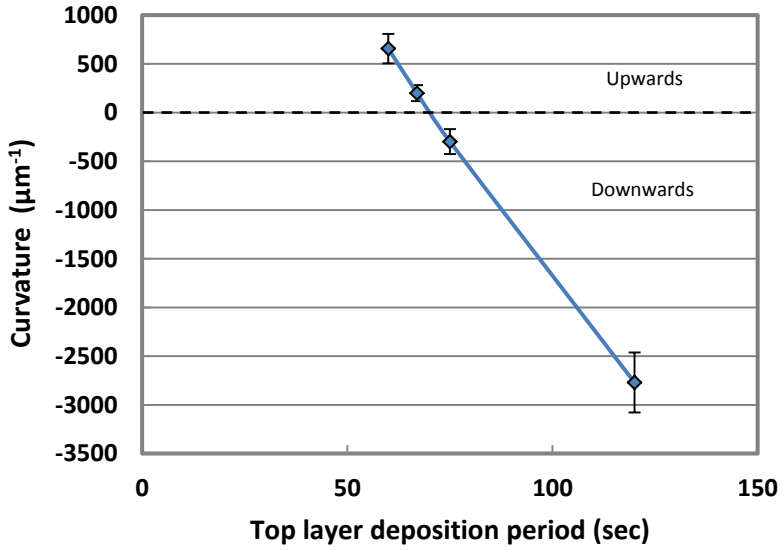


Figure 16: Change in the cantilever curvature with variable compensating layer thickness. The desired deposition time can be extracted from the graph at its zero crossing.

When a thin film is deposited on a beam, the stress mismatch between the film and the beam will cause the beam to bend. If we assume that the film thickness is negligible compare to the beam thickness, the radius of curvature of the beam can be calculated, and is defined as [50]:

$$\rho = \frac{EI}{M} \qquad (3\text{-}4)$$

where

$$EI = \frac{1}{12} W H^2 (E_1 H + 3E_0 h)$$

$$M = \frac{1}{2} \sigma_{0,relaxed} H h$$

$$\sigma_{0,relaxed} = \frac{(E_1 \sigma_0 + E_0 \sigma_1) H}{E_0 h + E_1 H}$$

W, H, E_1, and σ_1 are the beam's width, thickness, biaxial modulus, and intrinsic stress respectively, and h and E_0 are the film's thickness and biaxial modulus, and σ_0 is the film intrinsic stress. In the specific case of an embedded layer within a film from the

same material, we can assume that the biaxial modulus of the bulk of the film and the embedded layer are the same. With this assumption, the “curvature of the beam” versus “*h/H*” curve, for small values of *h/H*, is almost a straight line which is in agreement with the experimental results. Figure 17 shows the calculated change in the curvature of a beam with respect to the thickness ratio of the compensating layer, *h,* and uncompensated portion of the film, H (constant value).

The released cantilevers shown in Figure 18, were fabricated from a 300 nm-thick Nichrome film deposited with a variable substrate bias voltage. During sputtering, we kept the bias voltage zero for the first nine minutes of the deposition and changed it to -50 volts for the last 70 seconds. The top portion of the film develops compressive stress due to negative bias voltage, and it is only 30 nm thick. The effect of the ion bombardment on the film stress parameters and the force applied by the top compressive portion of the film is obvious from the image. The stress mismatch between the very thin top portion and the bulk of the film has compensated the effect of the film stress gradient. As a result, the released cantilevers are practically flat.

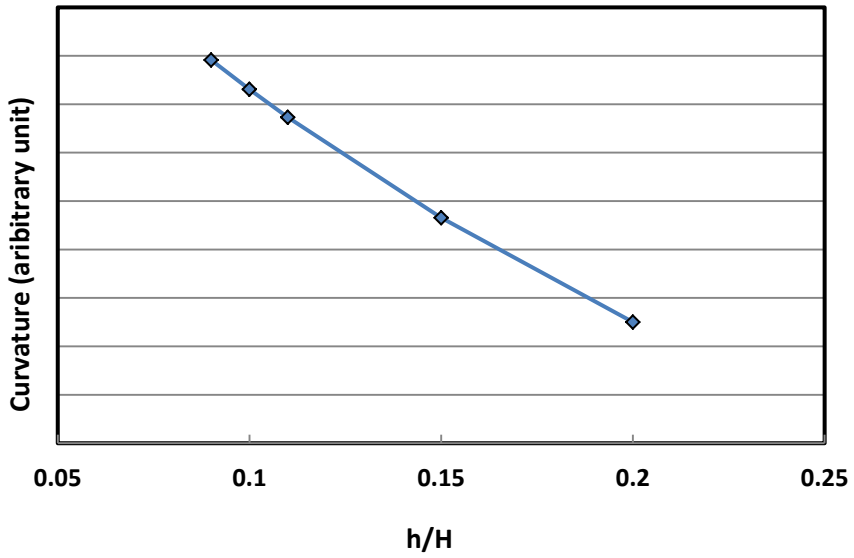


Figure 17: Estimated variation in curvature of a bimorph film with respect to the h/H ratio.

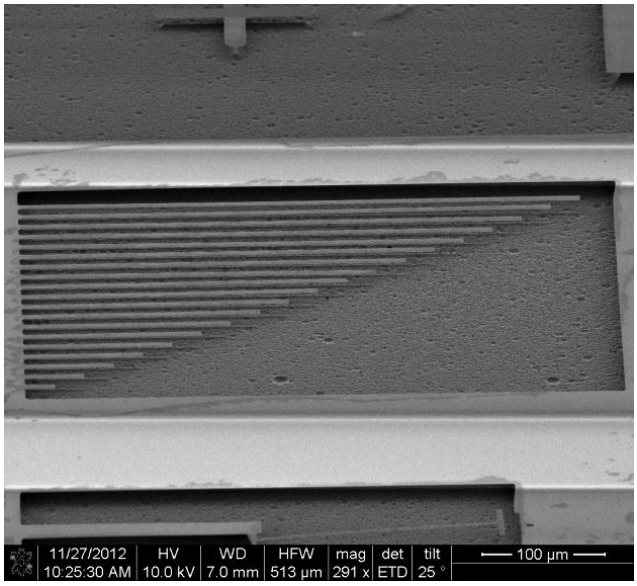


Figure 18: **Array of cantilevers deposited at room temperature with a variable bias voltage.**

We studied the effect of the substrate bias and the subsequent energetic ion bombardment on the film morphology and micro-crystalline structure by analyzing the film with x-ray diffraction (XRD) and by observing the film microstructure with nano-SEM imaging. To expose and image the cross section of the films we cleaved the prepared samples by hand along the (110) plane of the silicon substrate. We used FEI Nova NanoSEM 430 to image the samples cross section. Figure 19 shows the SEM images of the cross section of two Nichrome films that were deposited with and without variable substrate bias voltage. The film in Figure 19.a was deposited at room temperature for 15 minutes with zero bias voltage. The film in Figure 19.b was deposited in two cycles: 12 minutes with zero bias voltage and 3 minutes biased at -50 volts. Decrease in the surface roughness and therefore the film's smaller grain size that resulted from the ion bombardment of the film can be observed from the images. Although the film in Figure 19.b was deposited in two cycles with different bias voltages and despite the extreme magnification of the image, the boundary of the film's two regions cannot be distinguished.

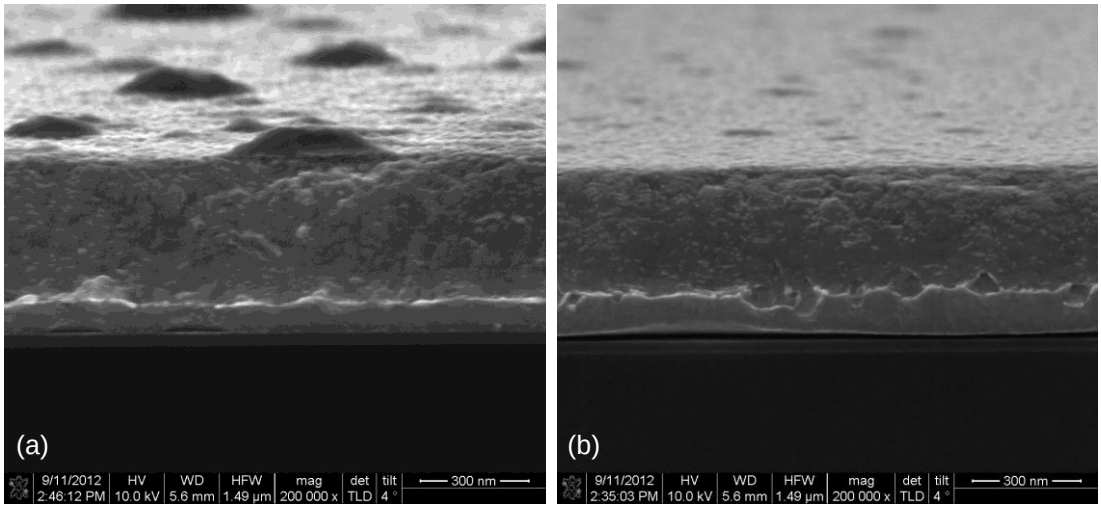


Figure 19: Cross section of the deposited films (a) without and (b) with variable bias voltage.

Decrease in the surface roughness due to the smaller grain size and less crystalline order seems to be confirmed by Figure 20 which shows the XRD diffraction pattern of the deposited films. We used the "Rigaku Rapid Axis" X-ray diffraction machine with curved imaging plate detector for the XRD analysis (X-ray source: Cu K_{α}, λ=1.54 Å). Considering the crystallite size in terms of the Full Width at Half Maximum (FWHM) of the peaks, we could observe diffraction-peak attenuation and broadening for (220) planes when film was sputtered with bias voltage. For low intrinsic stress levels, this broadening can be mainly correlated to the decrease in the grain size and crystallites' order [48]. However, peak broadening could be due the lattice strain (micro-strain) as well, which makes the XRD results hard to interpret.

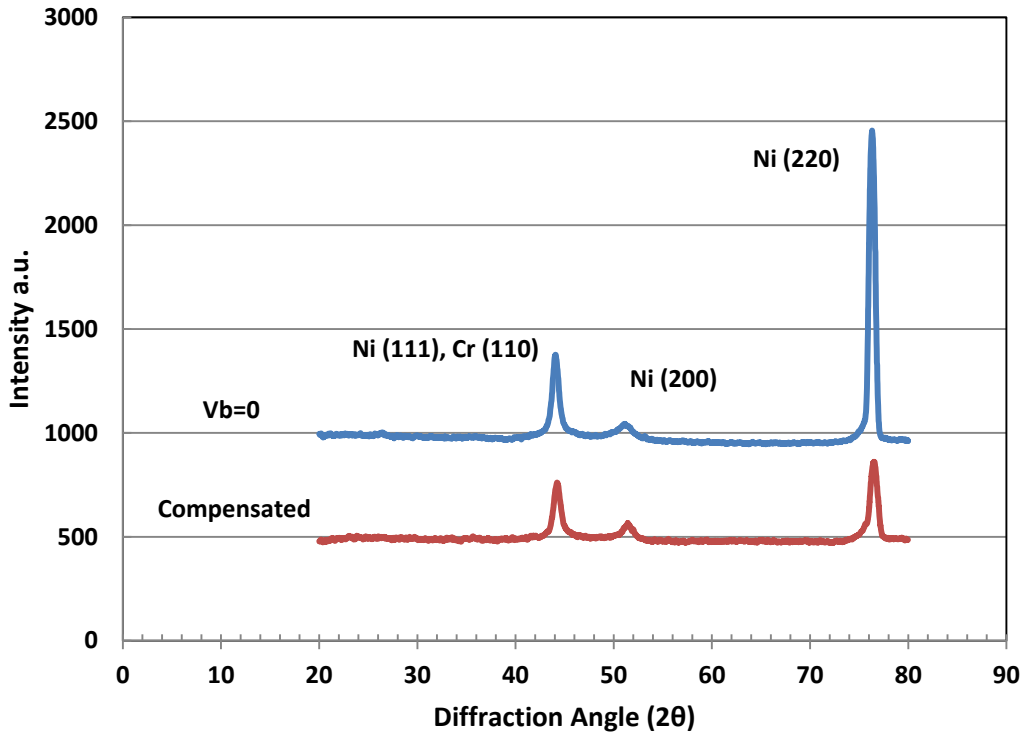


Figure 20: X-ray diffraction pattern of Nichrome films deposited with and without bias voltage. Note that curves have a vertical offset for clarity.

English physicists Sir W.H. Bragg and his son Sir W.L. Bragg developed a relationship in 1913 to explain why the cleaved faces of crystals appear to reflect X-ray beams at certain angles of incidence (theta, θ). In materials with a crystalline structure, X-rays scattered by ordered features (atom rows and plates) in certain directions can meet the criteria for constructive interference which results in the amplification of the scattered radiation. The conditions for the constructive interference are determined by Braggs' law which is illustrated in Figure 21.

$$n\lambda = 2d\,sin\,\theta$$

λ = X-ray wavelength

d = distance between lattice planes

θ = angle of incident with respect to the lattice plane

n = integer

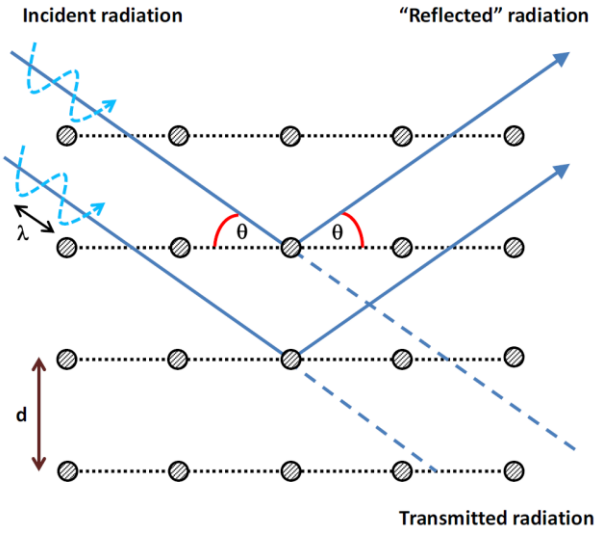


Figure 21: Braggs' law for constructive interference of reflected (scattered) x-ray from atoms of a crystal. Source, http://cc.usst.edu.cn/Download /26da9cdf-6134-41fc-bf56-6dcccd9edd20.pdf, retrieved May 12, 2013.

By careful analysis of the X-ray diffraction data, different properties and characteristics of a material can be studied, including:

- Average spacing between layers or rows of atoms.
- Orientation of a crystal or grains.
- Crystal structure of an unknown material.
- Size, shape, and internal stress of a small crystalline region.

The effect of ion bombardment on the film stress anisotropy could be quite deteriorating if the bias voltage is kept constant. We noticed that, regardless of the film's overall stress polarity, increasing the substrate bias voltage (the absolute value) increases the film's stress gradient. We aforementioned that the tensile stress level of a sputtered metal film can be increased by applying a bias voltage less than the transition voltage, or the film stress level can be changed to compressive if the bias voltage passes that critical value. In either case, the effect of stress anisotropy is more profound, and the released cantilevers radius of curvature decreases significantly.

An array of cantilevers fabricated out of a Nichrome film deposited with a constant bias voltage at -110 volts is shown in Figure 22a. This figure reveals that the stress gradient has become more significant due to the constant bias voltage. The other

important film characteristic is that the net stress of the film has changed from tensile to compressive. The film's compressive stress can be noticed by the buckled clamped-clamped beams (Figure 22b) and/or by the ripples at the edge of the released film. In contrary, as shown in Figure 22c, a deposited film with zero bias voltage develops tensile stress which results in a flat array of beams.

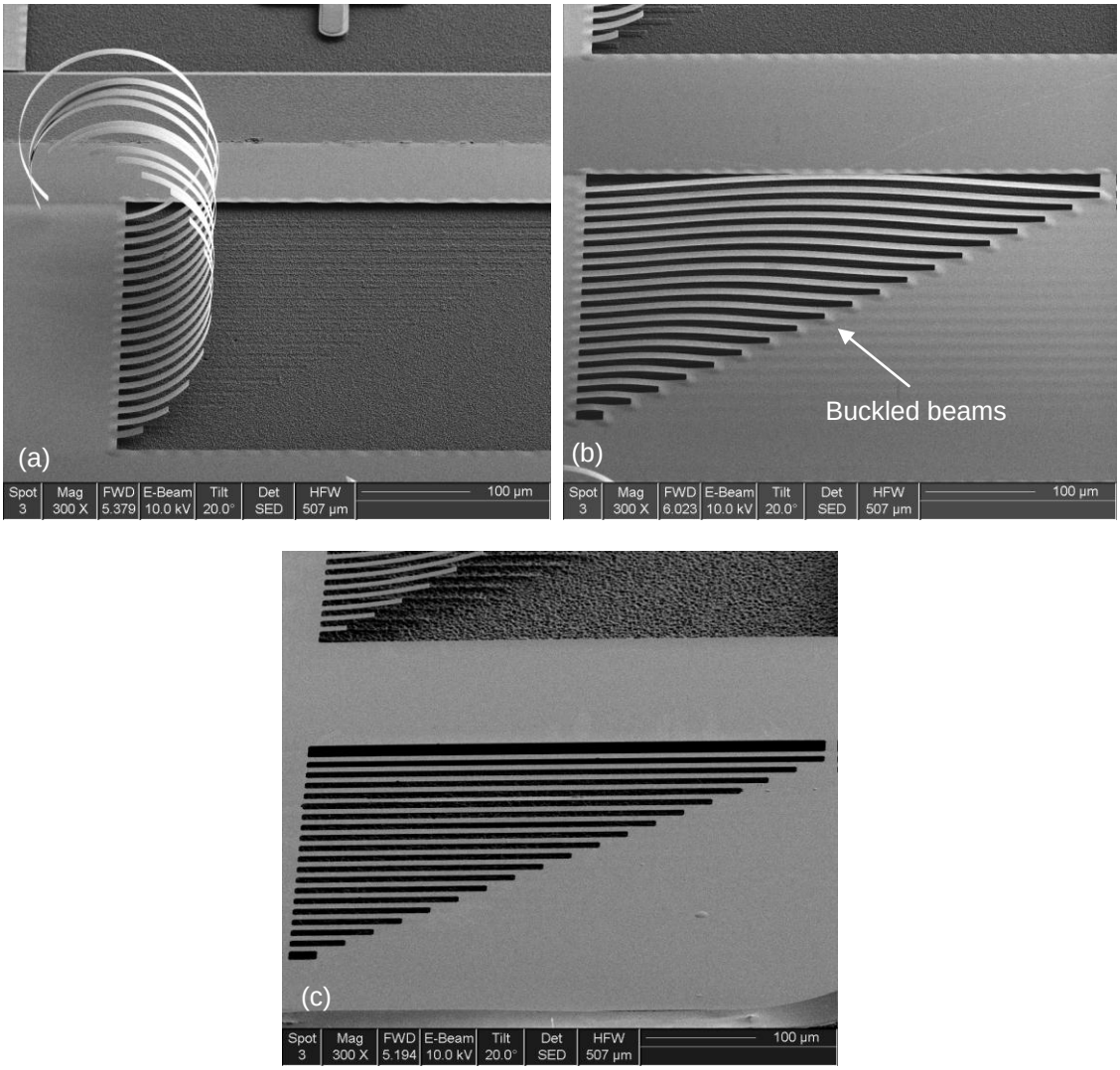


Figure 22: **The deposited and released structures at room temperature with constant bias voltage at -110 volts. (a) An array of cantilevers. (b) An array of clamped-clamped beams. (c) An array of beams deposited at zero bias voltage.**

The substrate temperature has a similar effect on the stress gradient as a constant bias voltage. The elevated substrate temperature increases the stress anisotropy across the film thickness without changing the stress polarity. Figure 23 shows images of two cantilever arrays that were deposited at 150ºC and at room temperature. Clearly, the decrease in the radius of curvature of the cantilevers is an indication of a larger stress gradient at higher deposition temperatures.

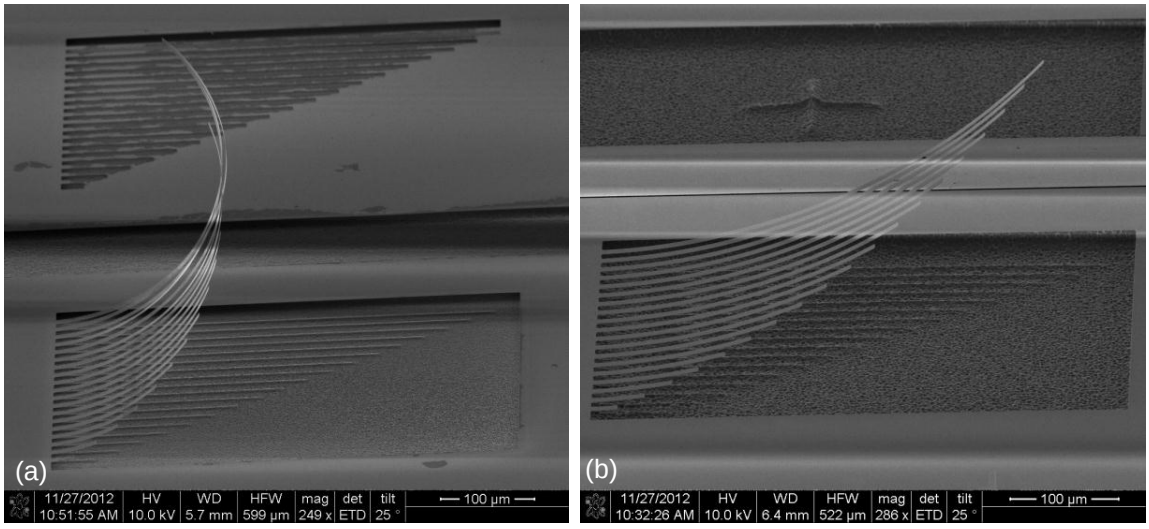


Figure 23: **The effect of deposition temperature on the vertical stress gradient. (a) An array of cantilevers deposited at 150ºC. (b) The same cantilevers deposited at room temperature.**

The film formed by variable bias sputtering might resemble a bimorph structure. However, the thermal behaviour of the deposited film is significantly different from that of a bimorph film. By carefully forming a bimorph structure, the effect of the stress anisotropy can be compensated, but the thermal mismatch between these two layers can significantly distort the freestanding structure if the ambient or the structure temperature changes. The elevation in structure's temperature can happen in many cases, such as thermal actuators or thermal inertia sensors [3]. With our technique, the thermal properties of the embedded layer are practically the same as the bulk of the film; therefore, second order effects such as thermal expansion mismatch, is insignificant.

To study the behaviour of a bimorph structure at elevated ambient temperatures, we used the CoventorWare program to simulate the scenario. A 500µm long bi-layer cantilever was modeled. The cantilever consisted of a 30 nm thick oxide film on top of a

300 nm thick Nichrome film. The cantilever was anchored from one end and its other end was free to move. The temperature of the top surface of the cantilever was forced to 393 °K as the boundary condition. After rendering the simulation we plotted the cantilever's vertical deflection (z-axis) along its length. The maximum deflection of the cantilever at its tip due to the thermal mismatch between the two layers was about 29µm. Figure 24 shows the simulation result.

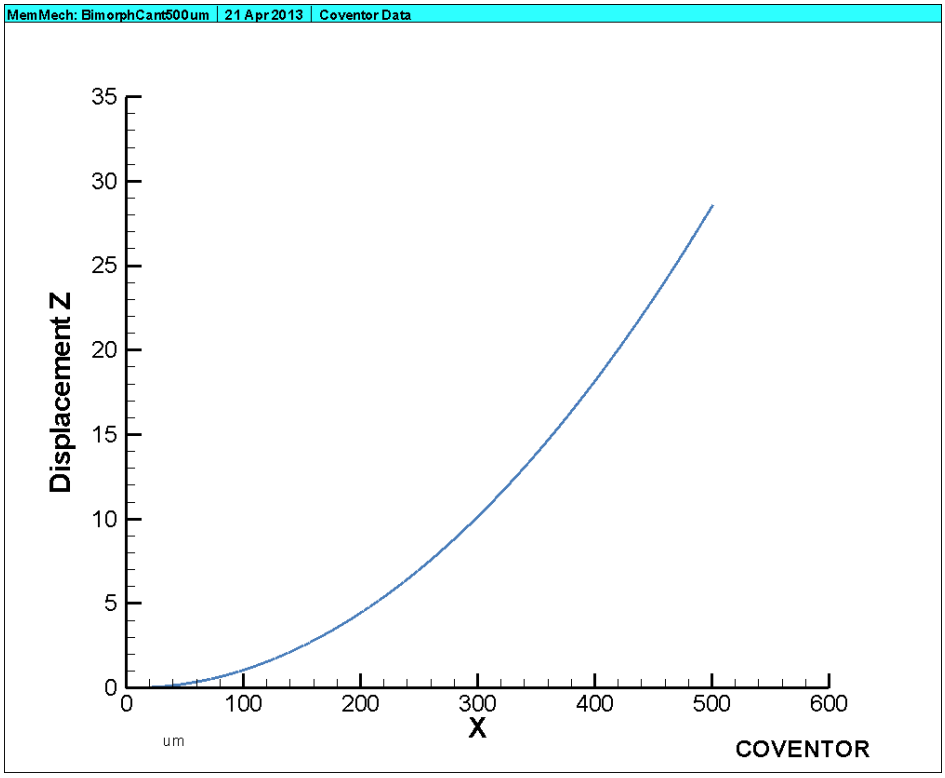


Figure 24: Simulation result of a bimorph film at elevated temperature.

To investigate the uniformity of the thermal property of the deposited film with the embedded compensating layer, we heated a 500 µm-long released cantilever and measured the deflection of the structure's tip due to the elevated temperature. We measured less than 1 µm deflection after heating the cantilever up to 120°C, which clearly shows that the integrated layer thermal expansion coefficient matches perfectly to that of the bulk of the film.

In summary, we demonstrated a technique to compensate for the stress anisotropy in sputter-deposited metal films by embedding a layer in the film with different stress polarity. This is achieved by altering the bias voltage during the film deposition. Using this process, the deformation of the freestanding structures due to the film's stress gradient was minimized, and the thermal mismatch in the deposited film was proven to be negligible. Our process has enabled us to fabricate flat freestanding structures up to a few hundreds of microns at room temperature without requiring any post-deposition high temperature annealing.

4. Application

In this chapter, we present an application example that benefits from the planarization, and the stress anisotropy compensation processes introduced in the previous chapters. The practicality and versatility of these techniques will be illustrated through the fabrication of a functional device that has a significant and growing share in the electronics consumer market. The operation principle, design, fabrication process, assembly, packaging, and test results of the fabricated device will be presented and discussed. An inorganic based post-CMOS compatible fabrication process for an out-of-plane three-axis thermal accelerometer is presented. While we do not emphasize the fabrication of a particular transducer, we chose the three-axis thermal accelerometer to demonstrate a real-world application because of its market potential, ease of design and characterization, and well-studied operating principles [3].

4.1. Out-of-plane structures and Assembly techniques

Conventional photolithography fabrication processes can create structures on the substrate plane. Special mechanisms and assembly techniques are therefore required to achieve an out-of-plane mechanism. Hinged or hinge-less free standing structures can be rotated or pushed out of plane by one of the many existing assembly techniques and locked in their final configuration, if necessary. Assembly techniques can be divided into two broad categories: batch assembly and serial assembly [31]. Batch assembly techniques such as surface tension, non-uniform residual stress, magnetic, or centrifugal, can simultaneously assemble several devices, which make them much faster than the serial techniques. Serial assembly techniques usually require an external device such as a probe or a manipulator to assemble the devices and they can only assemble one or a few devices at a time.

The out-of-plane structure that is necessary for fabrication of our device is basically a sensor plate attached to tip of a cantilever. Using a microprobe, we manually push the cantilever's tip towards its anchor to make the cantilever buckle. When the probe is retracted, the cantilever is locked at its finale shape by an auxiliary cantilever. A small tab at the tip of the auxiliary cantilever is jammed into a small slot in the main cantilever tip to lock the structure in place. The angle that the sensor plate forms with respect to the substrate is only a function of the main cantilever displacement and geometry, and it is independent from the cantilever's material properties or thickness [32] .

4.2. Thermal accelerometer

Micromachined thermal accelerometer was initially introduced in 1997 [51]. Thermal accelerometers have no proof-mass, and they have many advantages over their conventional micromachined counterparts. Due to the lack of a solid proof mass they are mechanically more robust, and they can stand to extreme accelerations up to 50,000 g [52]. Not having a proof-mass makes the fabrication process less complicated and less expensive which is a crucial factor in the manufacturing of products targeting the consumer market. One of the drawbacks of these devices is their slower frequency response compare to that of the conventional micromachined accelerometers.

4.2.1. Operation principle

Most micromachined accelerometers operate on the principle of detecting the displacement of a proof mass caused by acceleration. The proof mass is supported by flexible anchors (springs) and its displacement is measured by different means such as strain gauge, capacitance sensors, and so forth. On the other hand, thermal accelerometer operation principle is based on the effect of acceleration on the free-convection heat transfer from a tiny hot air bubble in a sealed chamber [53]. A tiny pocket of hot air is generated by joule heating around a heater, usually a resistor, which is suspended over a cavity. With no acceleration, there is no temperature difference between two points that are equally distanced from the heater on its opposite sides. When acceleration is applied to the body of the sensor, due to the buoyancy force

experienced by the hot air pocket, temperature gradient around the heater is shifted towards the direction of the acceleration. Shift in the temperature profile causes a temperature difference between the two symmetrical points, and the temperature difference between these two points becomes a measure for acceleration. The symmetrical temperature profile around a heater and the disturbed profile due to acceleration are depicted in Figure 25.

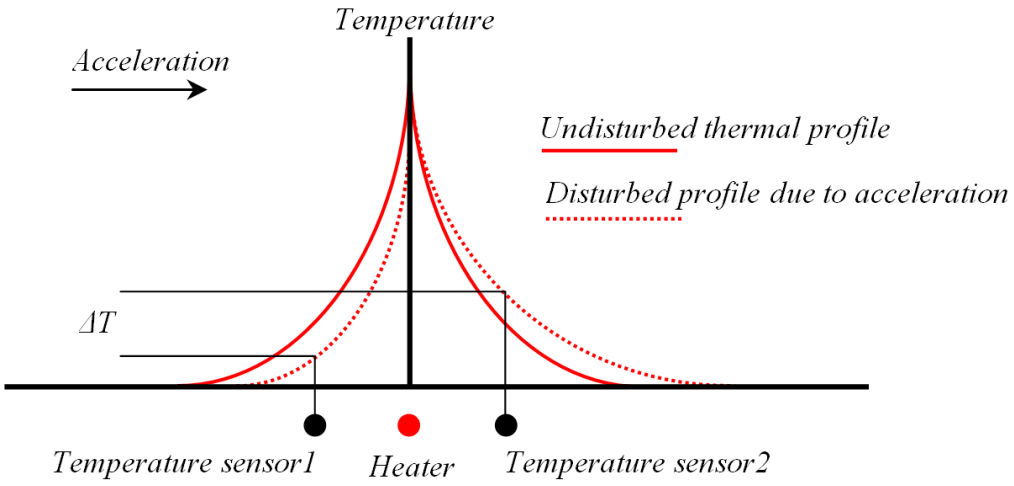


Figure 25: Non-disturbed and disturbed temperature profile around a heater.

A single-axis thermal accelerometer consists of a single heater suspended over a cavity that is etched into a silicon substrate. The cavity provides thermal isolation for the heater, and it enables the formation of a heated air bubble. Two temperature sensors are suspended over the cavity at equal distances from the heater, and they measured the differential temperature. Figure 26 illustrates the conceptual design of a single-axis thermal accelerometer. The device has to be sealed in a chamber (simply a package cavity) to prevent the external airflow from disturbing the device operation. The differential temperature sensor is usually a pair of thermocouples with its hot and cold junctions placed and equal distance from the heater center.

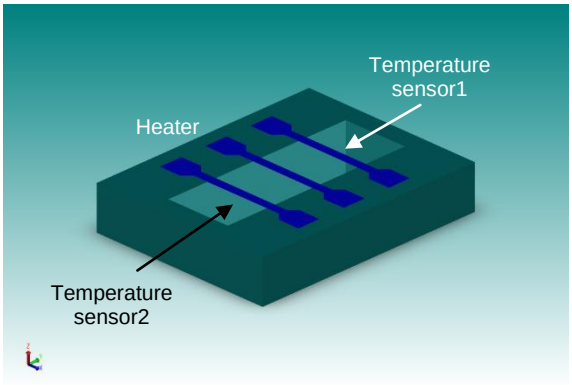


Figure 26: A simple depiction of a single-axis thermal accelerometer.

To add another axis of sensitivity to the device, an extra pair of differential temperature sensor is needed. The axis of the second sensor pair is aligned perpendicular to the axis of the first pair, and the sensors are placed at the same distance from the heater as of the first pair. This configuration allows the device to detect acceleration in both x and y directions. To accommodate the second sensor, the heater shape has to be transformed from a bridge to a small square. Figure 27 shows a dual-axis thermal accelerometer with a small heater source surrounded by two differential temperature sensors.

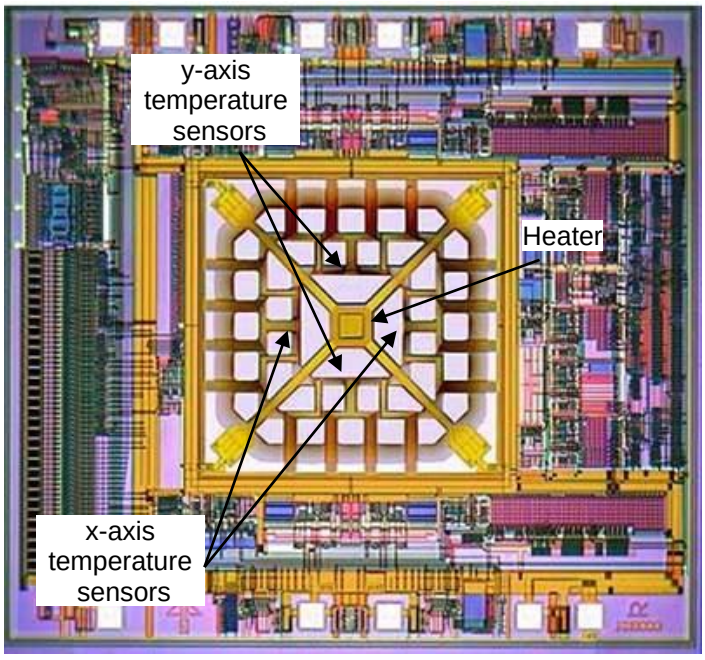


Figure 27: A dual-axis thermal accelerometer. Source, http://www.memsic.com /technology/thermal-mems.cfm, retrieved May 12, 2013.

4.2.2. 3-axis thermal accelerometer

It is almost impossible to add the z-axis (third axis) differential temperature sensor to the structure of a dual-axis thermal accelerometer using the conventional in-plane surface micromachining techniques because the distance between the heater and the temperature sensors is in the order of a few hundreds of microns. Even if one end of a differential temperature sensor is somehow fabricated on top of the heater, the other end has to be implemented almost on backside of the wafer (to maintain the distance from the heater) which makes the process extremely complicated. One solution to this problem is to use out-of-plane structures to integrate the sensor into the design. These out-of-plane structures also provide thermal isolation form the substrate; therefore etching a cavity into the substrate is not necessary. Adding the out-of-plane sensor plate provides lots of flexibility to the sensor design and several different configurations can be used to implement the 3-axis thermal accelerometer.

Perhaps the easiest way to add the third axis of sensitivity to the sensor is to add an independent z-plate. The z-plate is assembled perpendicular to the substrate plane and it includes the necessary elements to form a stand-alone sensor, which are a heater and a differential temperature sensor. The main disadvantage of this design is the silicon efficiency. The z-plate is fabricated on the substrate, and after it is released, it is erected vertically. The foot print of the z-axis sensor plate is almost as big as the x-y sensor, and in order to fabricate the z-plate, die size of the device has to be increased substantially. However, after the z-plate assembly, the underlying silicon area is completely useless, which increases the die size and decreases the silicon efficiency. The conceptual design of a 3-axis sensor with a separate z-plate is illustrated in Figure 28. In Figure 28, H_1 *and* H_2 are the two heaters and Tc_x, Tc_y, Tc_z are the three differential temperature sensors (thermocouples) in the *x*, *y* and *z* directions.

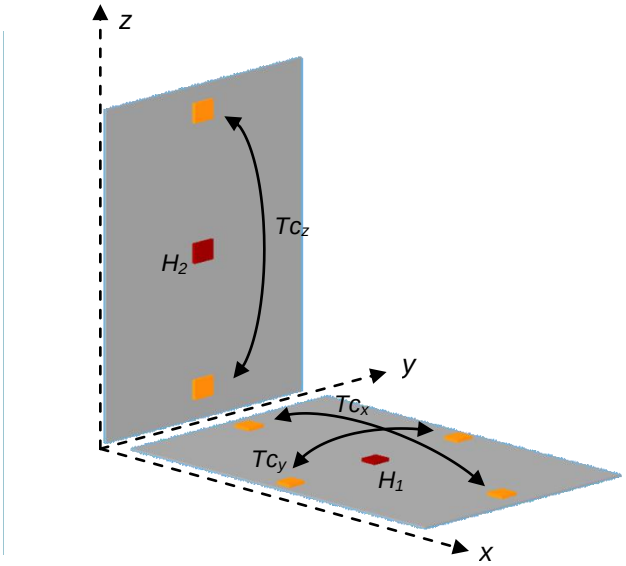


Figure 28: 3-axis accelerometer with z-plate implementation.

An alternative design for a 3-axis accelerometer is to combine the x-y plate and the z-plate into two plates that are pushed out of plane and locked in their positions. The out-of-plane plates provide the thermal isolation necessary for the sensor; therefore, etching a cavity into the substrate is not required. Each plate maintains the same angle with respect to the substrate and contains a heater and two differential temperature sensors. Four differential temperature sensors in total are required to extract the acceleration information for all the three axes. The output of the temperature sensors are not a direct measure for the acceleration and output data for each axis is calculated based on the four measurements from the differential temperature sensors [3].

One possible design configuration for such a sensor is depicted in Figure 29. Each plate carries a heater and two differential temperature sensors (thermocouples) and both plates are oriented to form angle θ with respect to the substrate.

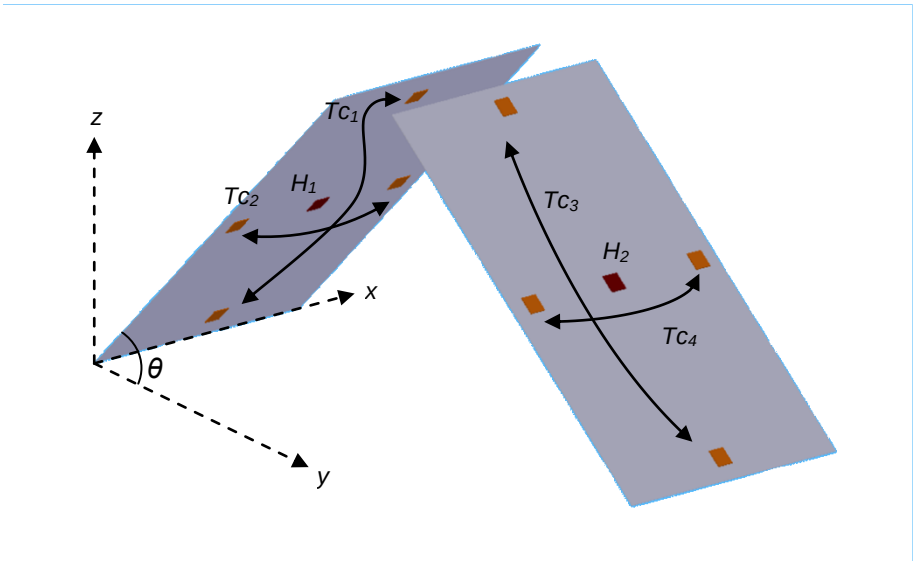


Figure 29: 3-axis accelerometer with two tilted out-of-plane sensor plates.

The following equations govern the relation between the acceleration output data for each axis, the output of four differential temperature sensors, and the angle of the sensor plates with respect to the substrate. The tilt angle contributes significantly to the final signal output; therefore, in order to have identical sensitivity and resolution in the y and z-axis output signals, the sensor plates need to be tilted and locked in placed at 45°. For details about the sensor design and the derivation of the governing equations, please refer to [31]. In (4-1) $\boldsymbol{k_{av}}$ is a constant coefficient that is measured experimentally.

$$\boldsymbol{a_x = \frac{(V_{TC2} + V_{TC4})}{2k_{av}}}$$

$$\boldsymbol{a_y = \frac{(V_{TC1} - V_{TC3})}{2k_{av}\cos\theta}}$$

$$\boldsymbol{a_z = \frac{(V_{TC1} + V_{TC3})}{2k_{av}\sin\theta}} \qquad (4\text{-}1)$$

The sensor configuration that we have adopted in this thesis is based on the same concept of having two tilted out-of-plane sensor plates, but with much smaller footprint. This configuration uses a split-heater on the two tilted sensor plates to form the heated air bubble for all four differential temperature sensors.

4.2.3. Split-heater 3-axis thermal accelerometer

Instead of having two separate heaters surrounded by the two differential temperature sensors on each sensor plate, the split-heater configuration uses two split sensor plates to form a single heater in the space after the plates are assembled. This configuration is very similar to the tilted-plate design and can be constructed if each of the plates are cut into half and then shifted toward each other to form a cross when they are pushed out of plane. The schematic of an assembled sensor is illustrated in Figure 30. In Figure 30, the thermocouple junctions are indicated as '*J*'. Please refer to [3] and [54] for details about the sensor design and characteristics.

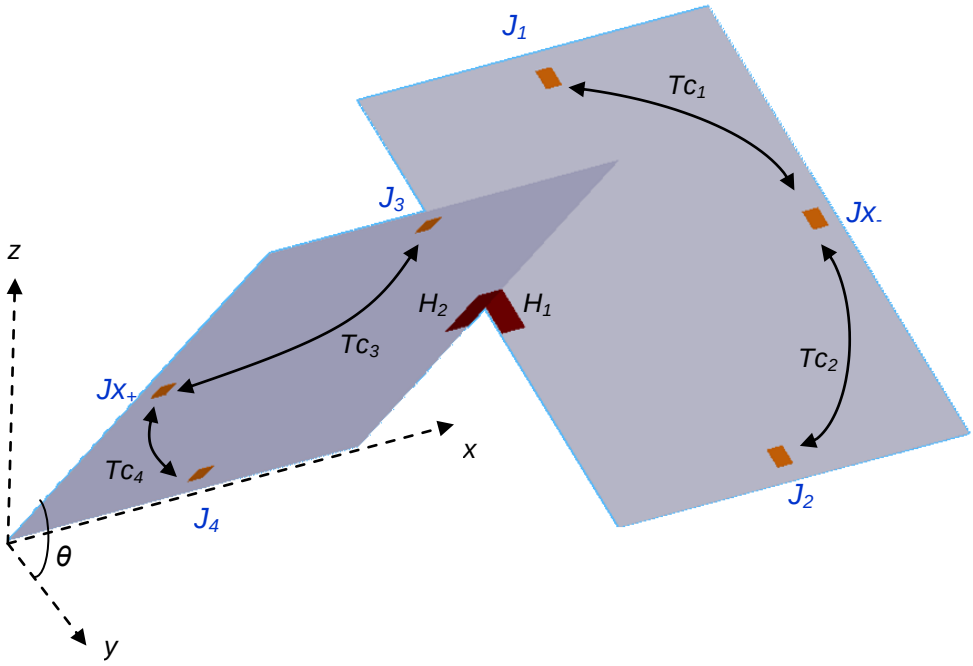


Figure 30: Schematic of an assembled split-heater 3-axis accelerometer.

The differential temperature between the two points across the x-axis (J_{x+}, J_{x-}) cannot be measured directly because of the split design and lack of direct thermocouple connection. However, the output of the four thermocouples shown in the Figure 30 can be used to measure the temperature different across the x-axis. The x-axis acceleration introduces identical temperature changes to Tc_1, Tc_2, Tc_3, and Tc_4. Therefore, the temperature difference between J_{x+}, and J_{x-} is proportional to the sum of the voltages

across the Tc_1, and Tc_2, minus the sum of the voltages across the Tc_3, and Tc_4. The acceleration along each axis can be calculated using the following equations [3]. In (4-2) $\boldsymbol{k_x}$ and $\boldsymbol{k}$ are constant coefficients.

$$\boldsymbol{a_x} = \boldsymbol{k_x}[(-\boldsymbol{V_{TC1}} + \boldsymbol{V_{TC2}}) - (\boldsymbol{V_{TC3}} + \boldsymbol{V_{TC4}})$$

$$\boldsymbol{a_y} = \frac{\boldsymbol{k}}{\cos\boldsymbol{\theta}}[(\boldsymbol{V_{TC1}} + \boldsymbol{V_{TC2}}) - (\boldsymbol{V_{TC3}} + \boldsymbol{V_{TC4}})$$

$$\boldsymbol{a_z} = \frac{\boldsymbol{k}}{\sin\boldsymbol{\theta}}[(\boldsymbol{V_{TC1}} + \boldsymbol{V_{TC2}}) + (\boldsymbol{V_{TC3}} + \boldsymbol{V_{TC4}}) \qquad (4\text{-}2)$$

4.3. Accelerometer design

The design of the sensor in this thesis has been adopted from the work of Bahari *et al.* [3], [54]. The sensor structure has been modified from its original state to facilitate the fabrication process (in order to have less critical dimensions). The design details and the parameters that affect the sensor performance and its output characteristics are beyond the scope of this work and they are found in [3]. An overview of the sensor design is presented here to depict an image of the sensor and its structure and to help better understanding the fabrication process. The anatomy of the sensor is divided into two broad sections; mechanical layers and electrical layers. The mechanical layers consist of anchor, sacrificial layer, and structural layers that together enable the fabrication of an out-of-plane sensor plate. The electrical layers form the bonding pads, electrical connections, heaters and the thermocouples.

4.3.1. Sensor plate

Each sensor plate contains half of a heater and two differential temperature sensors (thermopiles) as it is illustrated in Figure 31. To increase the device sensitivity four thermocouples are connected in series to form a thermopile. The two thermopiles have a common connection at the J_x junction and the other junctions are placed across the heater. To increase the resistance, the heater is designed as a serpentine in the middle of the sensor plate, and it is connected to the bonding pads through low resistance tracks. The low resistance connection to the bonding pads localizes the joule

heating to the heater area and minimizes the heat dissipation along the track which could potentially offset the sensor output.

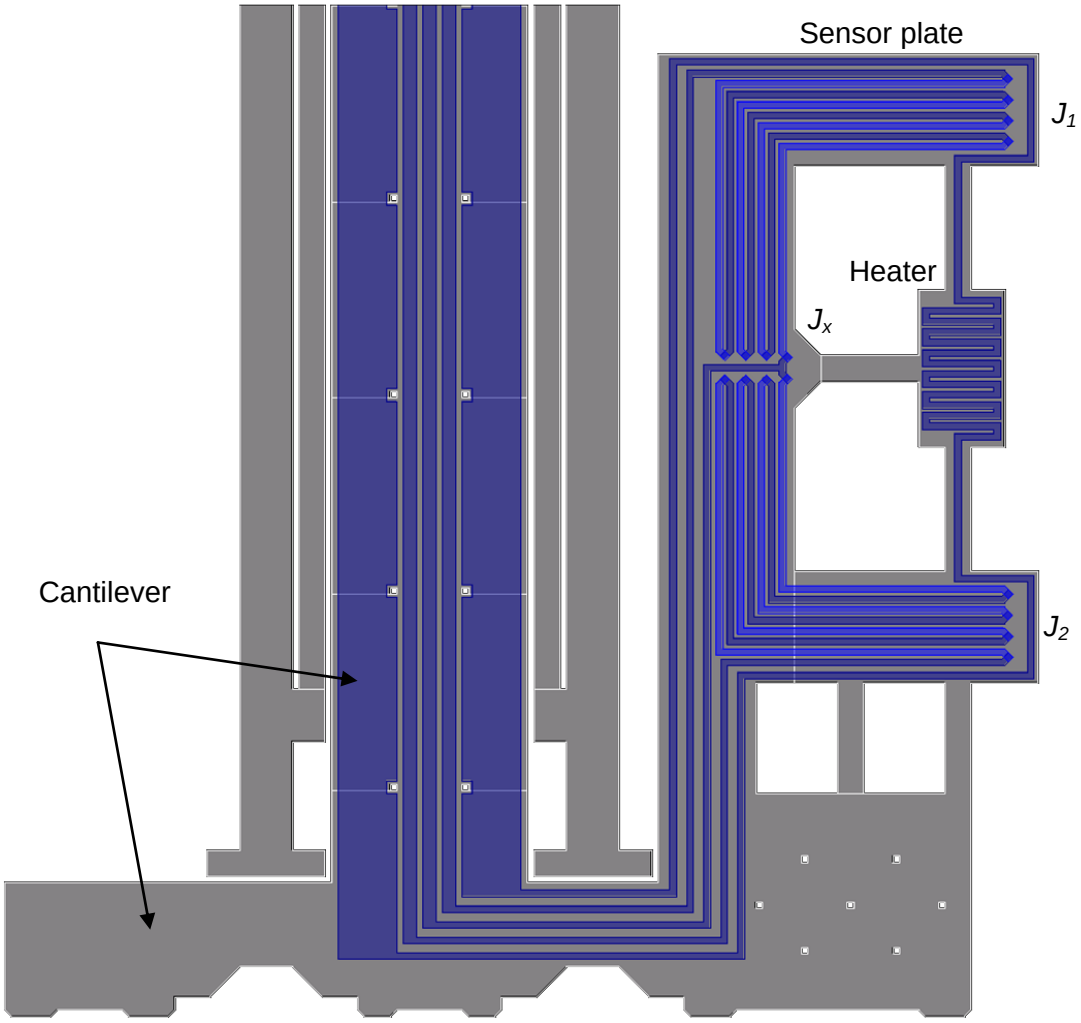


Figure 31: Layout of the sensor plate with the heater and the thermopiles.

Nichrome (Nickel 80%, Chromium 20%) was chosen as the heater material because of its high resistivity, stability (low oxidation rate), and good adhesion. To reduce the resistance of the electrical connections, the nichrome wires were over-coated by aluminum, which also forms the bonding pads. The sensor plate is connected to the tip of a cantilever that is anchored to the substrate at its other end. The electrical connections between the heater, the thermopiles and the bonding pads were routed through the main cantilever. The thermocouple junctions are formed between Nichrome

and a Nickel-Copper alloy (Nickel 67%, Copper 33%) with Seebeck coefficient of around 30 μV/°C. Nickel-Copper alloy was chosen to build the thermocouples because of it good adhesion to the oxide and the relatively large Seebeck coefficient of the formed junction.

4.3.2. Main cantilever and locking mechanism

The main cantilever is a compliance mechanism that is pushed to buckle out of plane with the sensor plate attached to its tip [31], [32]. An external probe (e.g., a wire-bonder tip) is used to assemble the cantilever by pushing its tip towards the cantilever anchor. Two locking cantilevers on each side of the main cantilever lock the buckled structure in place. The buckled cantilever, the locking mechanism and the tilted sensor plated are shown in Figure 32. The main cantilever is a T-shape structure with two recesses (slits) that are wide enough for the locking cantilever body to pass through; however, the tip of the locking cantilevers cannot pass through this slit. To assemble the structure, the main cantilever is pushed back far enough to pass over the locking cantilever tip. When the main cantilever buckles, the auxiliary cantilevers (tethers) slightly lift up the locking cantilevers. When the probe is retracted and the main cantilever is released, the locking cantilevers tips hold the main cantilever and lock it in place.

The angle that the sensor plates forms with respect to the substrate (when it is assembled), is dictated by the main and the locking cantilevers design. This angle is independent of the cantilever's thickness or material and it is only a function of design geometry [32].

4.3.3. Anchor and bonding pads

The main cantilever is anchored to the substrate through an etch-resistant patch that is created by the method explained in chapter 2. This patch has the same thickness as of the sacrificial layer and eliminates the step between the structural layer at its anchor. With planar structure the conformal step coverage of the deposition process for the electrical layers is not an issue which grantees a reliable electrical connection to the

sensor plate. The aluminum overcoat on the Nichrome lines is extended all the way to the bonding pads area and the chip is wire bonded through the aluminum layer.

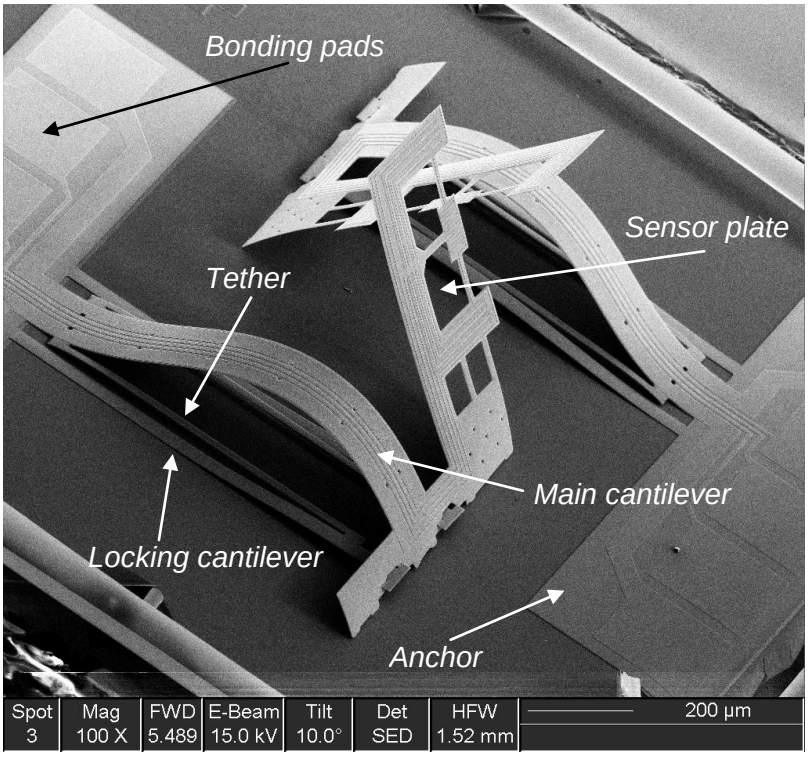


Figure 32: The buckled main cantilever with the locking mechanism.

4.4. Accelerometer fabrication and test result

In this section the layout and the fabrication process of the accelerometer is explained. As we mentioned before the sensor design and layout has been adopted from [3], and [54], but the fabrication process is new, and takes advantage of the techniques that we presented earlier in this thesis. The process steps, with depiction of the corresponding mask, are briefly explained. The fabrication process details are included in Appendix A for the reference.

4.4.1. Sensor layout

The layout of the accelerometer is illustrated in Figure 33. The centerline of the thermopile junctions on each sensor plate (J1-J2 and J3-J4) is slightly protruded with

respect to the centerline of the heaters. This protrusion guarantees that the four junctions are align with the center of the heated air bubble that is formed by the two split heaters. The distance between the centers of the heaters, (*d*), ensures that the heaters are perfectly aligned and form a cross when the device is assembled to its final out-of-plane configuration.

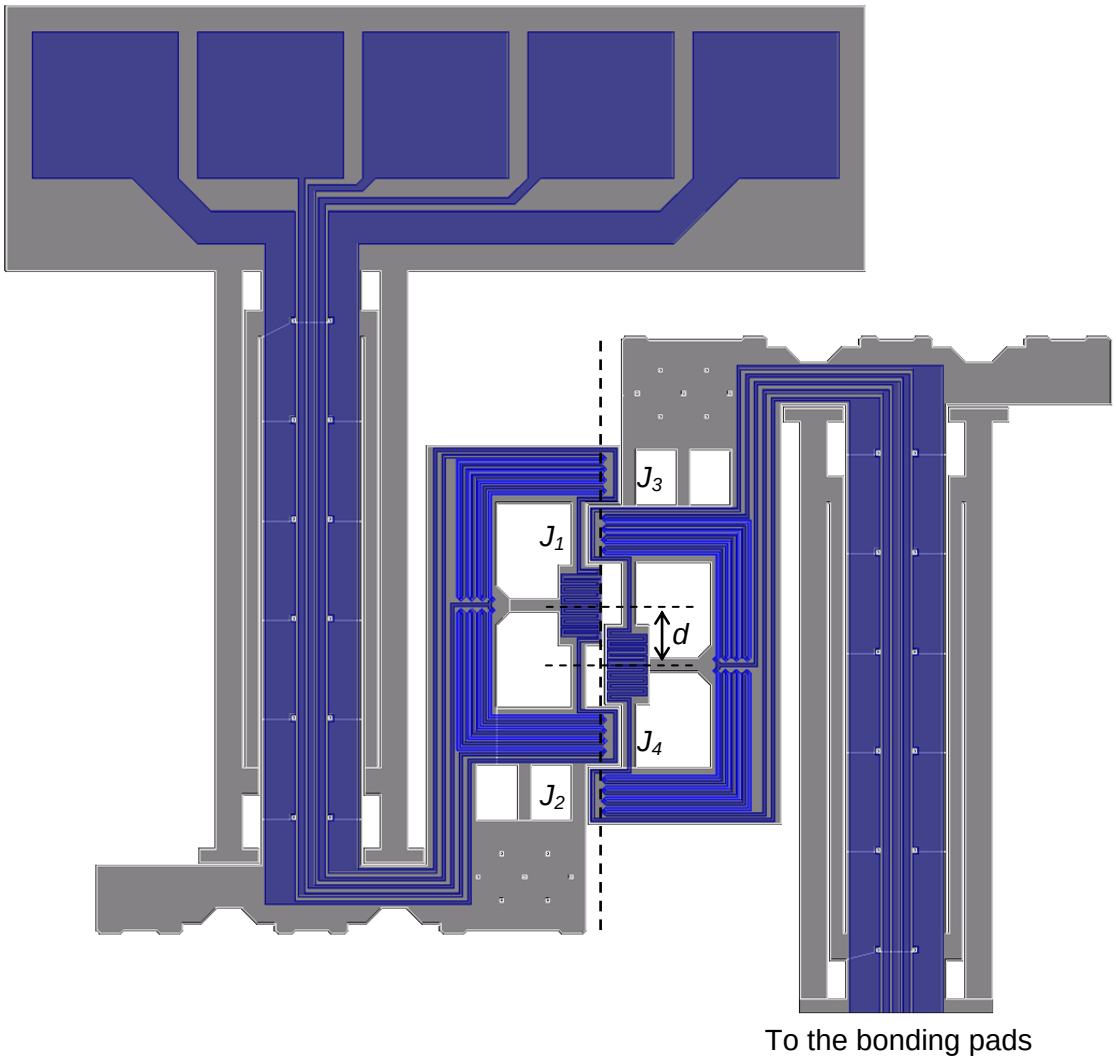


Figure 33: Layout of the split-heater accelerometer.

4.4.2. Sensor fabrication

Fabrication process of the sensor requires 6 masks and 10 different layers. Figure 34 shows the fabricated device before the release and assembly steps. The

anchor mask (dark field) is used to make the device anchors by taking advantage of the planarization technique explained in chapter 2. The composite structural layer is deposited after the anchors are formed. The structural layer has 3 layers and consists of two layers of PECVD oxide on top and bottom of a Nichrome layer. We used the technique that was explained in chapter 3 to compensate for the Nichrome film stress anisotropy. After the first oxide layer deposition we deposited and patterned a layer of aluminum by the second mask (grid) to form the electrical grid before the Nichrome film deposition. After DC sputtering of the Nichrome film by variable bias voltage, the top oxide layer is deposited to finalize the structural layer construction. Figure 35 illustrates the anchor and grid mask layout. The grid runs around the die perimeter and does not interfere with the chip design.

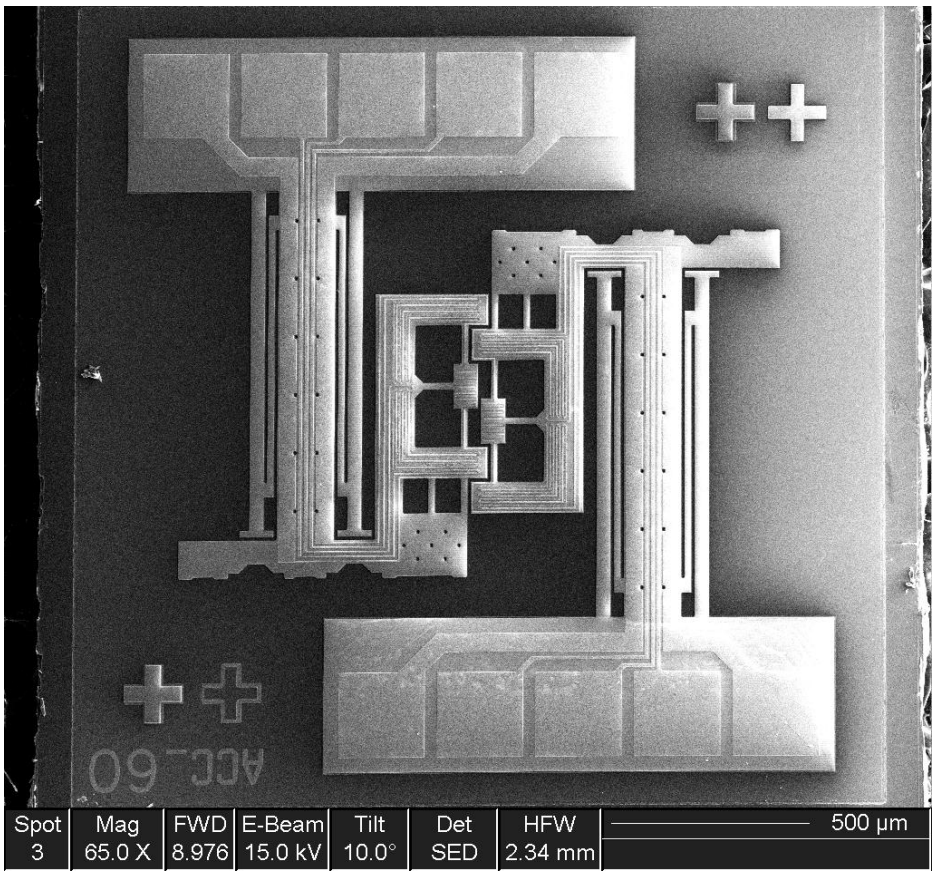


Figure 34: Fabricated accelerometer before release and assembly steps.

The structural layer is patterned after all electrical layers are deposited and patterned. The first electrical layer is aligned to the anchor layer, but the structural layer

is aligned to the first electrical layer before patterning. To form the heaters, the first junction of the thermocouples, the bonding pads and the electrical connections, a stack of Nichrome and aluminum films is deposited without breaking the vacuum. The Nichrome film is not exposed to the atmosphere before sputtering the aluminum to prevent oxidation and loss of adhesion between the two layers. These two layers are self-aligned and patterned by the third mask (wire) using wet etching. Figure 36 shows the layout of the third mask. Each thermopile consists of four thermocouples that are connected in series. After patterning the Nichrome-Aluminum stack, the aluminum layer over the undesired areas (the heater and the thermocouple junctions) has to be removed. To form the thermocouple junctions, the aluminum layer has to be removed to expose the Nichrome layer. Removing the aluminum layer from the heater increases the heater resistivity drastically and ensures that the joule heating is concentrated in that area.

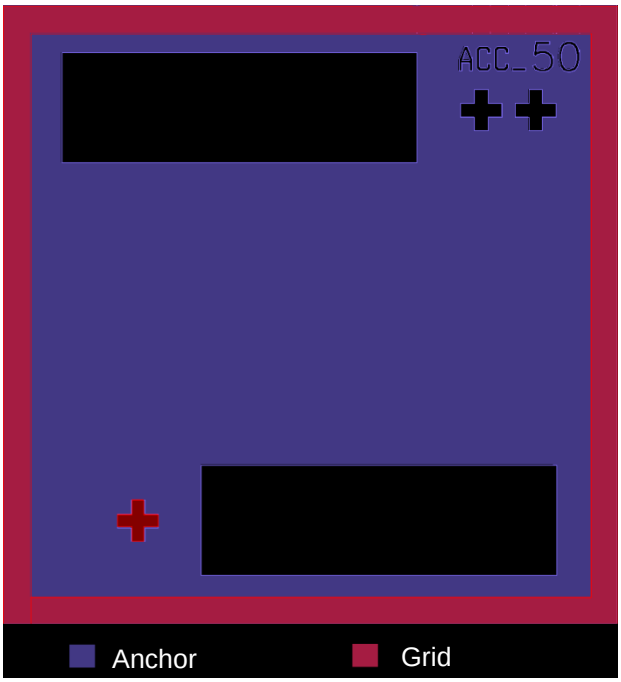


Figure 35: Anchor and metal grid masks layout (mask 1 & 2).

The excellent wet-etch selectivity between the Nichrome and the aluminum layer enabled us to easily remove the unwanted aluminum on top of the Nichrome. The fourth mask (a dark-field mask) was used to remove the aluminum from the heater and the thermocouple junctions. The mask layout is illustrated in Figure 37. To complete the

thermocouple junctions, the second metal (nickel-copper alloy) is deposited and patterned using the lift-off technique (mask 5). A lift-off resist is spun and cured before spinning the photoresist layer in order to create a re-entrant profile when the photoresist is developed. The re-entrant profile creates discontinuity in the film at the edge of the patterned areas and enhances the lift-off process. Layout of the lift-off mask is shown in Figure 38.

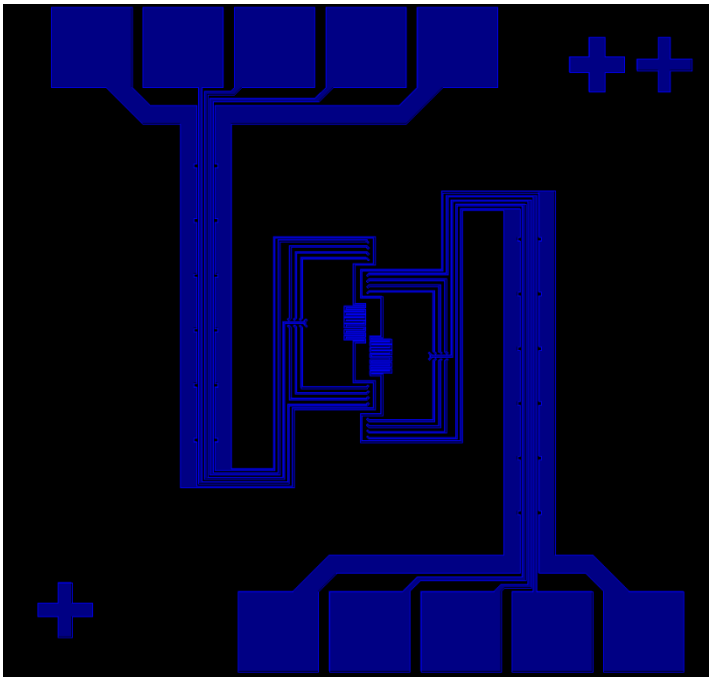


Figure 36: Layout of the third mask that forms the electrical connections, the heater, and the bonding pads.

By finishing the thermocouple structure by the nickel-copper alloy deposition, all the necessary electrical layers and components to form the accelerometer are completed. The next step towards finalizing the sensor fabrication is to pattern the composite structural layer by the structure mask (mask 6). All three layers of the structural layer are self-aligned and patterned using the final mask. The top and bottom oxide layers are dry etched using fluorine based RIE, and the Nichrome layer is wet etched. Over etching the oxide layers does not affect the process; therefore, we timed the RIE etch process for end-point detections. The layout of the structural layer mask is illustrated in Figure 39.

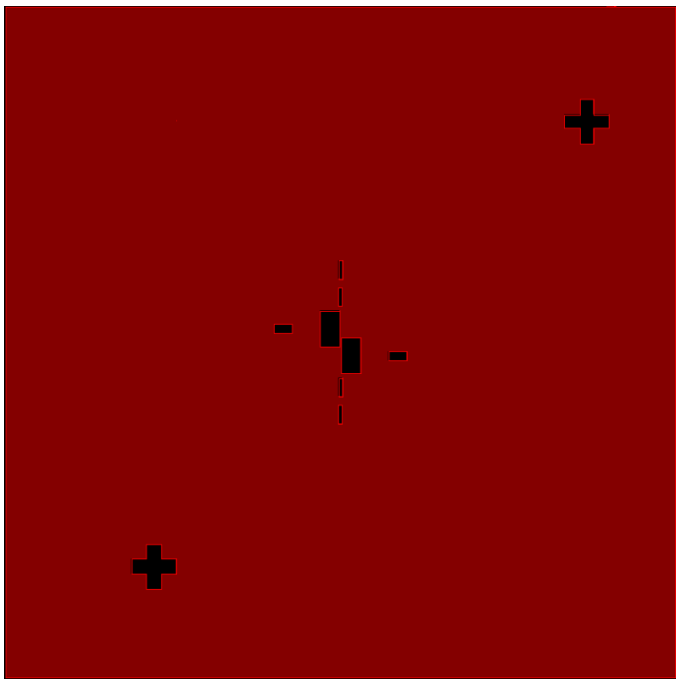


Figure 37: The fourth mask (dark-field) layout. It was used to remove the aluminum from undesired areas.

After the structural layer is patterned, the wafer is diced into individual dies and each die is mounted into a 16-pin DIP ceramic package. We release and assemble the structure after we packaged and wire bonded the chip; this increases the packaging and the assembling yield significantly. The chip is wire-bonded using a ball-wedge bonder and gold wire. The wired package is placed into the Xenon Difluoride gas-phase etching machine to etch the sacrificial layer (amorphous silicon) and to release the structures from the substrate.

To assemble the structure into its out-of-plane configuration we used a probe to push the main cantilever back until it passes the locking cantilever tip. At this point the auxiliary cantilever (tether) has lifted the locking cantilever and if the main cantilever is released, it will be hold in place by the locking cantilever. Figure 40 shows the assembled accelerometer.

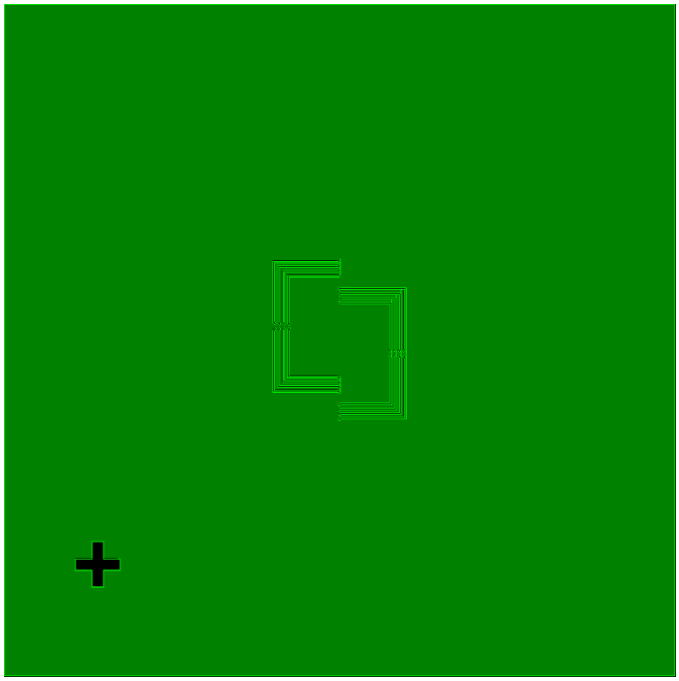


Figure 38: The fifth mask layout. It was used to lift-off the NiCu alloy for the thermocouple's second junction.

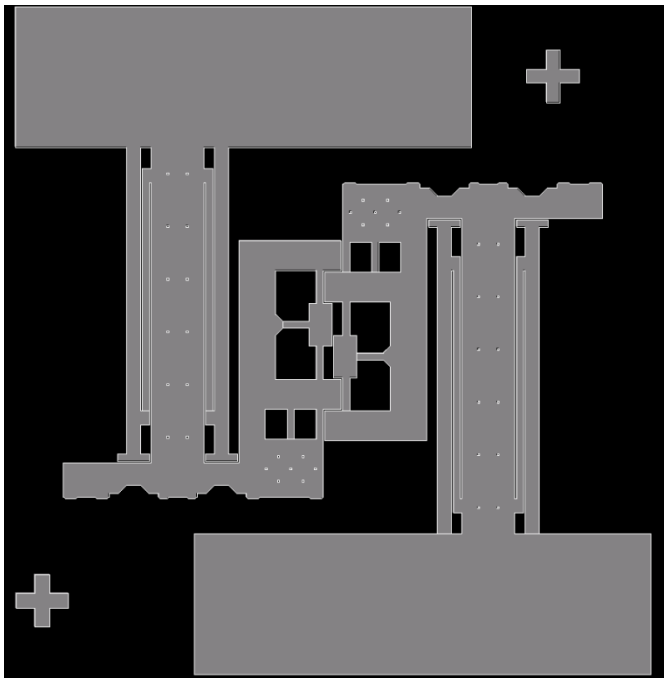


Figure 39: Layout of the sixth mask. It was used to pattern the structural layer.

To finalize the device packaging, the package cavity is covered by a metal lid that forms the top heat sink. The distance between the heater and the substrate is

supposed to be equal to the gap between the heater and the metal lid. The top heat sink makes the device output symmetrical when the device is rotated along the x and y axes. To increase the device sensitivity the package cavity has to be filled with heavy gases like SF_6. The effect of the gas type on the device sensitivity and the procedure for filling the package cavity with the desired gas can be found in [31], [55].

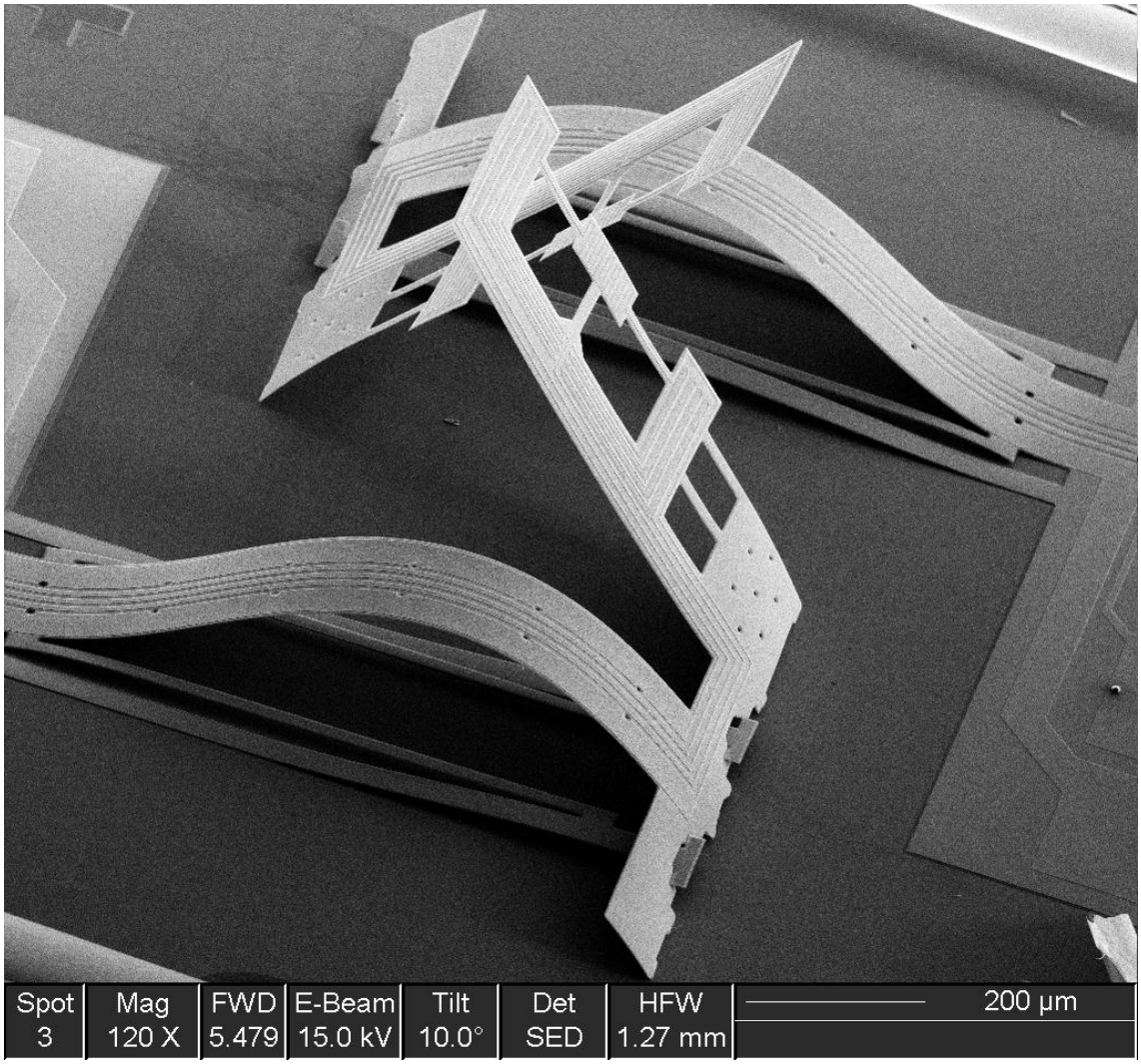


Figure 40: Assembled accelerometer into its final out-of-plane configuration.

4.4.3. Test result

The output of a single thermopile was measured in order to test the device functionality. The complete test results and output values for all three axes can be found in [3]. To test the thermopile output we mounted the device on a rotating stage and oriented the packaged device so that the thermopile's corresponding plate becomes parallel to the rotating stage plane. The rotating stage plane was kept vertical in order to measure the effect of the gravitational acceleration on the sensor output.

The heater was powered by a simple resistive circuit and the heater current was manually adjusted (using a trimming potentiometer) to limit the heater power dissipation to 2.5 mW. Heater's nominal resistance was about 2.5 kΩ. We used a simple amplifier to amplify the thermopile (four thermocouple in series) output and to shift the output signal into the mV range. Figure 41 depicts the thermopile test circuit.

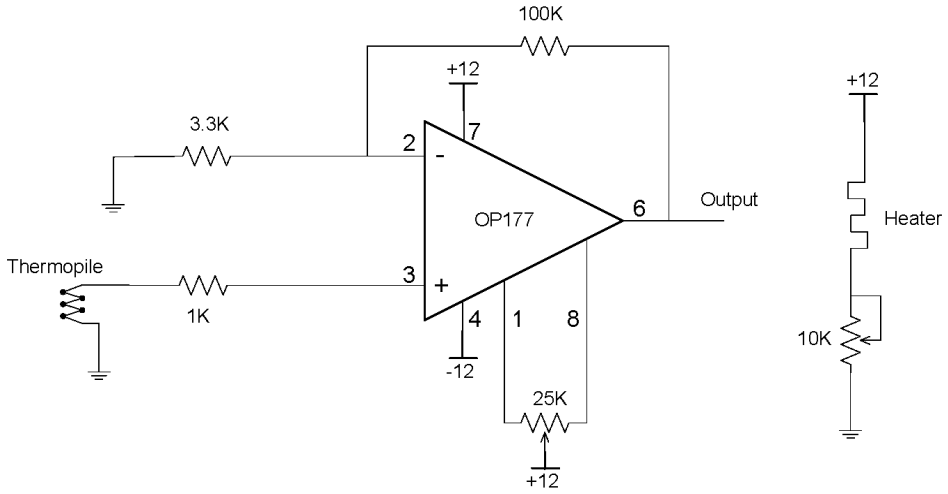


Figure 41: Amplifier circuit for the thermopiles.

The thermopile's amplified output versus the angle of rotation is plotted in Figure 42. The offset of the output signal is due to the thermopile position relative to the heater. In our test setup the axis of rotation is along the x-axis; therefore, "x" junction of the thermopiles is always at an elevated temperature (compare to the thermopile other junction) regardless of the angle of rotation. This imbalance heat distribution causes the offset in the output signal. Please refer to Figure 31 for details about the sensor plate layout and the "x" junction location with respect to the heater.

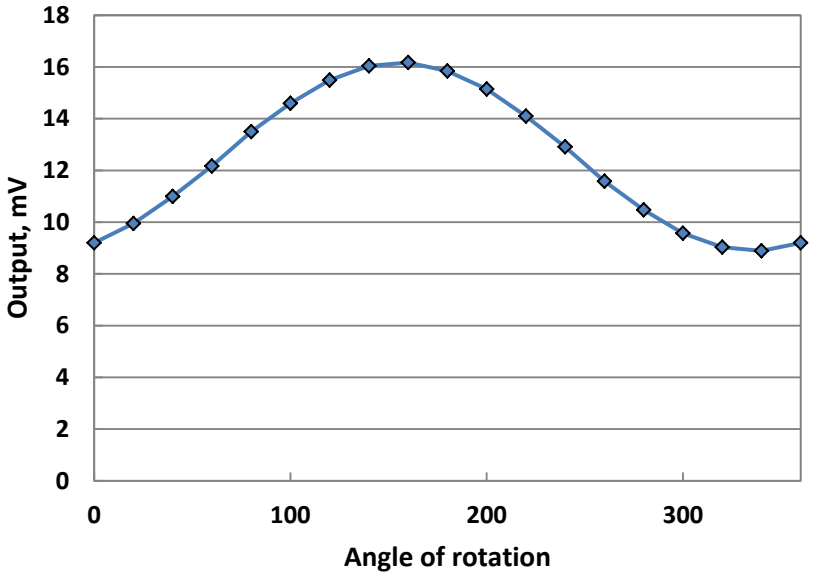


Figure 42: Single thermopile output with respect to the angle of rotation.

To conclude, we presented an example of potential applications for the planarization, and stress anisotropy compensation processes that were introduced earlier in this thesis. The practicality and versatility of these techniques was demonstrated through the fabrication of a 3-axis thermal accelerometer that has a significant and growing share in the electronics consumer market. The operation principle, design, fabrication process, assembly, packaging, and test results of the fabricated device was presented and discussed. The electrical measurement was merely performed to demonstrate the success in fabricating a functional 3-axis thermal accelerometer using the processes developed in this research. The detailed characterization of the device is not the focus and is beyond the scope of this thesis and can be found in [3], [54].

5. Contributions and future works

We originally introduced the idea of using the nickel silicide for planarization in the sacrificial surface micromachining processes in a journal paper and a conference paper:

I. *Khosraviani K, and Leung A M 2009 The NanoGap Pirani — A Pressure Sensor with Superior Linearity in Atmospheric Pressure Range J. Micromech. Microeng 19 p045007*
II. *Khosraviani K, and Leung A M 2009 Planar Sacrificial Surface Micromachining by Nickel Silicide the 15th international conference on solid-state sensor and actuators and Microsystems, Transducers p1051-4*

The modified process that enabled us to increase the sacrificial thickness to a few hundreds of microns was introduced in another conference paper:

III. *Khosraviani K, Bahari J, and Leung A M 2011 Robust Micromachining of Compliant Mechanisms by Nickel Silicide The 24th International Conference on Micro Electro Mechanical Systems MEMS p316-9*

To overcome the stress-hump formation and to increase the process yield and reproducibility we modified the process and presented a more advanced process in a journal paper:

IV. *Khosraviani K, and Leung A M 2013 Robust Micromachining of Compliant Mechanisms by Silicides Journal of Micromechanics and Microengineering 23 p015015*

The compensation method for balancing the stress anisotropy across the thickness of the sputter-deposited metal films and its results was published in a journal:

V. *Khosraviani K, and Leung A M 2013 Stress anisotropy compensation of the sputter-deposited metal thin films by variable bias voltage Journal of Micromechanics and Microengineering (in press Ref: JMM/463219/PAP/206806)*

To best of our knowledge, we are the first group who has introduced the planarization, and stress anisotropy control techniques presented in this thesis. These processes use only inorganic materials that are compatible with the standard industrial practices. To further enhance the processes reliability, reproducibility, and controllability we are suggesting a few ideas for further investigations and for the future works.

As we mentioned earlier, we replaced the bottom nickel silicide layer (the etch-stop layer) with Nickel-Chromium silicide. The deposited Nichrome layer diffused into the silicon substrate at temperatures as low as 350°C and formed silicide. We believe that nickel (to form the anchors) can be replaced by a binary or even ternary nickel alloy, and the formed silicide properties can be tailored by engineering the alloy composition. Silicon consumption, percentage of growth above the initial silicon interface, and the volume increase in the formed silicide, are the main characteristics that could potentially be controlled to increase the process yield and reproducibility.

We compensate for the effect of the stress anisotropy across the thickness of a sputter-deposited metal film by embedding a layer in the film with opposite stress sign compare to that of the bulk of the film. Theoretically, number of these layers can be increased, and these layers can be spread uniformly throughout the film thickness. To control the stress level and polarity of each of these layers, the magnitude and pulse width of the bias voltage has to be adjusted for each cycle. Perhaps, a completely amorphous film as oppose to a polycrystalline film can be deposited by this technique.

As it is indicated by the flat sensor plate in Figure 40, the mechanical effect of the electrical layers on the sensor plate was minimized in our process. We achieved this by minimizing the electrical connections width and their layer's thicknesses, and by carefully selecting the deposition parameters (pressure and power). To further diminish the effect of the stress mismatch between the electrical layers and the structural layer, the electrical layer mechanical properties can be tailored by biased sputter deposition. One can easily apply the same technique that we applied to the Nichrome layer (middle layer

of the structural layer), in order to minimized the stress gradient and intrinsic stress level of these layers. This requires an additional grid for applying voltage to the growing film, or use of an RF source to bias the substrate. An alternative to this process is to over-compensate the structural layer to balance the effect of the electrical layers. Without the electrical layers, the over-compensated structural layer will bend but the electrical layers cancel out this effect and the overall sensor plate remains flat.

6. Conclusion

We presented an inorganic-based post-CMOS compatible process for fabricating compliant mechanisms upon which out-of-plane structures for micro sensors and actuators can be made. The presented process took advantage of two novel techniques: a planarization technique and a compensation technique for the stress anisotropy across the thickness of the sputter-deposited metal films.

To enhance the mechanical robustness of freestanding microstructures and compliant mechanisms, and to facilitate the fabrication, and improve the assembly yield of the out-of-plane micro sensors and actuators, we introduced an innovative planarization technique. Fabrication of a compliant mechanism using conventional sacrificial surface micromachining results in a non-planar structure with a step between the structure and its anchor. During mechanism actuation or assembly, stress accumulation at the structure's step can easily exceed the yield strength of the material and lead to the structure failure. Our process overcomes this topographic issue by eliminating the step between the structure and its anchor, and achieves planarization without using Chemical Mechanical Polishing (CMP). The process was based on low temperature and post-CMOS compatible nickel silicide technology. We used a layer of amorphous silicon (a-Si) as a sacrificial layer, which was locally converted to nickel silicide to form the anchors. High etch selectivity between silicon and nickel silicide in the Xenon Difluoride gas (sacrificial layer etchant) enabled us to use the silicide to anchor the structures to the substrate. The formed silicide had the same thickness as the sacrificial layer; therefore, the structure was practically flat. The maximum measured step between the anchor and the sacrificial layer was about 10nm on a 300nm thick sacrificial layer. The experimental results showed a significant improvement in the assembly yield of the compliant mechanisms that were fabricated by our proposed planarization technique.

To balance the effect of the stress anisotropy across the thickness of sputter-deposited metal films we introduced a novel compensating technique. Our technique balanced the film vertical stress gradient by altering the substrate bias during sputtering, and by controlling the ion flux and energy that bombards the growing film. Sputter-deposited metal films are appealing materials for microfabrication of freestanding and out-of-plane structures, especially because of their low thermal budget. These microstructures extend the design space of Micro-Electro-Mechanical-Systems (MEMS) based devices, and they overcome some of the limitations of in-plane processing. Unfortunately, most elemental metals and alloys when sputter deposited have a substantial stress gradient across their thickness that can deteriorate their mechanical properties and severely distort the shape of the fabricated freestanding microstructures.

We compensated (balanced) the stress gradient across the thickness of a sputter-deposited film by embedding a layer in the film with the opposite stress polarity compared to that of the bulk of the film. The force exerted by the stress mismatch between this layer and the bulk of the film easily overcomes the film's vertical stress gradient. This compensating force guarantees that a released freestanding structure remains flat and does not curl upward. This layer was introduced to the growing film by altering the substrate bias voltage during the sputtering process. The substrate bias voltage controls the ion flux and energy that bombards the film and it enabled us to tailor the film stress parameters and to embed a thin layer in the film with a different stress polarity. Using this process, the corresponding structural deformation of the freestanding structures due to the film's stress gradient was minimized, and the thermal mismatch in the deposited film was proven to be negligible. Our process has enabled us to fabricate flat freestanding structures up to a few hundreds of microns at low temperatures without requiring any post-deposition high temperature annealing.

Appendix

Appendix A

3-axis thermal accelerometer fabrication run-sheet

In this appendix, the process steps and parameters for fabrication of a 3-axis thermal accelerometer, based on the presented planarization and stress anisotropy compensating techniques in this thesis, has been listed. The listed process time and temperatures are all typical, and might vary if they are attempted with a different set of machines or equipment.

#	Process title	Process parameters
Substrate preparation		
1	RCA-SC1 clean	5:1:1, DI water, Ammonium Hydroxide , Hydrogen peroxide, at 80°C for 10 minutes
2	Native oxide removal	10:1, DI water, 48% HF for 1 min Note: this step is important otherwise the native oxide prevents the bottom silicide formation
Etch-stop layer and sacrificial layer deposition		
3	Nichrome sputtering	3” target Base pressure: less than $2x10^{-7}$ Torr Deposition pressure: 1 mTorr Source power: 150 W Deposition time: 40 seconds Thickness: 20 nm
4	a-Si deposition	100% Silane Base pressure: less than $5x10^{-7}$ Torr Deposition pressure: 350 mTorr Deposition temperature: 350°C Source power: 2 W Deposition time: 30 minutes Thickness: 300 nm Note: deposition without breaking the vacuum.
5	Bottom silicide formation	Annealing in 5% forming gas atmosphere (Hydrogen balanced in Nitrogen) at 350°C for 10 minutes

#	Process title	Process parameters
Anchor formation		
6	PECVD Oxide mask deposition (diffusion mask)	10% Silane in Argon: 10 sccm Nitrous Oxide: 80 sccm Deposition pressure: 250 mTorr Deposition temperature: 250 °C Deposition time: 10 minutes Thickness: 200 nm
7	Photoresist spinning and patterning	-Spin S1813 photoresist at 3500 RPM for 30 seconds. -Soft-bake at 110 °C for 1 minute and 30 seconds. -Exposure using the first mask (dark-field). Exposure time varies according to the UV source dose (typically 9 seconds at 20 mW/cm^2). -Develop in MF319 at room temperature for 40 seconds. -Hard-bake at 110 °C for 2 minutes
8	Diffusion mask etching and photoresist removal	-Etch in BOE at room temperature for 1 minute. -Stripping photoresist by acetone (double bath).
9	a-Si partial etch in RIE	CF4: 50 sccm O2: 5 sccm Pressure: 100 mTorr Power: 200 Watts Etch time: 1 minute Approximate etch depth: 45 nm
10	Nickel e-beam evaporation	Base pressure: less than $5x10^{-7}$ Torr Deposition pressure: less $5x10^{-6}$ Torr e-beam current: 100 mA e-beam Voltage: 10 Kv Deposition rate: ≈ 1Å/sec Thickness: 200 nm Note: nickel has to be evaporated directly from the hearth.
11	Top silicide formation	Annealing in 5% forming gas atmosphere at 350°C for 40 minutes
12	Etching the non-reacted nickel	1:1, sulphuric acid (90%), and hydrogen peroxide (40%) at 85°C for 5 minutes

#	Process title	Process parameters
13	Oxide mask removal	In BOE at room temperature for 1 minute.
Structural layer deposition		
14	Bottom structural oxide layer deposition	10% Silane in Argon: 10 sccm Nitrous Oxide: 80 sccm Deposition pressure: 250 mTorr Deposition temperature: 250 °C Deposition time: 15 minutes Thickness: 300 nm
15	Sputter deposit aluminum for electrical grid	Base pressure: less than $2x10^{-6}$ Torr Deposition pressure: 1 mTorr Source power: 250 W Deposition time: 5 minute Thickness: 300 nm
16	Etching aluminum layer to form the grid	-Standard photolithography process stated in step 7. Used the second mask. -Aluminum etch in Transene type A aluminum etchant Etch time: 80 seconds Etch temperature: 45 °C -Stripping photoresist by acetone (double bath).
17	Structural Nichrome layer deposition	Base pressure: less than $2x10^{-7}$ Torr Deposition pressure: 1 mTorr Source power: 150 W Deposition time: 15 minutes Thickness: 500 nm Note: This layer is sputtered by variable bias voltage to compensate for the film vertical stress gradient.
18	Top structural oxide layer deposition	10% Silane in Argon: 10 sccm Nitrous Oxide: 80 sccm Deposition pressure: 250 mTorr Deposition temperature: 250 °C Deposition time: 15 minutes Thickness: 300 nm

#	Process title	Process parameters
Bonding pads, electrical connections, and heater formation		
19	Electrical Nichrome layer	Base pressure: less than $2x10^{-7}$ Torr Deposition pressure: 1 mTorr Source power: 150 W Deposition time: 3 minutes and 30 seconds Thickness: 100 nm
20	Aluminum overcoat layer	Base pressure: less than $2x10^{-6}$ Torr Deposition pressure: 1 mTorr Source power: 250 W Deposition time: 5 minutes Thickness: 300 nm Note: aluminum layer was deposited without breaking the vacuum.
21	Patterning the NiCr-Aluminum stack	Two layers are self-aligned. Third mask used. -Standard photolithography process stated in step 7. -Aluminum etch in Transene type A aluminum etchant Etch time: 80 seconds Etch temperature: 45 °C -Nichrome etch in Transene 1020AC Chromium etchant Etch time: 90 seconds Etch temperature: 45 °C -Stripping photoresist by acetone (double bath).
Thermocouple formation		
22	Removing the extra aluminum to form the heater and expose the Nichrome to make the thermocouples.	Fourth mask used (Dark field). -Standard photolithography process stated in step 7. -Aluminum etch in Transene type A aluminum etchant Etch time: 80 seconds Etch temperature: 45 °C -Stripping photoresist by acetone (double bath).
23	Bilayer Lift-off layer preparation	Fifth mask used (Dark field). Used MicroChem LOR-10A Spin at 3500 RPM 45 seconds

#	Process title	Process parameters	
		Softbake at 160 °C	100 seconds
		Spin S1813 at 3500 RPM	30 seconds
		Softbake at 110 °C	1 minute
		Expose at 20 mW/cm^2	8 seconds
		Develop in MF319 at room temperature for 35 seconds, only to develop the S1813 photoresist not the lift-off resist.	
		Hardbake at 110°C	2 minutes
		Develop the Lift-off resist (LOR-10A) to create the re-entrant profile.	
		MF319	75 seconds
		Dehydrate 100 °C	2 minutes in convection oven.
24	NiCu alloy deposition	Base pressure:	less than 2x10^{-6} Torr
		Deposition pressure:	1 mTorr
		Source power:	150 W
		Deposition time:	3 minutes and 30 seconds
		Thickness:	120 nm
25	Lift-off the undesired NiCu	Lift-off the LOR-10A layer in Remover PG.	
		First bath at 75 °C	one hour with agitation
		Second bath at 75 ° C	10 minutes
Structural layer patterning			
26	Thick Photoresist spinning and patterning	Used S1827 thick photoresist and the sixth mask	
		Spin:	3500 RPM, 30 seconds
		Soft bake:	at 110 ° C for 1 minute and 30 seconds
		Exposure:	30 seconds at 20 mW/cm^2
		Develop:	MF319 for 1 minute
		Hard Bake:	at 110 ° C for 2 minutes
27	Top oxide etch	Fluorine base RIE	
		CF4:	50 sccm
		O2:	5 sccm
		Pressure:	100 mTorr
		Power:	200 Watts
		Etching time:	9 minutes
		Note: the RIE stops at the Nichrome layer; therefore over-etching is OK and timing is not very critical.	

#	Process title	Process parameters
28	Nichrome etching	Self aligned with the previous layer -Nichrome etch in Transene 1020AC Chromium etchant Etch time: 150 seconds Etch temperature: 45 °C
29	Bottom oxide etch	Self-aligned to the two top layers Fluorine base RIE CF4: 50 sccm O2: 5 sccm Pressure: 100 mTorr Power: 200 Watts Etching time: 9 minutes Note: the RIE-etch can etch part of the sacrificial layer; therefore over-etching is OK and timing is not very critical.
30	Photoresist removal	-Stripping photoresist by acetone (double bath).
Structure release		
31	Xenon Difluoride etch	Packaged and wire-bonded dies Etch chamber pressure: 3 Torr Number of pulsed: roughly 8 Note: Number of the necessary pulses to release the structure varies by the amount of the exposed silicon, especially the substrate side-walls. For best performance the Si substrate side-walls has to be covered by a passivation layer (e.g. photoresist or thermal epoxy)

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